



12-Lane 3-Port Non-Transparent PCI Express™ Switch

89PES12N3
Product Brief
*Preliminary Information**

Device Overview

The 89HPES12N3 is a member of IDT's family of PCI Express™ based bridge and switch devices offering the next-generation I/O interconnect standard. The PES12N3 is a 12-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, graphics, and communications/networking. It provides fan-out and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

In addition to transparent switching, one port of the PES12N3 may be configured to operate in non-transparent mode. This allows the PES12N3 to be used in multi-host and intelligent I/O applications such as communications, storage, and blade servers.

Features

High Performance PCI Express Switch

- ◆ 12 PCI Express lanes (2.5Gbps), 3 switch ports
- ◆ 3 GBps (24 Gbps) aggregate switching throughput
- ◆ Low latency cut-through switch architecture
- ◆ 128 to 2048 byte supported payload sizes
- ◆ One virtual channel
- ◆ Fully compliant with PCI Express Base specification Revision 1.0a

Flexible Architecture with Numerous Configuration Options

- ◆ One port configurable as downstream port or non-transparent port
- ◆ Automatic per port link width negotiation to x4, x2 or x1
- ◆ Port arbitration schemes utilizing round robin or weighted round robin algorithms
- ◆ Static lane reversal on all ports
- ◆ Polarity inversion
- ◆ Ability to load device configuration from serial EEPROM

Legacy Support

- ◆ PCI compatible INTx emulation
- ◆ Bus locking

Non-Transparent Port

- ◆ Four mapping windows supported
 - Each may be configured as a 32-bit memory or I/O window
 - May be paired to form a 64-bit memory window
- ◆ Interprocessor communication
 - 32 inbound and outbound doorbells
 - Four inbound and outbound message registers
 - Two shared shadow registers
- ◆ Allows up to 16 masters to communicate through the non-transparent port
- ◆ No limit on the number of supported outstanding

Block Diagram

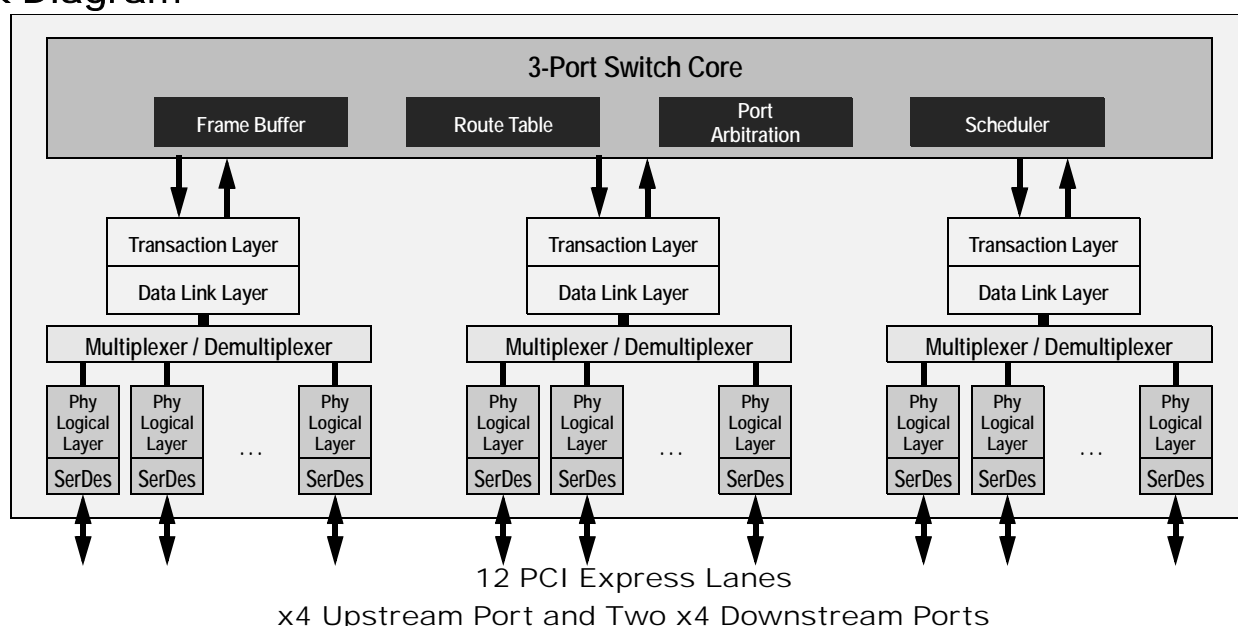


Figure 1 Internal Block Diagram

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- transactions through the non-transparent bridge
- ◆ Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run.
- ◆ Supports direct non-transparent port to non-transparent port connection

Highly Integrated Solution

- ◆ Requires no external components
- ◆ Incorporates on-chip internal memory for packet buffering and queuing
- ◆ Integrates 12 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)

Reliability, Availability, and Serviceability (RAS) Features

- ◆ Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
- ◆ Supports ECRC in transparent and non-transparent modes

Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O

- ◆ Compatible with Hot-Plug I/O expanders used on PC motherboards

Power Management

- ◆ Utilizes advanced low-power design techniques to achieve low typical power consumption
- ◆ Support PCI Express Power Management Interface specification (PCI-PM 1.1)
- ◆ Unused SerDes are disabled.
- ◆ Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state

Testability and Debug Features

- ◆ Support IEEE 1149.6 JTAG which extends the capability of the IEEE 1149.1 standard to include AC-coupled and/or differential nets
- ◆ Built in Pseudo-Random Bit Stream (PRBS) generator
- ◆ Numerous SerDes test modes
- ◆ Ability to read and write any internal register via the SMBus
- ◆ Ability to bypass link training and force any link into any mode
- ◆ Provides statistics and performance counters

8 General Purpose Input/Output pins

- ◆ Each pin may be individually configured as an input or output

- ◆ Each pin may be individually configured as an interrupt input
- ◆ Some pins have selectable alternate functions

Packaged in a 320-ball BGA

- ◆ 25x25 mm
- ◆ 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES12N3 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 3 GBps (24 GBps) of aggregated, switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES12N3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES12N3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 1 Gigabit I/Os, SATA controllers, and Fibre Channel HBAs.

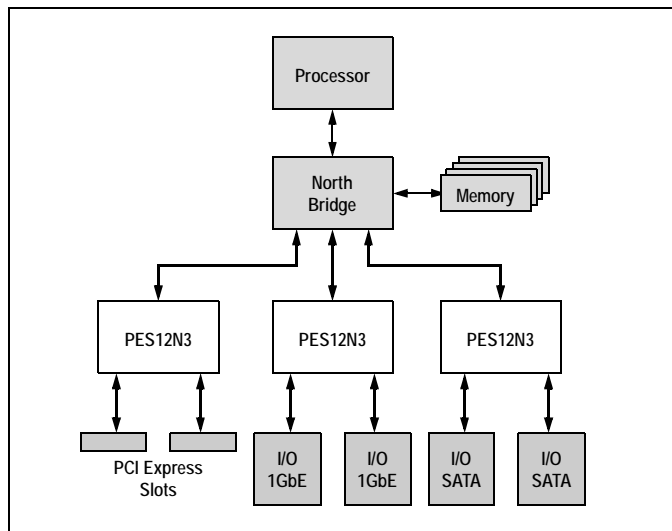


Figure 2 I/O Expansion Application



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-330-1748
 www.idt.com

for Tech Support:
 email: ssdhelp@idt.com
 phone: 408-492-8208