


# LOW SKEW, 1-TO-18 LVPECL-TO-LVCMOS/LVTTL FANOUT BUFFER

## ICS83940D

### GENERAL DESCRIPTION



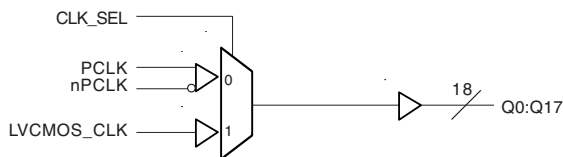
The ICS83940D is a low skew, 1-to-18 LVPECL-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS83940D has two selectable clock inputs. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The LVCMOS\_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The ICS83940D is characterized at full 3.3V and 2.5V or mixed 3.3V core, 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940D ideal for those clock distribution applications demanding well defined performance and repeatability.

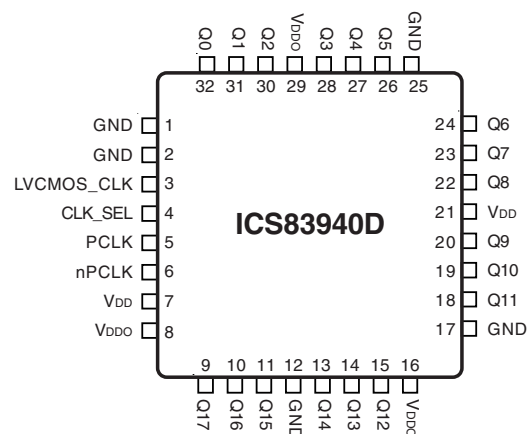
### FEATURES

- 18 LVCMOS/LVTTL outputs
- Selectable LVCMOS\_CLK or LVPECL clock inputs
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- LVCMOS\_CLK accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 250MHz
- Output skew: 150ps (maximum)
- Part to part skew: 750ps (maximum)
- Additive phase jitter, RMS: < 0.03ps (typical)
- Full 3.3V and 2.5V or mixed 3.3V core, 2.5V output supply modes
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Pin compatible with the MPC940L

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**  
7mm x 7mm x 1.4mm package body  
**Y Package**  
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Power supply ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Selects LVCMOS / LVTTL clock input when HIGH. Selects PCLK, nPCLK inputs when LOW. LVCMOS / LVTTL interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7, 21	$V_{DD}$	Power		Core supply pins.
8, 16, 29	$V_{DDO}$	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels.

NOTE: Pullup and Pulldown refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$C_{PD}$	Power Dissipation Capacitance (per output)			6		pF
$R_{PULLUP}$	Input Pullup Resistor			51		$K\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		$K\Omega$
$R_{OUT}$	Output Impedance		18		28	$\Omega$

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock		
	CLK_SEL	PCLK, nPCLK	LVCMOS_CLK
0	Selected	De-selected	
1	De-selected	Selected	

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	PCLK	nPCLK	Q0:Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	3.6V
Inputs, $V_I$	-0.3V to $V_{DD} + 0.3V$
Outputs, $V_O$	-0.3V to $V_{DDO} + 0.3V$
Input Current, $I_{IN}$	$\pm 20mA$
Storage Temperature, $T_{STG}$	-40°C to 125°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVC MOS_CLK	2.4		$V_{DD}$	V
$V_{IL}$	Input Low Voltage	LVC MOS_CLK			0.8	V
$V_{PP}$	Peak-to-Peak Input Voltage	PCLK, nPCLK	500		1000	mV
$V_{CMR}$	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK	$V_{DD} - 1.4$		$V_{DD} - 0.6$	V
$I_{IN}$	Input Current				$\pm 200$	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OH} = -20mA$	2.4			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 20mA$			0.5	V
$I_{DD}$	Core Supply Current				25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.6	3.0	ns
		LVC MOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.8	3.0	ns
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.6	3.3	ns
		LVC MOS_CLK; NOTE 2, 5	$f > 150MHz$	1.8	3.2	ns
$t_{sk(o)}$	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		150	ps
		LVC MOS_CLK			150	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$		1.4	ns
		LVC MOS_CLK	$f \leq 150MHz$		1.2	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150MHz$		1.7	ns
		LVC MOS_CLK	$f > 150MHz$		1.4	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		850	ps
		LVC MOS_CLK			750	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7			0.03		ps
$t_R / t_F$	Output Rise/Fall Time	0.5 to 2.4V	0.3		1.1	ns
odc	Output Duty Cycle	$f < 134MHz$	45	50	55	%
		$134MHz \leq f \leq 250MHz$	40	50	60	%

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 7: Driving only one input clock.

**TABLE 4B. DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVC MOS_CLK	2.4		$V_{DD}$	V
$V_{IL}$	Input Low Voltage	LVC MOS_CLK			0.8	V
$V_{PP}$	Peak-to-Peak Input Voltage	PCLK, nPCLK	300		1000	mV
$V_{CMR}$	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK	$V_{DD} - 1.4$		$V_{DD} - 0.6$	V
$I_{IN}$	Input Current				$\pm 200$	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OH} = -20mA$	1.8			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 20mA$			0.5	V
$I_{DD}$	Core Supply Current				25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.7	3.2	ns
		LVC MOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.7	3.0	ns
$t_{PLH}$	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.6	3.4	ns
		LVC MOS_CLK; NOTE 2, 5	$f > 150MHz$	1.8	3.3	ns
$t_{sk(o)}$	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		150	ps
		LVC MOS_CLK			150	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$		1.5	ns
		LVC MOS_CLK	$f \leq 150MHz$		1.3	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150MHz$		1.8	ns
		LVC MOS_CLK	$f > 150MHz$		1.5	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		850	ps
		LVC MOS_CLK			750	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7			0.03		ps
$t_R / t_F$	Output Rise/Fall Time	0.5 to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle	$f < 134MHz$	45	50	55	%

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 7: Driving only one input clock.

TABLE 4C. DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	LVC MOS_CLK	2		$V_{DD}$	V
$V_{IL}$	Input Low Voltage	LVC MOS_CLK			0.8	V
$V_{PP}$	Peak-to-Peak Input Voltage	PCLK, nPCLK	300		1000	mV
$V_{CMR}$	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK	$V_{DD} - 1.4$		$V_{DD} - 0.6$	V
$I_{IN}$	Input Current				$\pm 200$	$\mu A$
$V_{OH}$	Output High Voltage	$I_{OH} = -12mA$	1.8			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 12mA$			0.5	V
$I_{DD}$	Core Supply Current				25	mA

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

TABLE 5C. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ$  TO  $70^\circ$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				200	MHz
$t_{PLH}$	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	$f \leq 150MHz$	1.2	3.8	ns
		LVC MOS_CLK; NOTE 2, 5	$f \leq 150MHz$	1.5	3.2	ns
$t_{PLH}$	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	$f > 150MHz$	1.5	3.7	ns
		LVC MOS_CLK; NOTE 2, 5	$f > 150MHz$	2	3.6	ns
$t_{sk(o)}$	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		200	ps
		LVC MOS_CLK			200	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150MHz$		2.6	ns
		LVC MOS_CLK	$f \leq 150MHz$		1.7	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150MHz$		2.2	ns
		LVC MOS_CLK	$f > 150MHz$		1.7	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @ $V_{DDO}/2$		1.2	ns
		LVC MOS_CLK			1.0	ns
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 7			0.03		ps
$t_R / t_F$	Output Rise/Fall Time	0.5 to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle	$f < 134MHz$	45		55	%

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output  $V_{DDO}/2$ .

NOTE 2: Measured from  $V_{DD}/2$  to  $V_{DDO}/2$ .

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges,

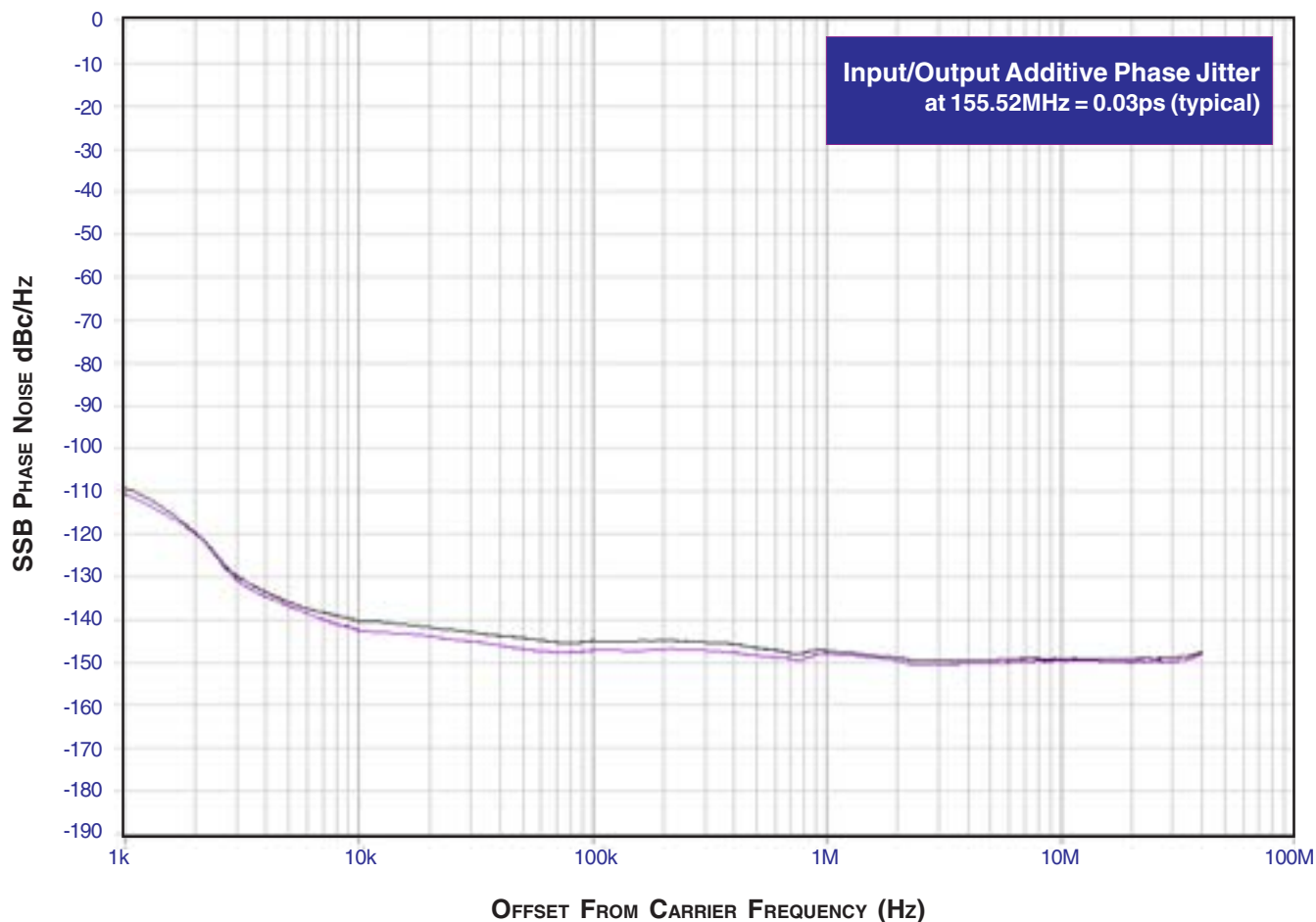
and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 7 Driving only one input clock.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

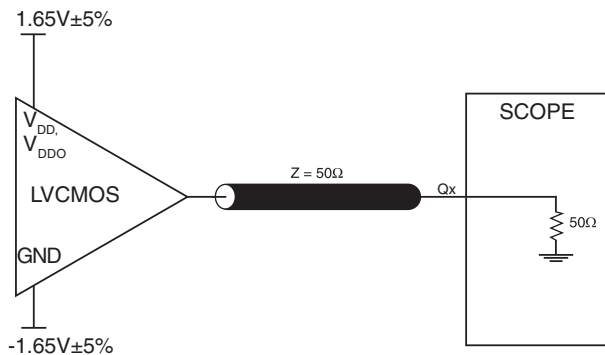
the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



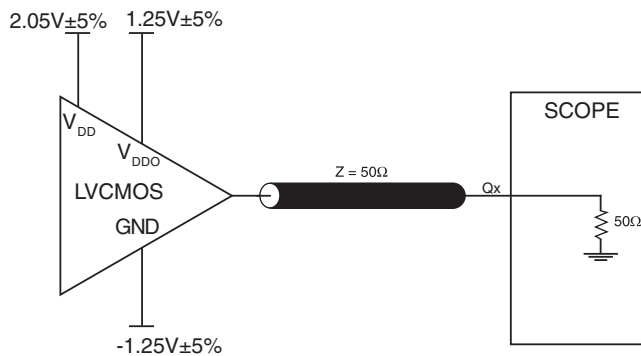
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The de-

vice meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

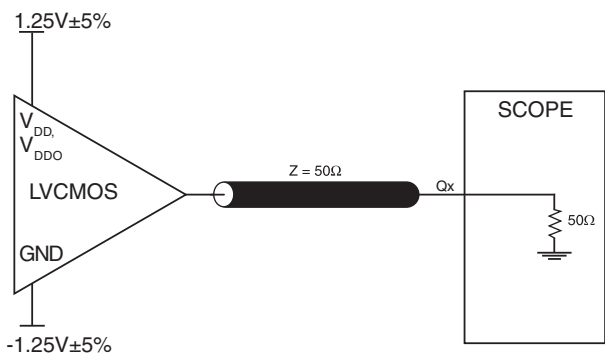
## PARAMETER MEASUREMENT INFORMATION



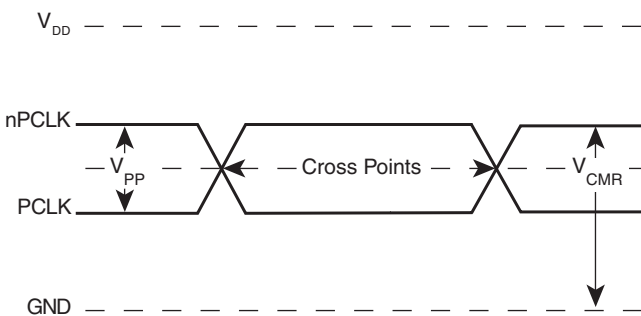
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



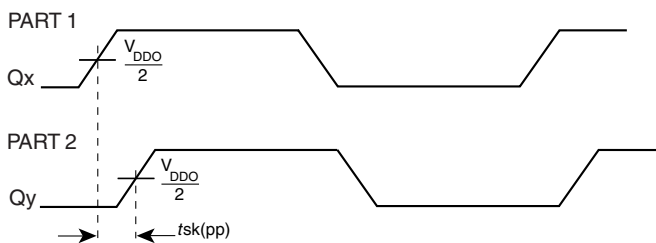
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



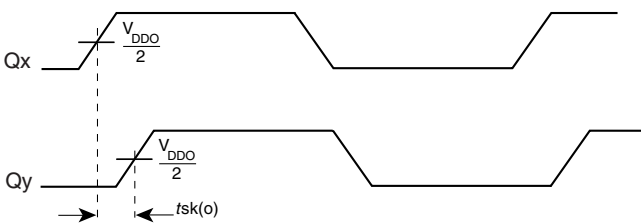
**2.5V OUTPUT LOAD AC TEST CIRCUIT**



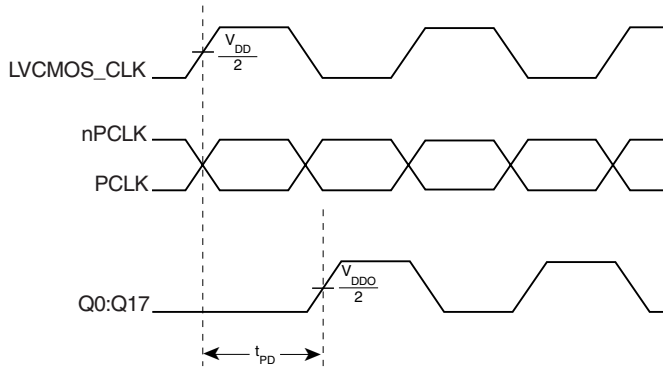
**DIFFERENTIAL INPUT LEVEL**



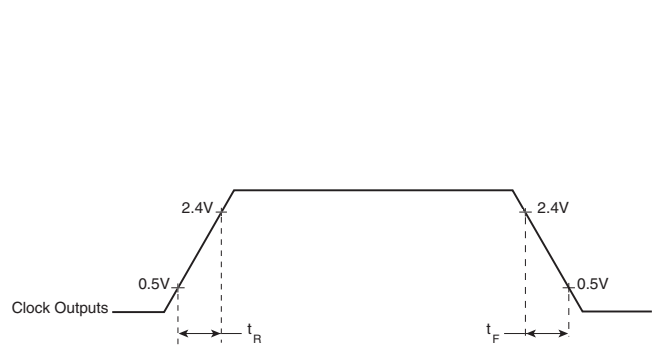
**PART-TO-PART SKEW**



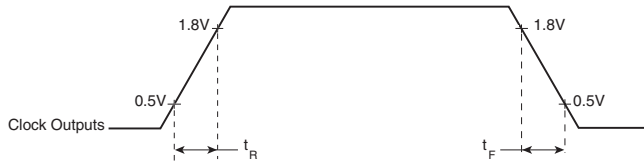
**OUTPUT SKEW**



PROPAGATION DELAY



3.3V OUTPUT RISE/FALL TIME



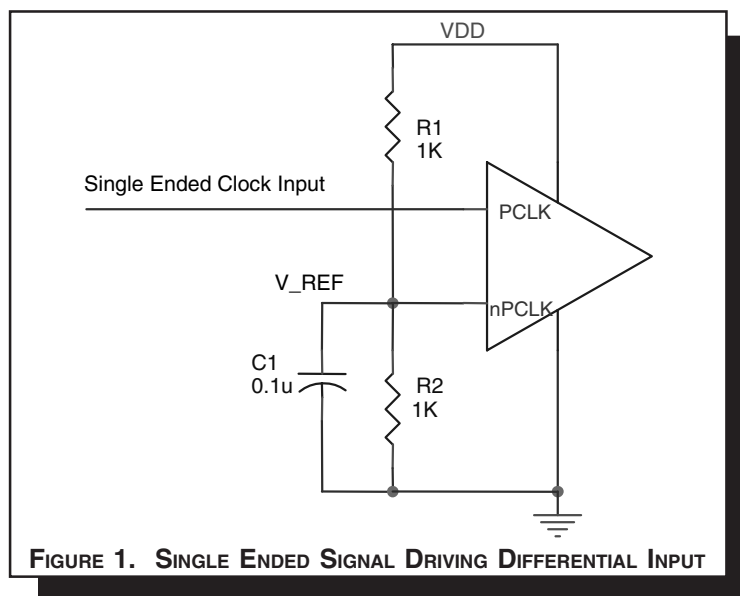
2.5V OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin.

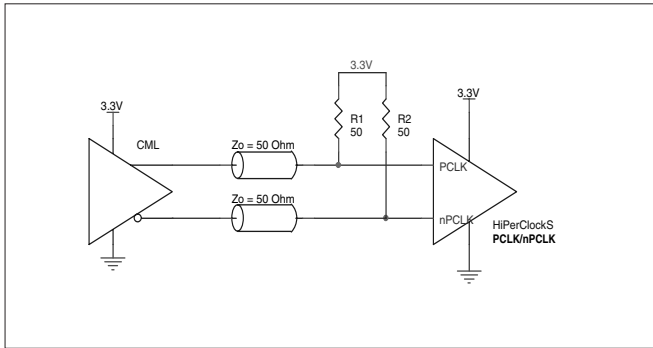
of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .



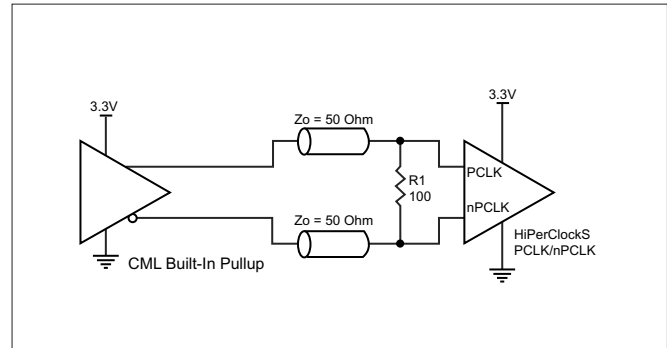
## LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested

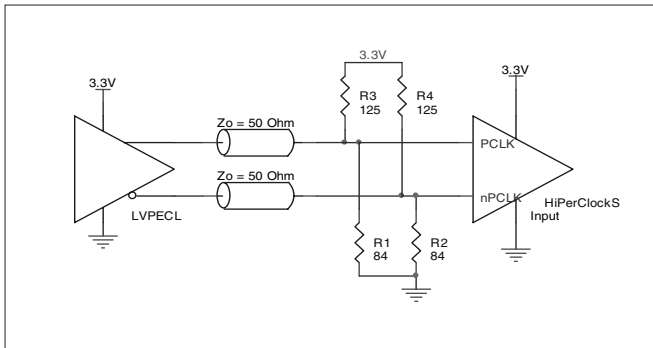
here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



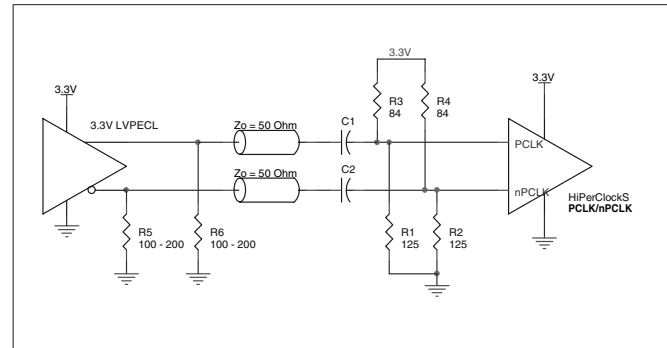
**FIGURE 2A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**



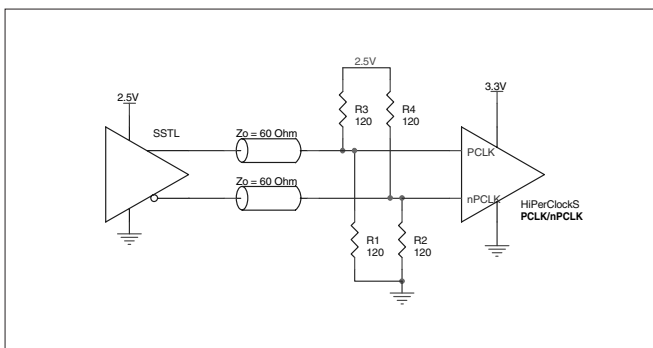
**FIGURE 2B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**



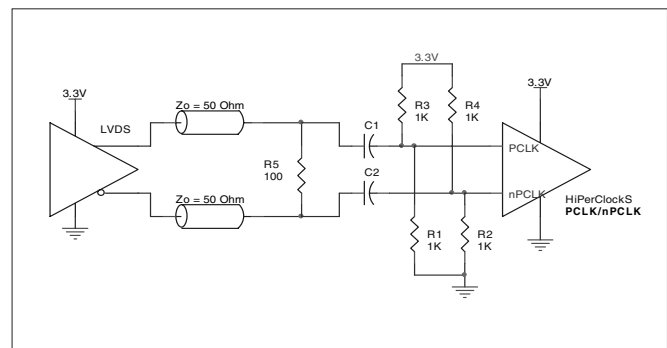
**FIGURE 2C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 2D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**



**FIGURE 2E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**



**FIGURE 2F. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD LQFP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS83940D is: 820

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

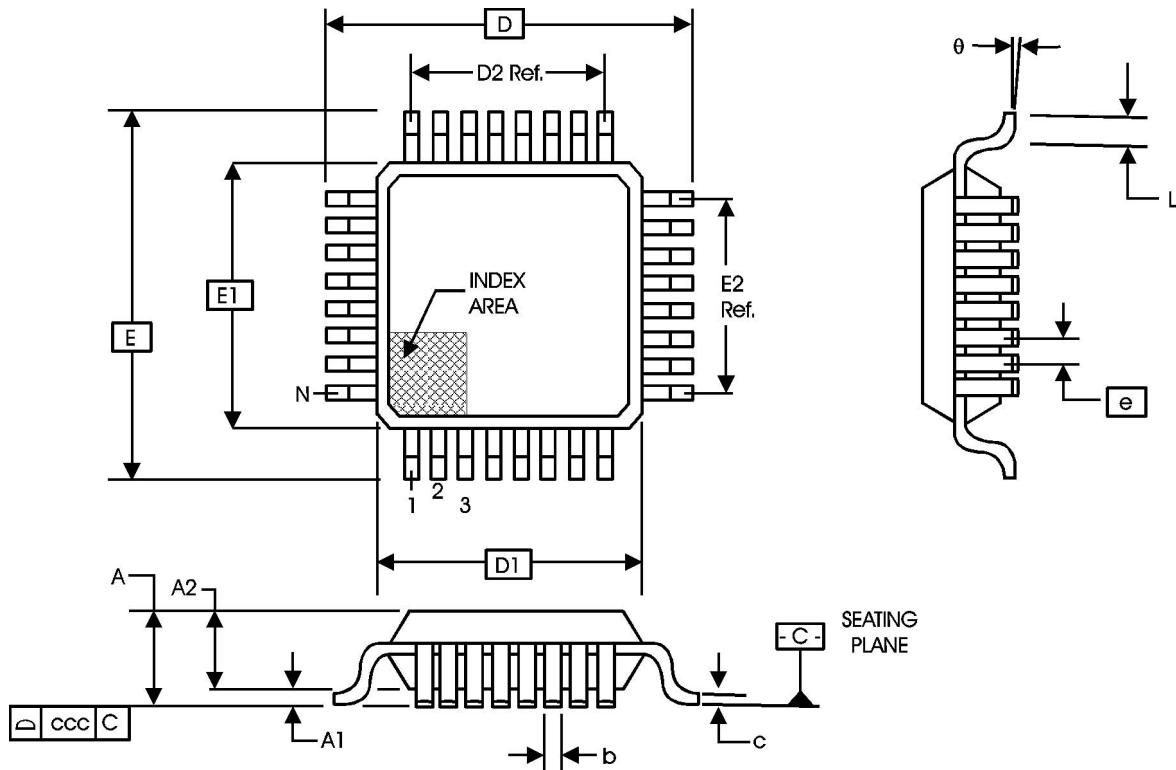


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83940DY	ICS83940DY	32 Lead LQFP	250 per tray	0°C to 70°C
ICS83940DYT	ICS83940DY	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C
ICS83940DYLF	ICS83940DYLF	32 Lead "Lead Free" LQFP	250 per tray	0°C to 70°C
ICS83940DYLF	ICS83940DYLF	32 Lead "Lead Free" LQFP on Tape and Reel	1000	0°C to 70°C

The aforementioned trademark, HiPerClockS™ is a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries. While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T5A	4	3.3V AC Characteristics table - <ul style="list-style-type: none"> <li>tsk(pp) Test Conditions, replaced "&lt;" with "≤"; corrected Units to "ns" from "ps".</li> <li>odc - corrected Test Conditions to read "134MHz ≤ f ≤ 250MHz", from "f ≤ 250MHz".</li> </ul>	10/11/02
	T5B	5	3.3V/2.5V AC Characteristics table - tsk(pp) Test Conditions, replaced "<" with "≤"; corrected Units to read "ns" from "ps".	
	T5C	6	2.5V AC Characteristics table - tsk(pp) Test Conditions, replaced "<" with "≤"; corrected Units to "ns" from "ps".	
A	T2	2	Pin Characteristics table - changed R <sub>OUT</sub> 25Ω maximum to 28Ω maximum. Delete R <sub>PULLUP</sub> row.	12/12/02
		7	3.3V Output Load AC Test Circuit diagram - corrected GND equation to read -1.65V... from -1.165V... Added LVTTTL to title. Updated format.	
B	T1	2	Pin Description Table - added <i>Pullup</i> and <i>Pulldown</i> to Pin 6, nPCLK.	10/9/03
	T2	2	Pin Characteristics Table - added R <sub>PULLUP</sub> row.	
	T5A	4	Added tjit row.	
	T5B T5C	5	Added tjit row.	
		6	Added tjit row.	
		7	Added <i>Additive Phase Jitter</i> section.	
	10	Updated <i>Single Ended Signal Driving Differential Input</i> diagram.		
	11	Added <i>LVPECL Clock Interface</i> section.		
B	T5A - T5C	1	Added "Lead-Free" bullet to Features section.	6/15/04
		4 - 6	Added NOTE 7.	
		11	Updated LVPECL Clock Input Interface section.	
		14	Ordering Information table - added "Lead-Free" part number.	

Innovate with IDT and accelerate your future networks. Contact:

**www.IDT.com**

**For Sales**

800-345-7015  
408-284-8200  
Fax: 408-284-2775

**For Tech Support**

clockhelp@idt.com  
408-284-8200

---

**Corporate Headquarters**

Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road  
San Jose, CA 95138  
United States  
800 345 7015  
+408 284 8200 (outside U.S.)

**Asia Pacific and Japan**

Integrated Device Technology  
Singapore (1997) Pte. Ltd.  
Reg. No. 199707558G  
435 Orchard Road  
#20-03 Wisma Atria  
Singapore 238877  
+65 6 887 5505

**Europe**

IDT Europe, Limited  
Prime House  
Barnett Wood Lane  
Leatherhead, Surrey  
United Kingdom KT22 7DE  
+44 1372 363 339