

TWO CHANNEL AC'97 2.3 CODEC WITH STEREO MIC, JACK/MIC SENSING
STAC9766/67 CC1
Overview

The current errata and updates for the STAC9766/67 revision CC1 are described below. These items were gathered through *preliminary evaluation*, if additional items are identified, notice will be given. Device reliability, life span, and suitability for intended use are not affected. Product covered by this errata carry standard guarantee and warranties.

Product Summary

Product can be identified in several ways. The main part number is located below the logo. The revision code can be found in the first four digits in the lot code. Product can be identified specifically through the software accessible registers as indicated in the table below. It is recommended that software programmers incorporate identification and adjustment code for the STAC9766/67 device revisions when updating drivers.

Revision Code Marking	CC1
Issue Date	August 2002
Vendor ID1 Register (index 7Ch)	8384h
Vendor ID2 Register (index 7Eh)	7666h
Date Code identification**	Date Code 0337 and higher
Production Status	Production

Table1. STAC9766/67Product Identification

** Date code can be found on the last line of the codec's marking

Errata Items

The items for the CC1 revision are listed in the chart below and are described in more detail below.

Errata Item	Issue
SPDIF Out	SPDIF Out issue at sample rates below 48 kHz

Table2. STAC9766/67CC1 Errata Items

- The SPDIF Out functionality is unreliable at sample rates lower than 48 kHz. This can occur in two situations. The first is if the audio stream is muted or paused/stopped by an application while data is being sent to SPDIF Out. The second is if the controller cannot access DMA data from memory to supply it to the codec. In either of these cases, the SPDIF Out data will stop. This occurs at sample rates lower than 48 kHz. Operation at 48 kHz is not affected and functions as expected.

NOTE: On STAC9766/67 CC1 codecs with a date code of 0337 or higher, pin 48, SPDIF Out, can properly be disabled with an external pull-up. This state will be reflected in bit D2 (SPDIF) of Register 28h. D2 is a status bit (Read Only) that reflects that status of pin 48 during the reset event. The value will change from 0605h to 0601h.

NOTE: The Recommendation for Double Reset is ***no longer applicable*** to STAC9766/67 CC1 units with a date code of 0337 or higher. If the double reset was implemented, there will no adverse effect using this product in those systems. The errata item for the Global ON/OFF 3D workaround is also no longer needed.

Please note there are no additional errata items at this time.

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