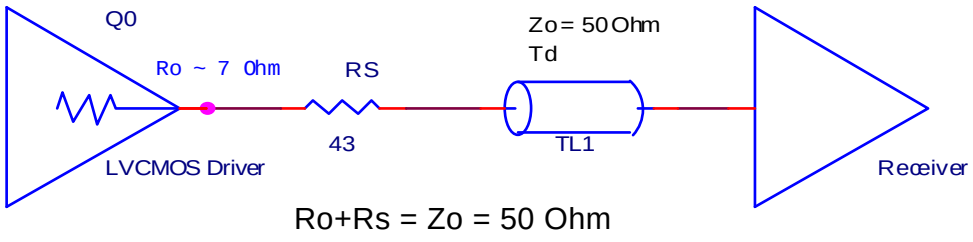
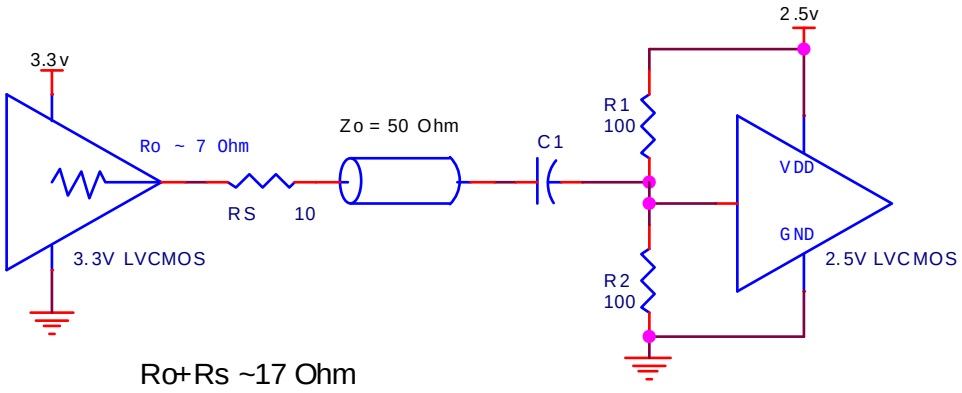
LVCMOS Terminations

Figure 1. LVCMOS Series Termination



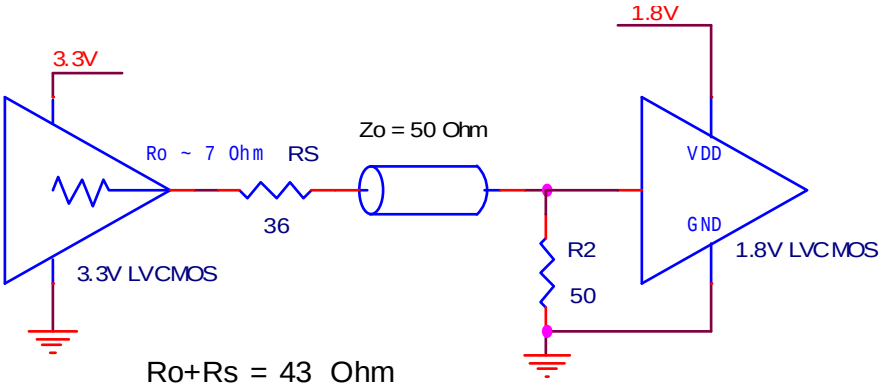
Ro+Rs = Zo = 50 Ohm

Figure 2. LVCMOS to 2.5V LVCMOS



Ro+Rs ~17 Ohm

Figure 3. LVCMOS to 1.8V



Ro+Rs = 43 Ohm

Figure 4. LVCMOS Signal to Differential Input

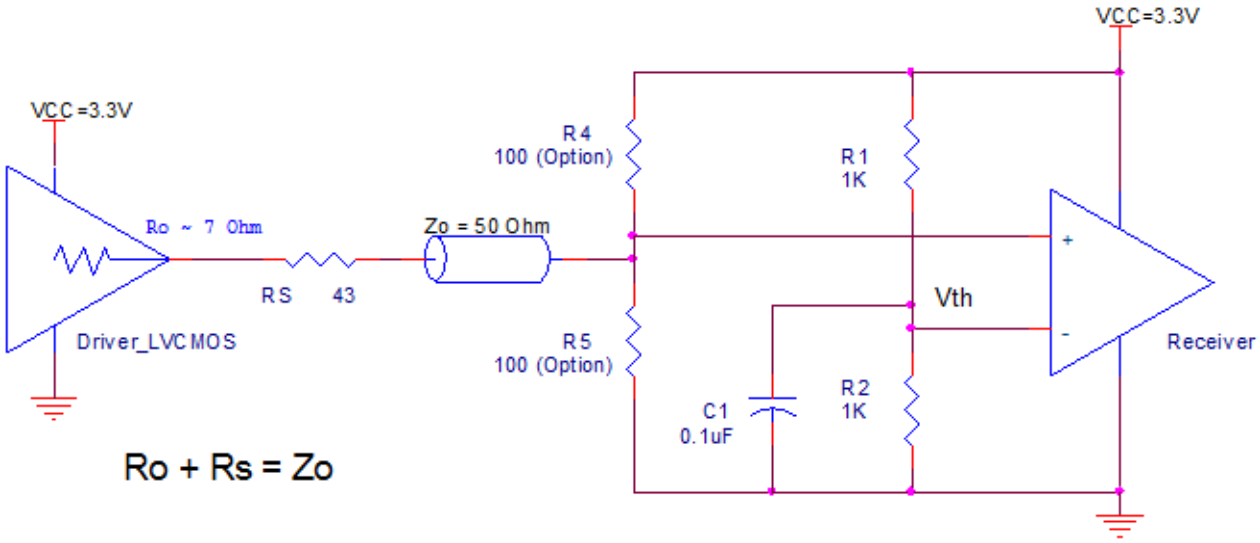
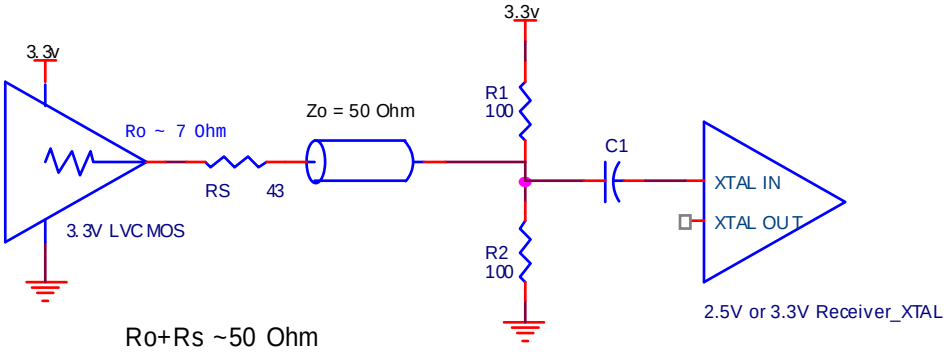
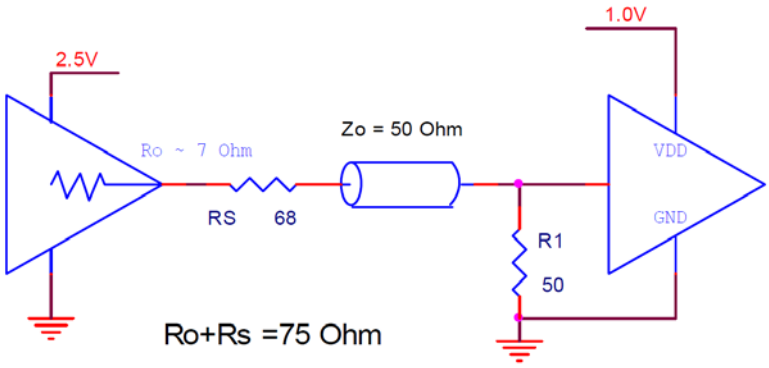


Figure 5. LVCMOS Overdrive XTAL Input



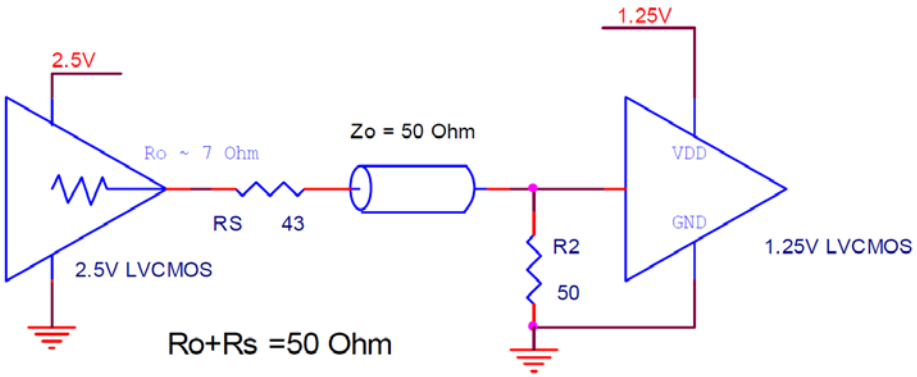
Increase Rs to reduce the amplitude

Figure 6. LVCMOS to 1.0V LVCMOS



The Rs may need to be slightly adjusted to obtain proper logic high level at the receiver.

Figure 7. LVCMOS to 1.25V LVCMOS



The Rs may need to be slightly adjusted to obtain proper logic high level at the receiver.

Figure 8. LVCMOS to 3.3V LVCMOS, Series Termination

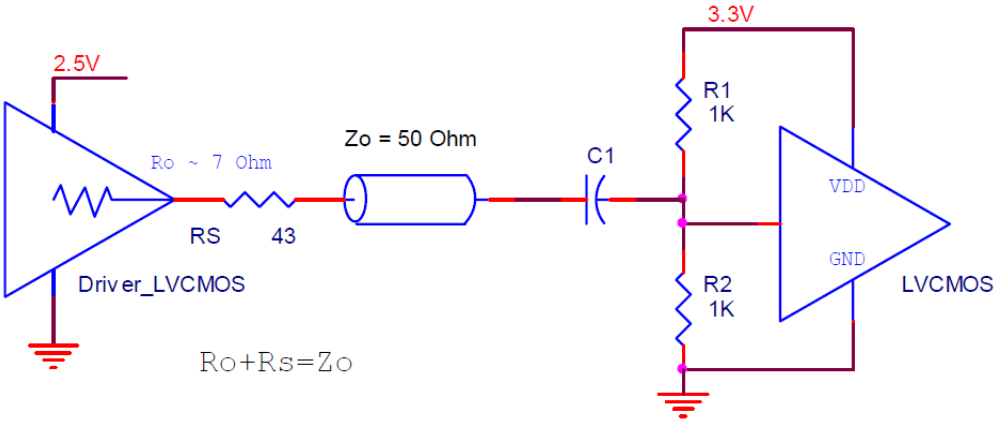


Figure 9. LVCMOS to 3.3V LVCMOS, Parallel Termination

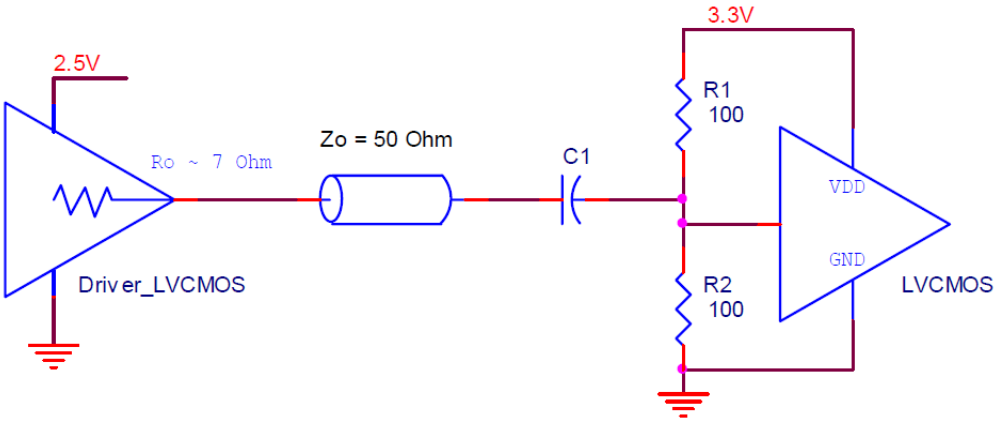


Figure 10. LVCMOS to Differential Input with built-in Termination and DC Bias

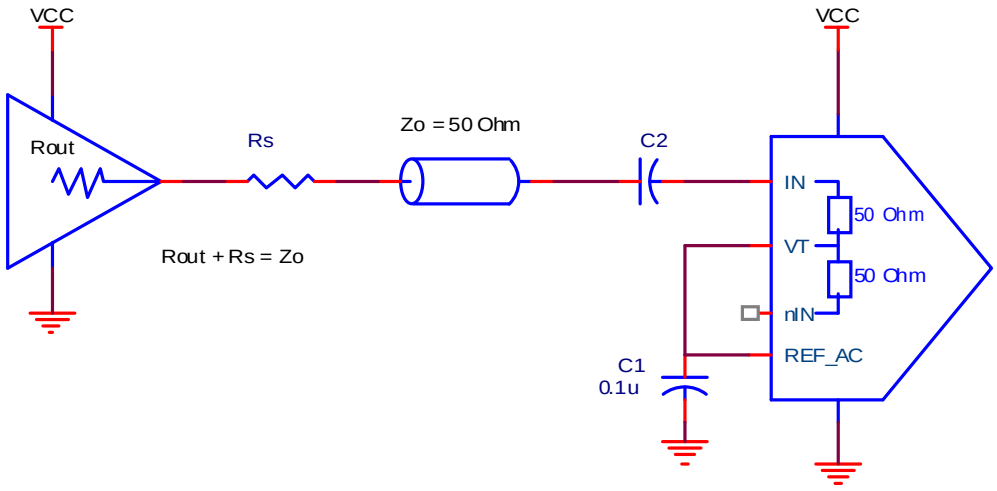
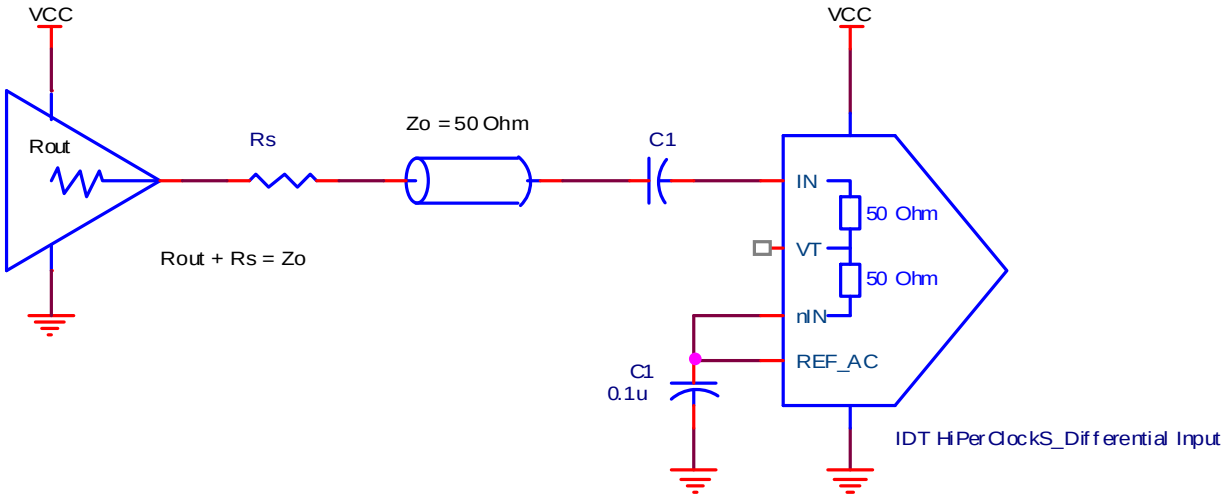


Figure 11. Alternative LVCMOS to Differential Input with Built-in Termination and DC Bias



Increase Rs if amplitude reduction is necessary.

Figure 12. LVCMOS to 1V BCM56700

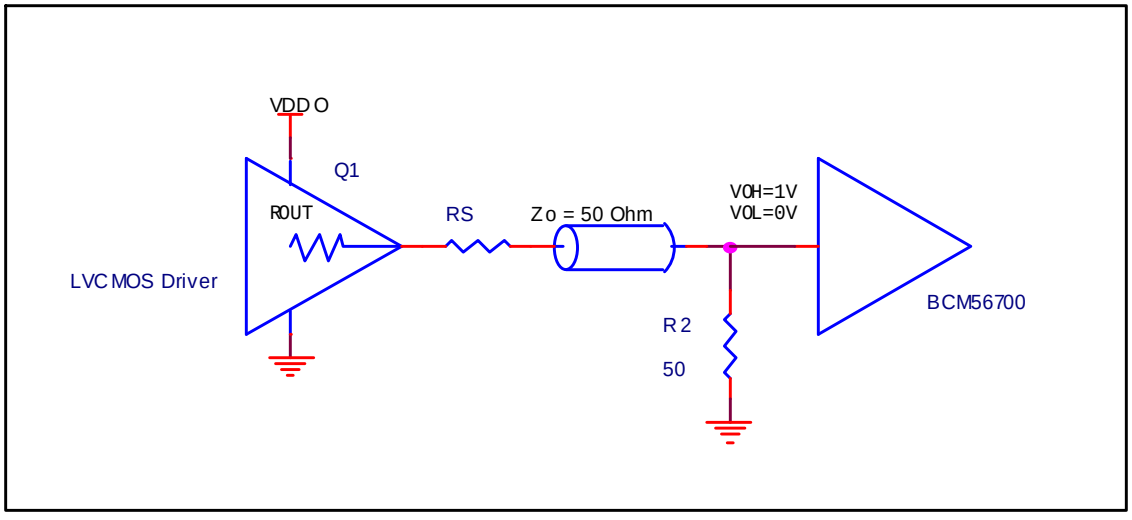
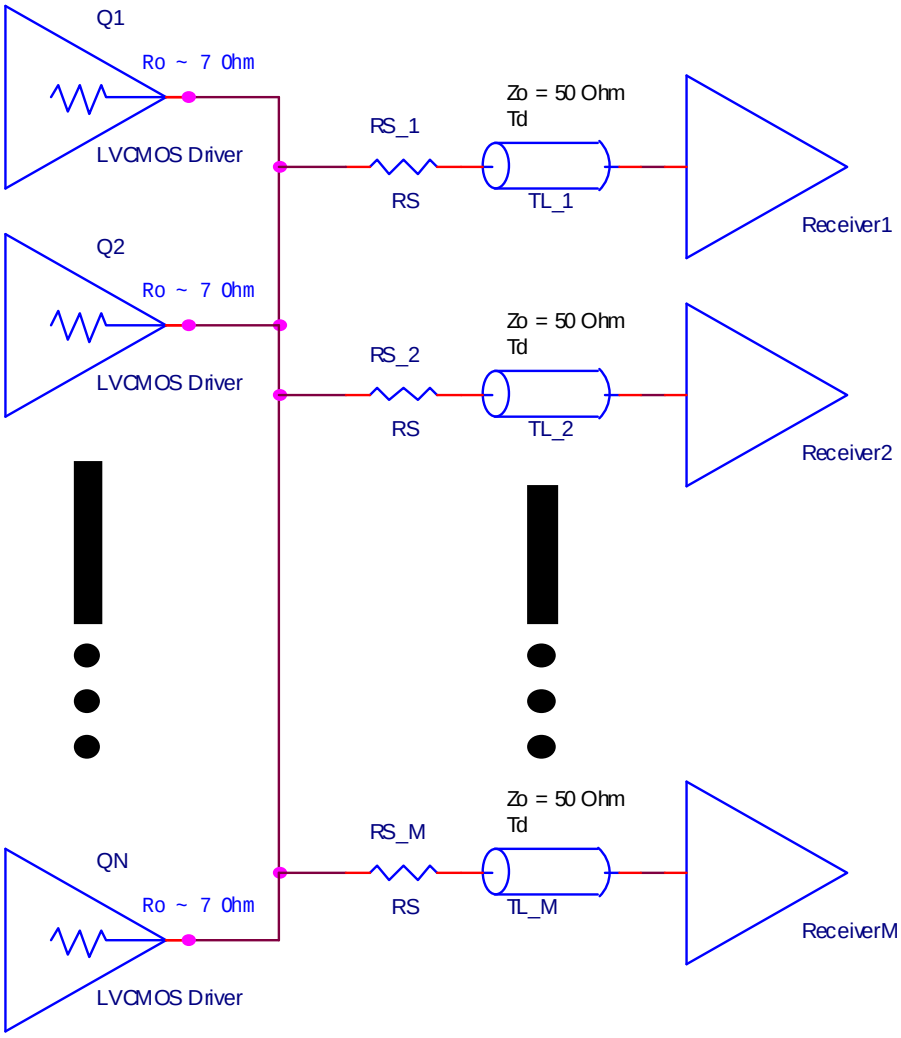


Figure 13. LVCMOS Tie N Outputs Together to Drive M Receivers



Rs = Zo - (Ro x M)/(N)

LVPECL Terminations

Figure 14. 3.3V LVPECL Standard Termination

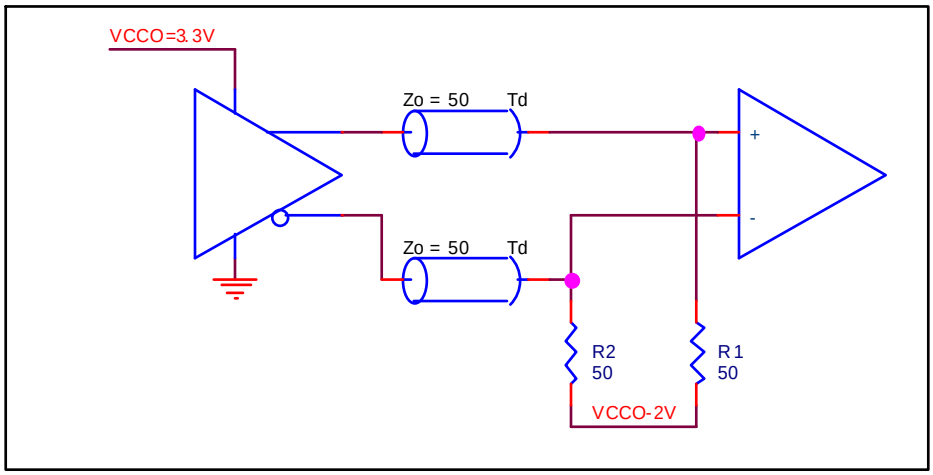


Figure 15. 3.3V LVPECL Equivalent Termination

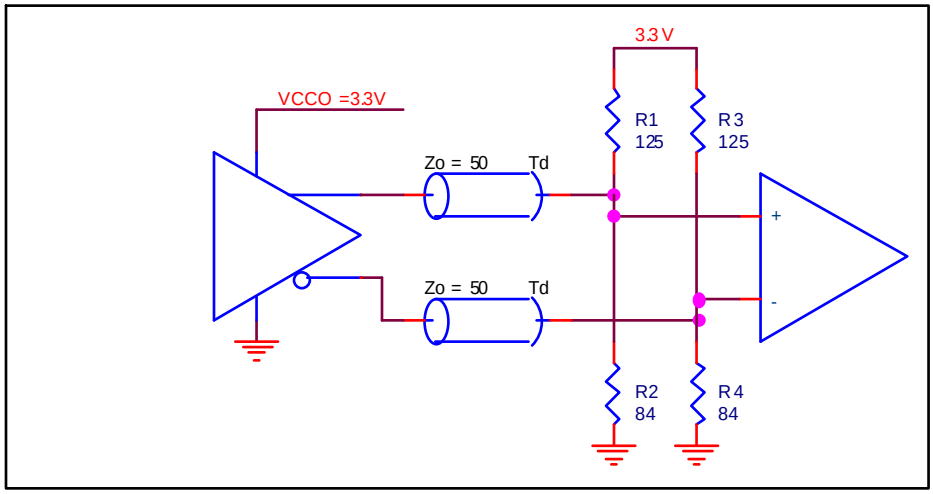


Figure 16. 3.3V LVPECL Equivalent Termination

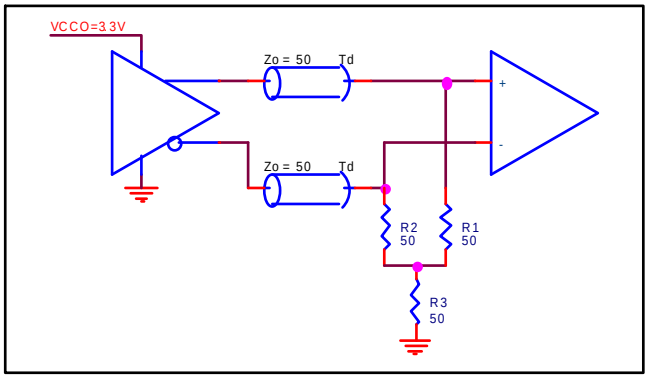


Figure 17. 3.3V LVPECL Offset to VCC - 2V

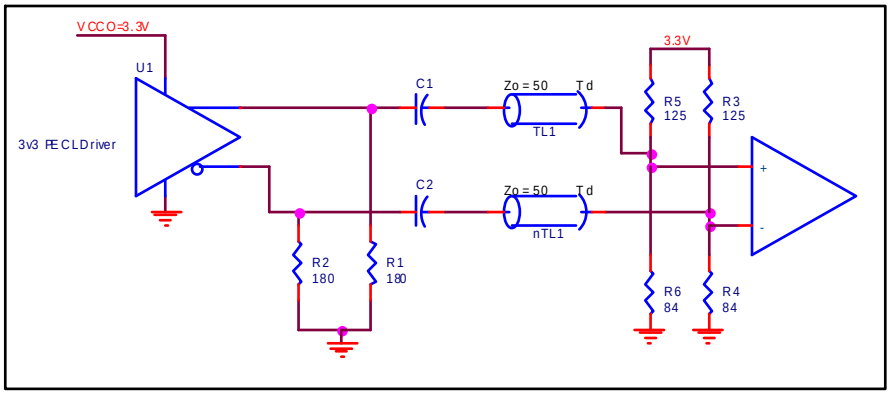


Figure 18. 3.3V LVPECL Offset to VCC - 1.3V

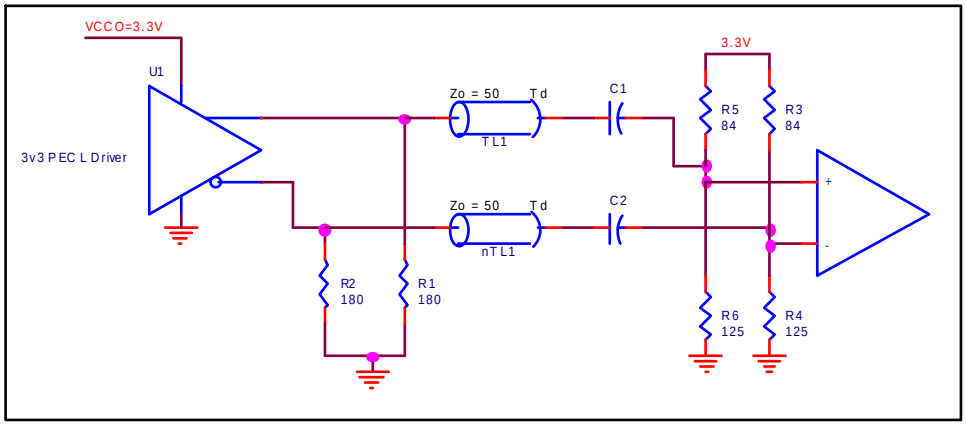


Figure 19. 3.3V LVPECL Driver to 1.5V SSTL

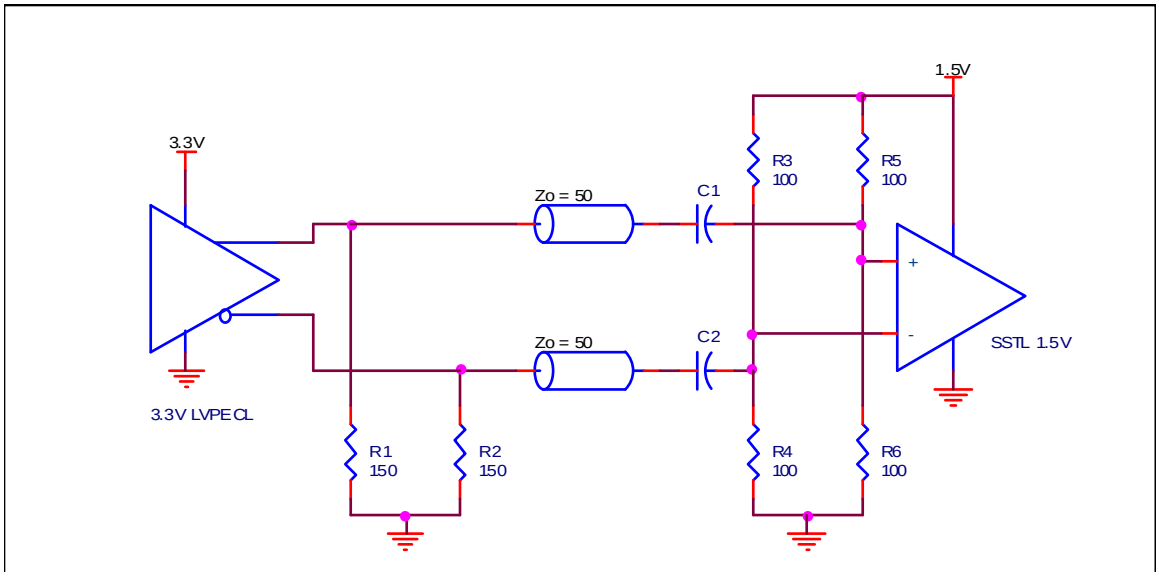


Figure 20. 3.3V LVPECL Driver to 1.8V SSTL

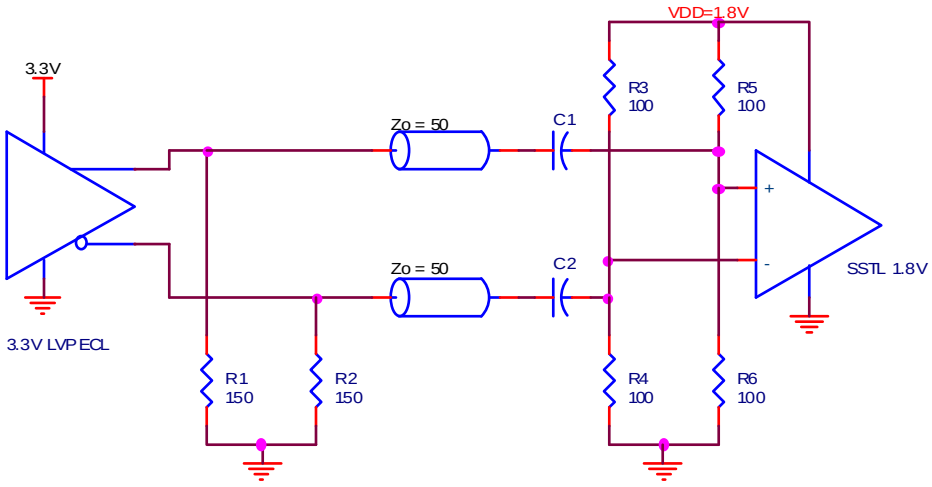


Figure 21. 3.3V LVPECL Driver to 1.8V SSTL, Thevenin Termination

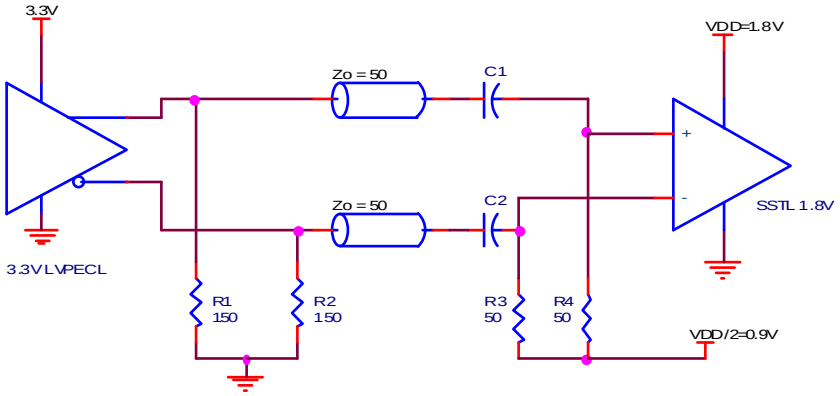
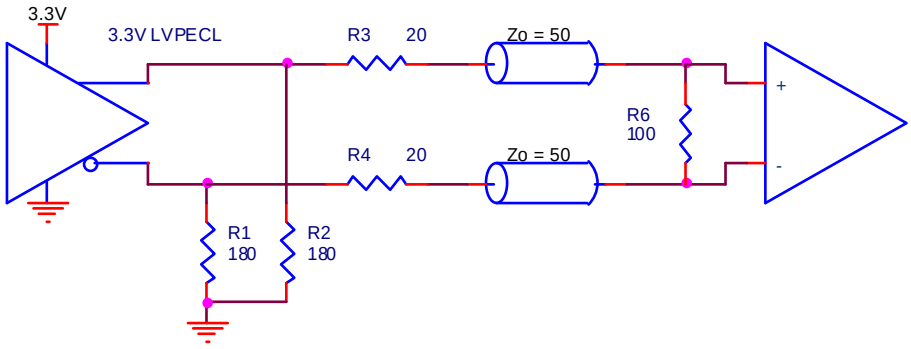


Figure 22. 3.3V LVPECL Termination Amplitude Reduction



Larger R3/R4 resistance further reduces the amplitude.

Figure 23. 3.3V LVPECL to 2.5 Differential Input with High DC Offset Requirement

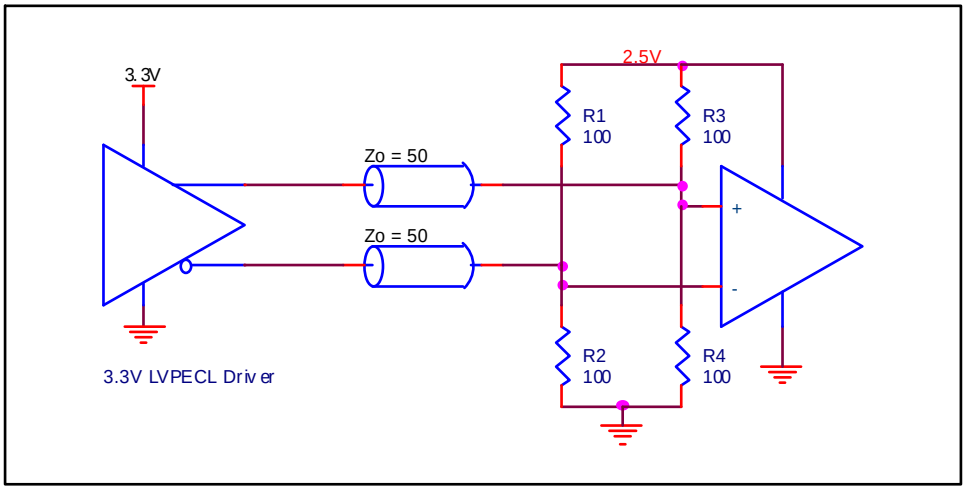


Figure 24. 3.3V LVPECL to LVDS, Option 1

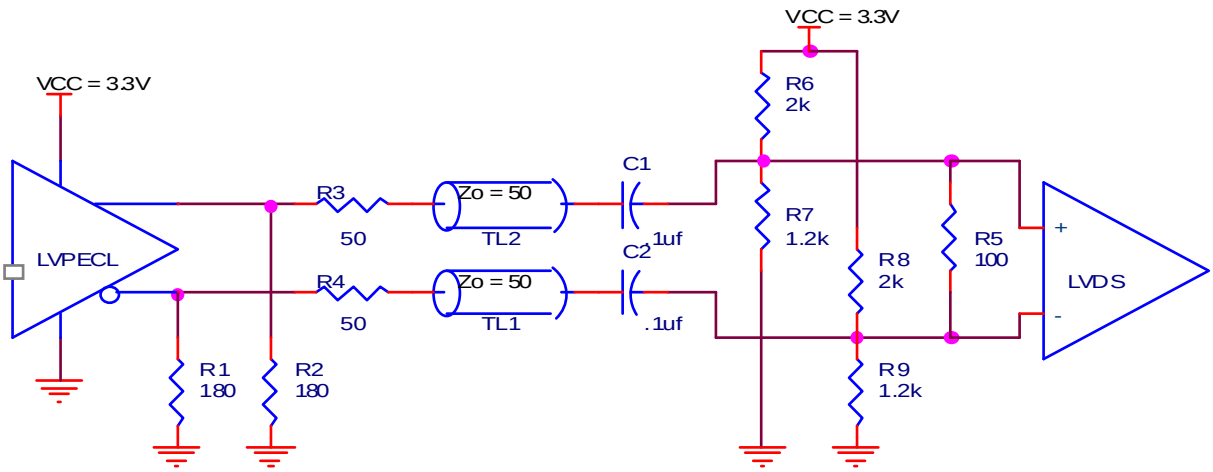


Figure 25. 3.3V LVPECL to LVDS, Option 2

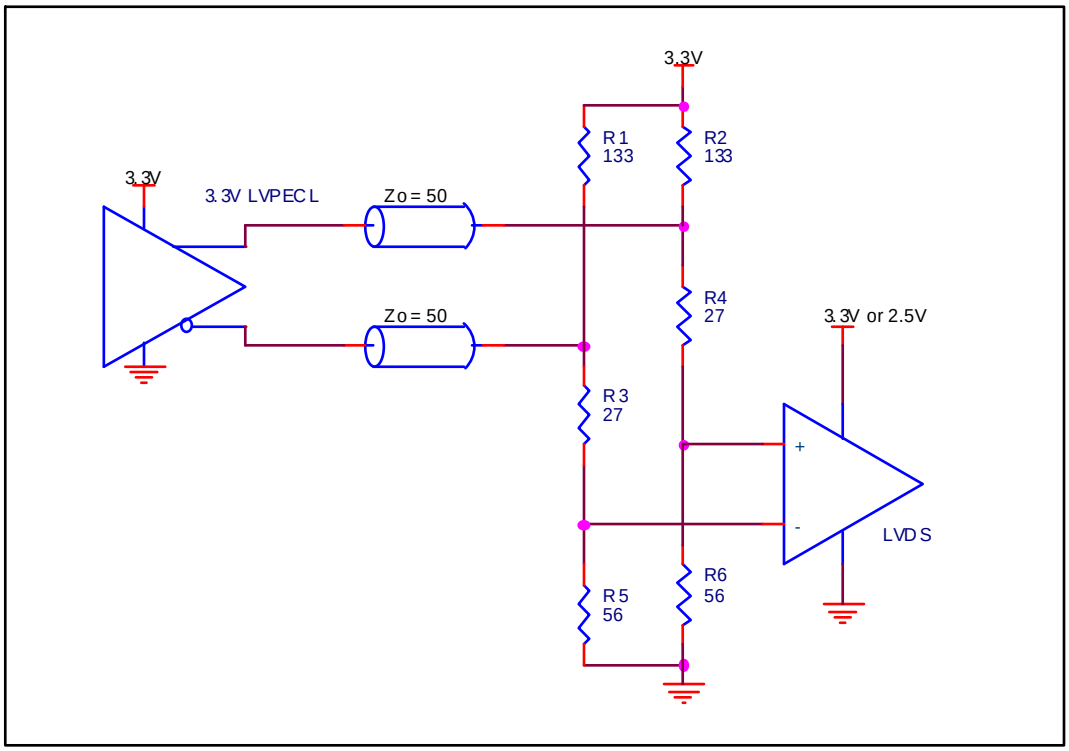
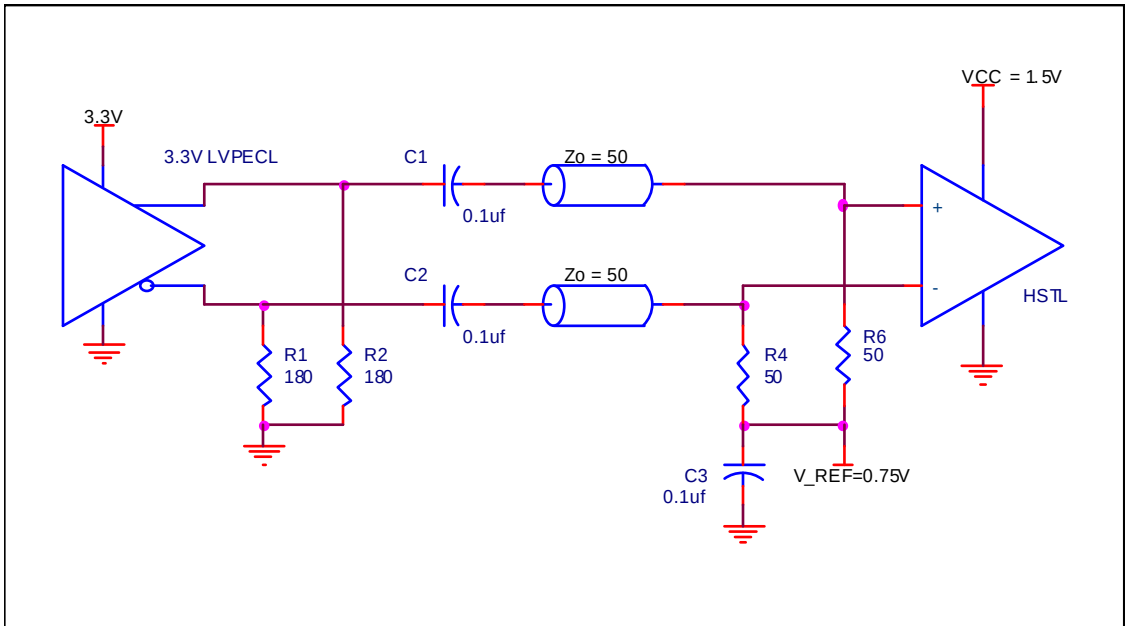


Figure 26. LVPECL to HSTL, Receiver VCC=1.5V and V_REF=0.75V, Option 1



Use this option if there is 0.75V rail available.

Figure 27. LVPECL to HSTL, Receiver VCC=1.5V and V_REF=0.75V, Option 2

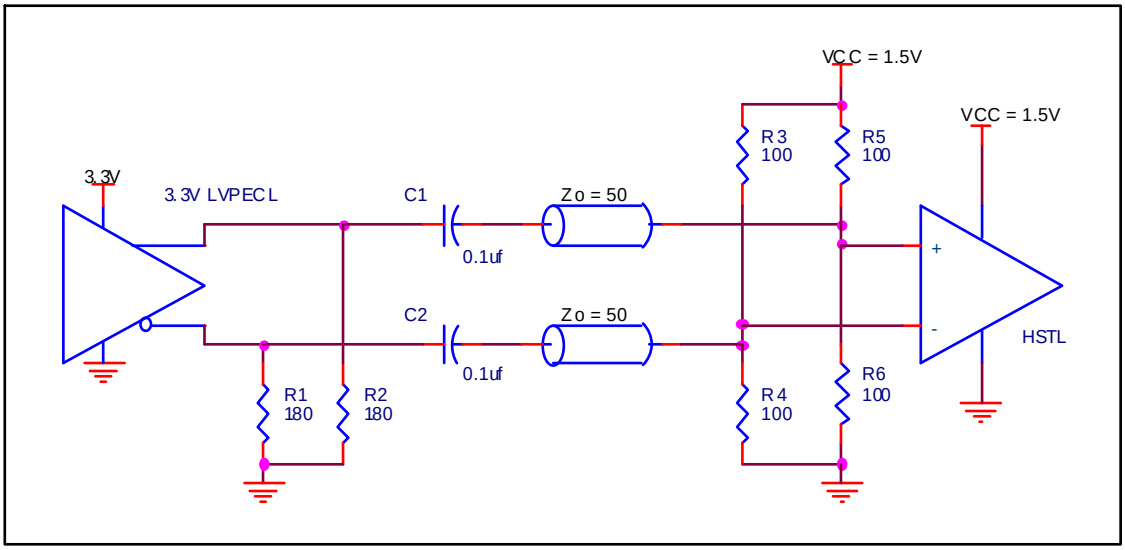


Figure 28. LVPECL to HSTL, Receiver VCC=3.3V

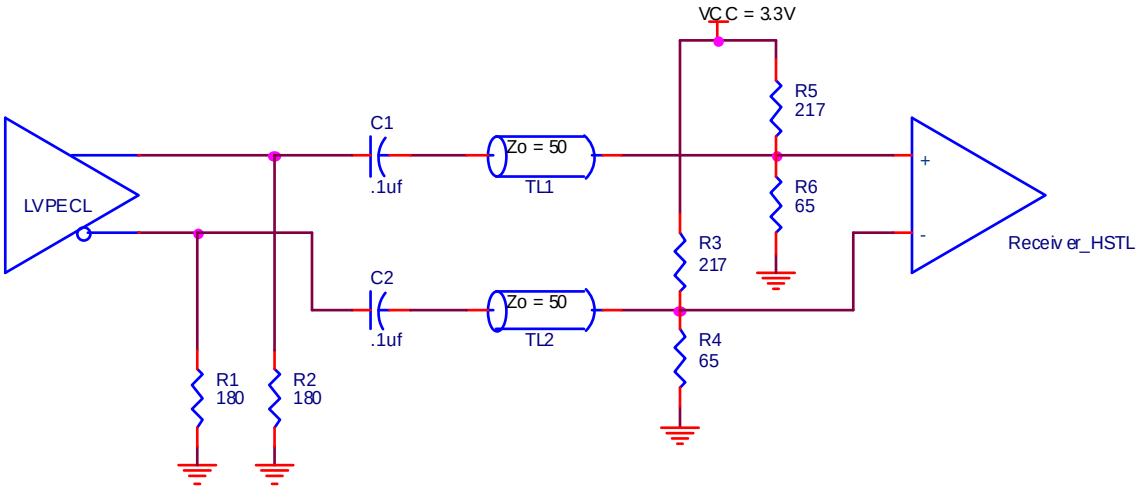


Figure 29. LVPECL to HCSL (DCM)

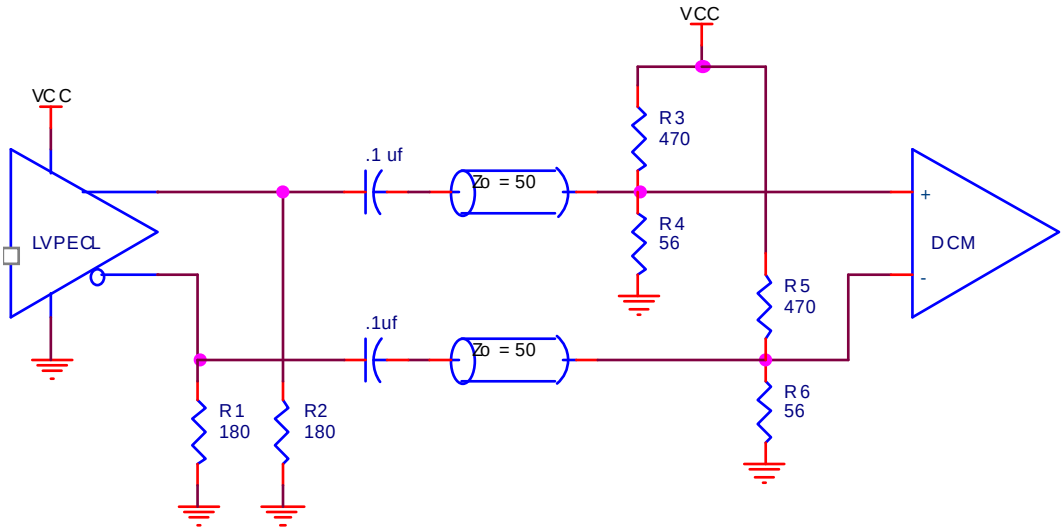


Figure 30. 3.3V LVPECL to Broadcom BCM5785

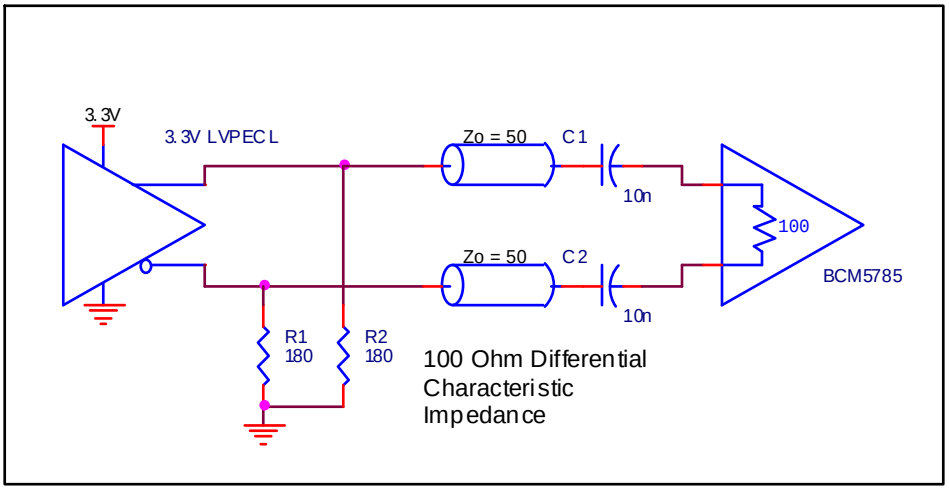


Figure 31. LVPECL to Differential 100ohm DC, 10K Bias

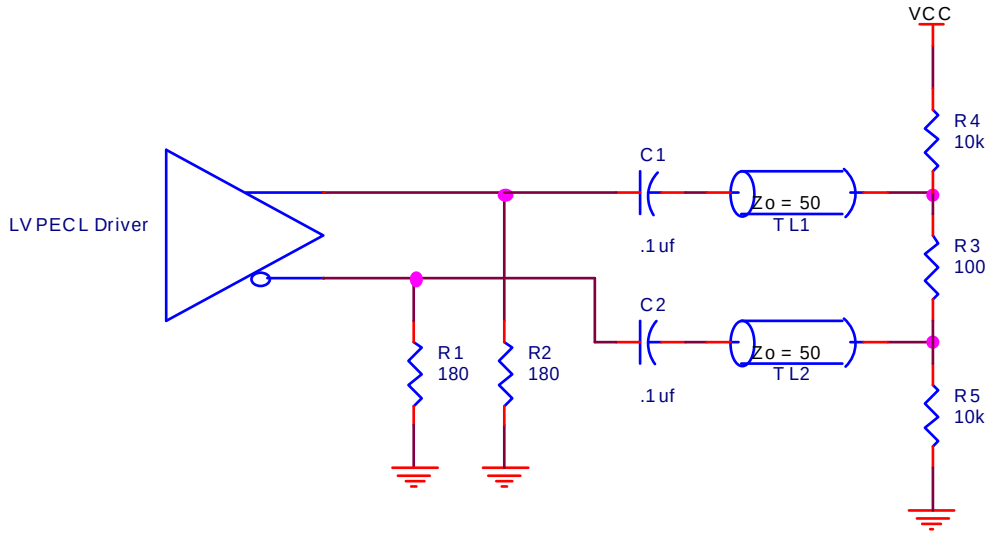


Figure 32. LVPECL to 2.5 LVCMOS

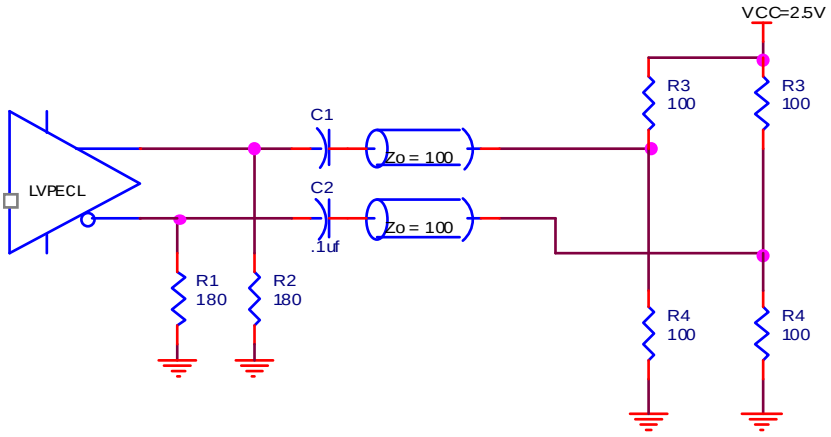


Figure 33. 3.3V LVPECL to 2.5V Different Input with LVDS DC Offset Level Requirement

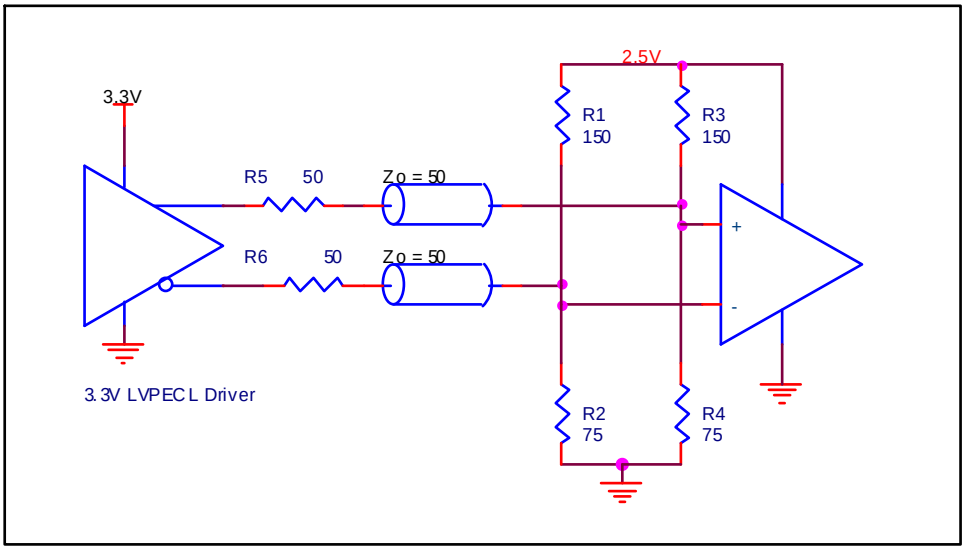


Figure 34. 3.3V LVPECL to PCML, Option 1

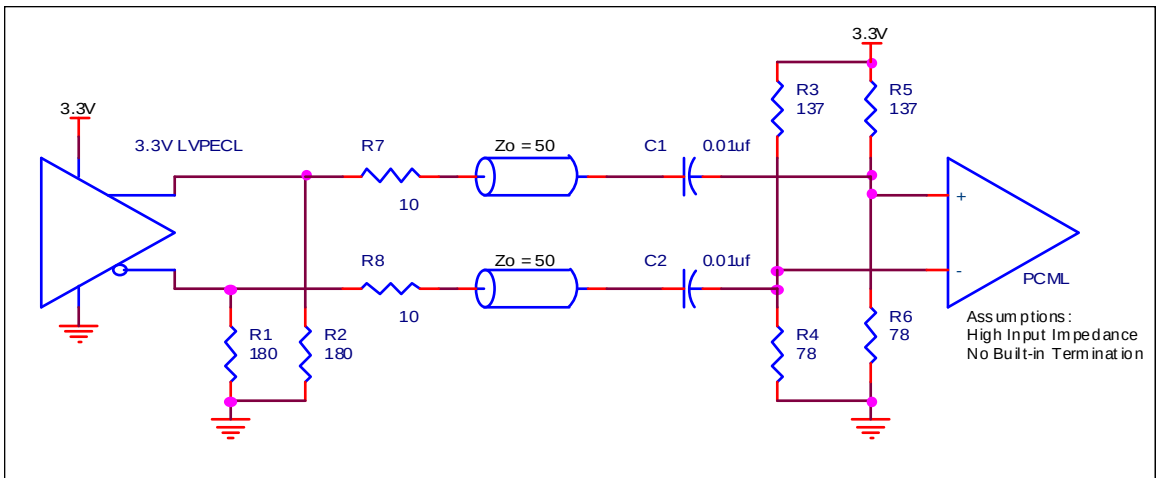


Figure 35. 3.3V LVPECL to PCML, Option 2

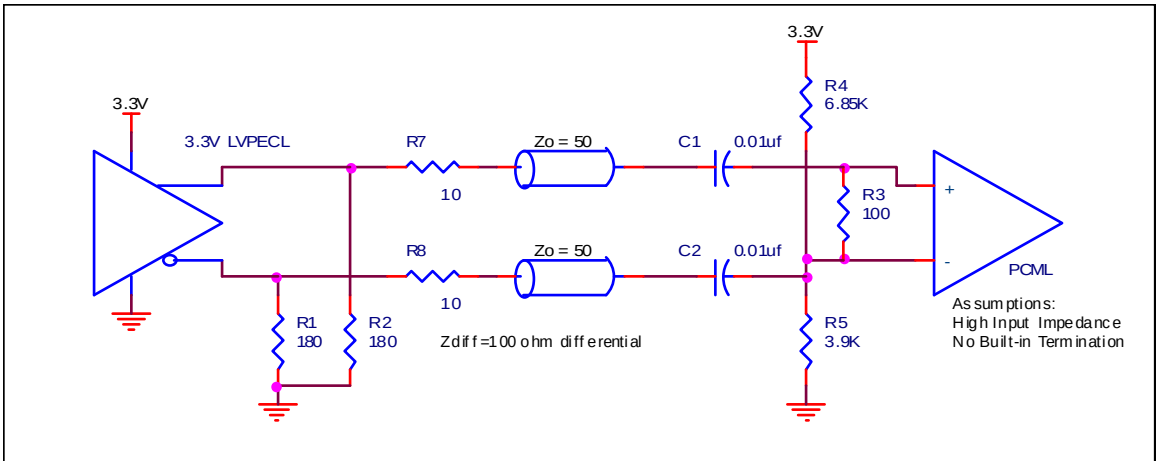


Figure 36. 3.3V LVPECL Driving Receiver with Built-in Termination and Built-in Self Bias

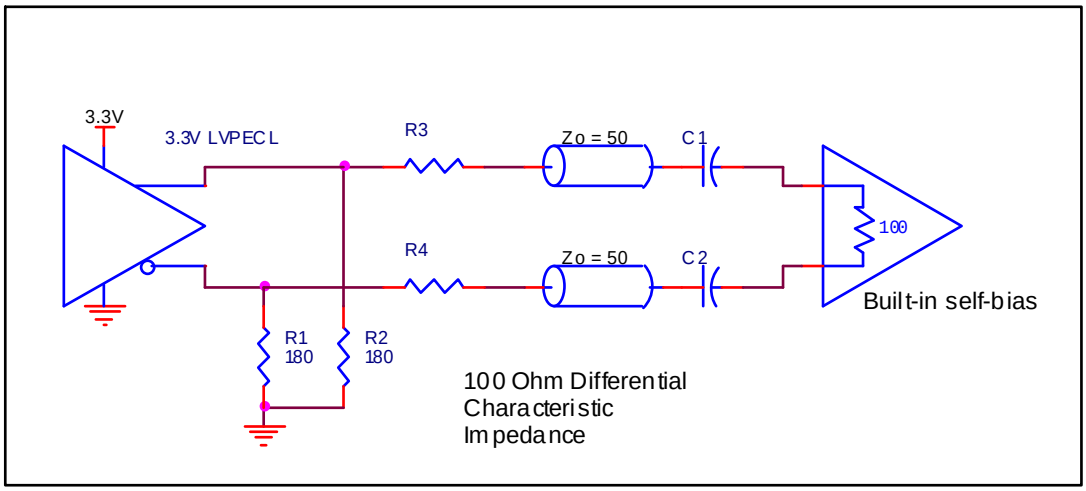


Figure 37. 3.3V LVPECL to HCSL

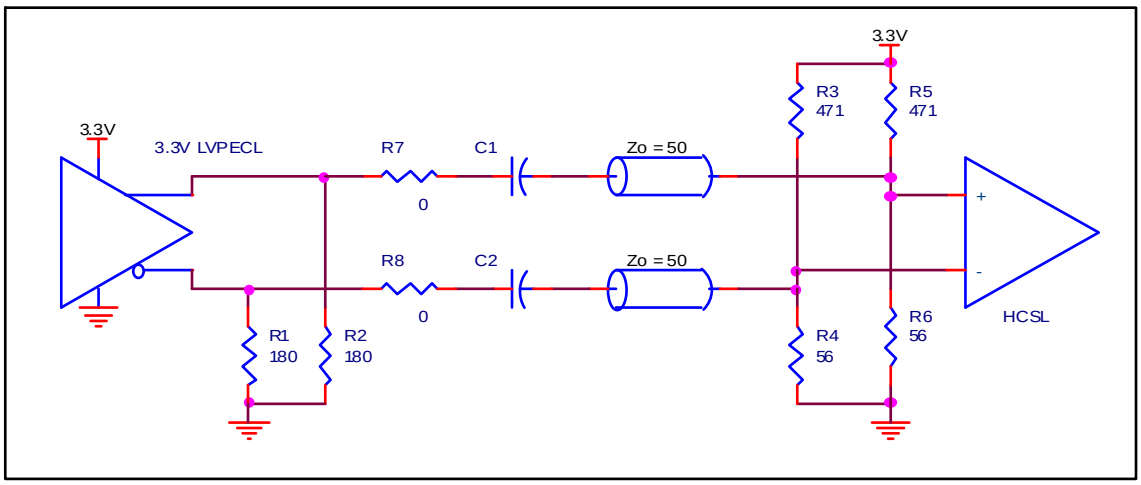


Figure 38. 3.3V LVPECL to 1.8V LVCMOS Interface

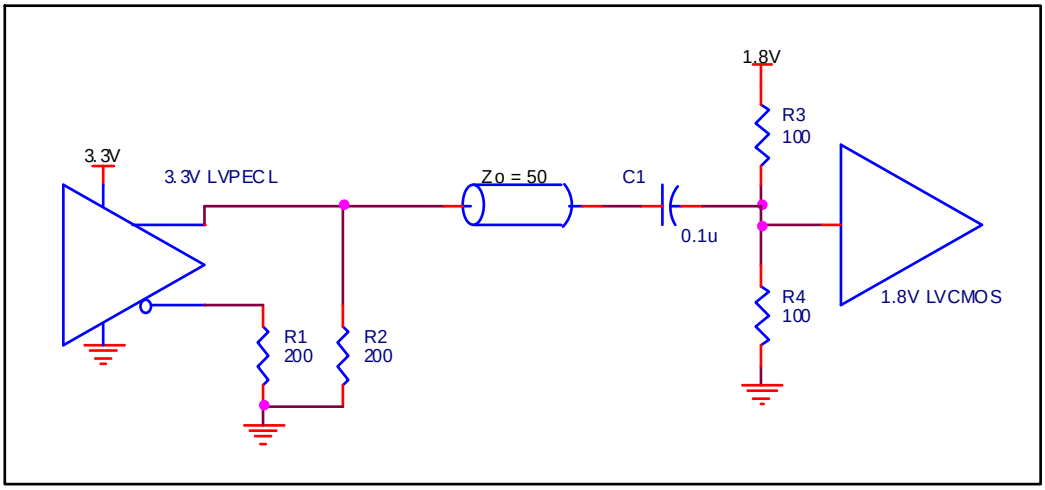


Figure 39. 3.3V LVPECL to 1.8V Differential Interface, Option 1

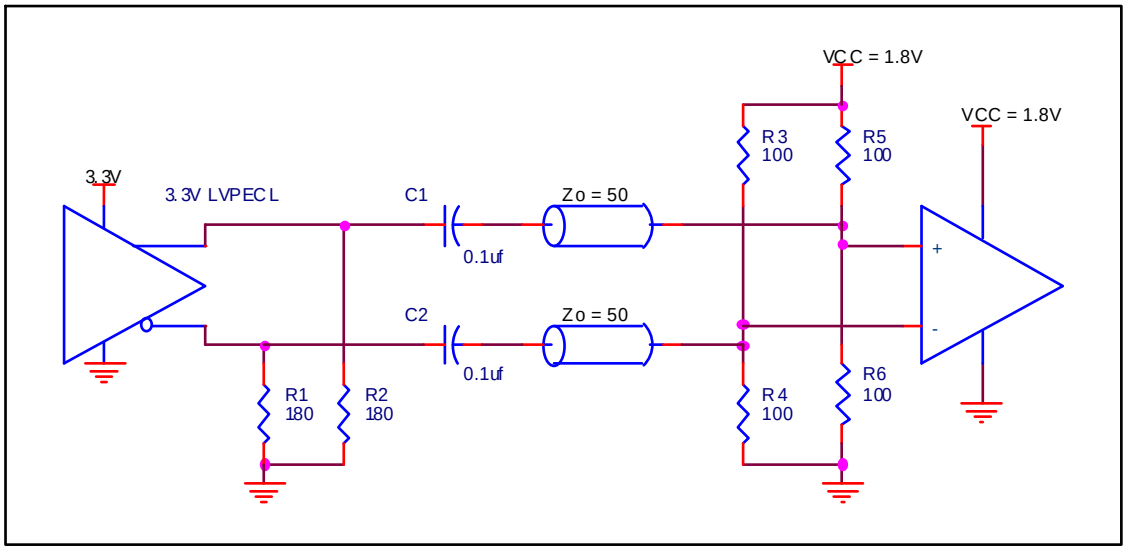


Figure 40. 3.3V LVPECL to 1.8V Differential Interface, Option 2

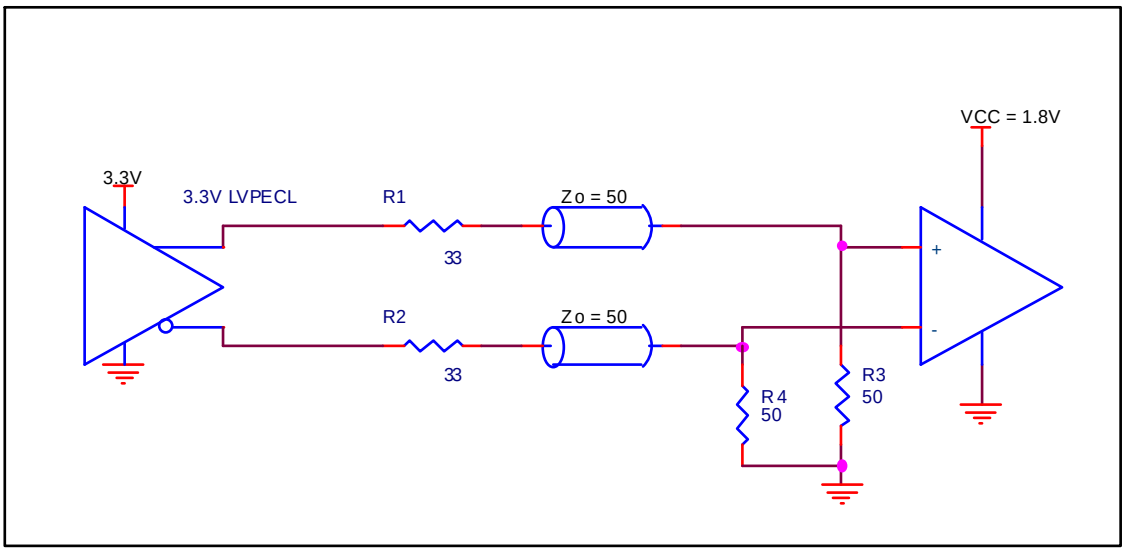


Figure 41. 3.3V LVPECL to 0.65V DC Offset

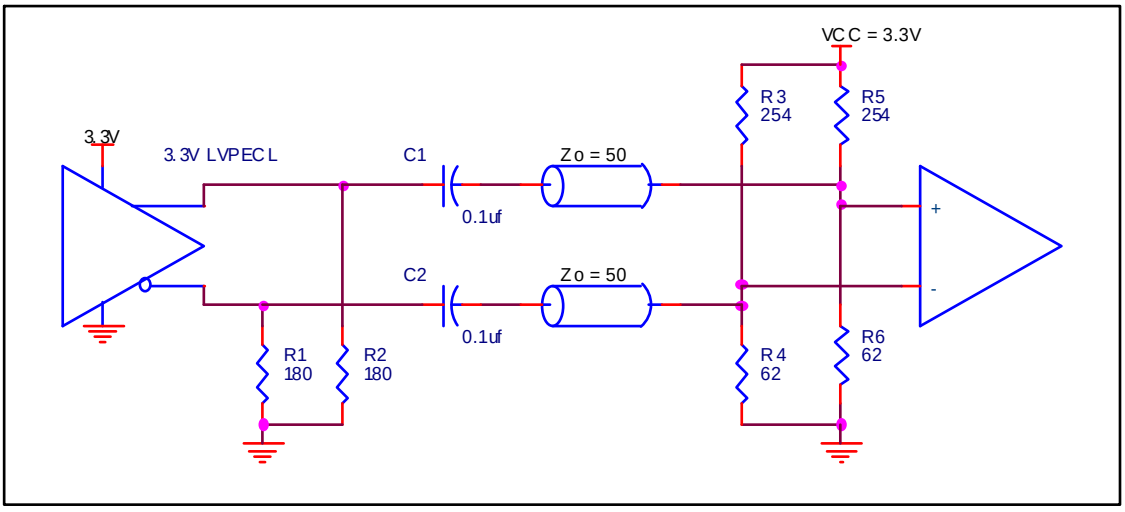


Figure 42. 3.3V LVPECL to CML

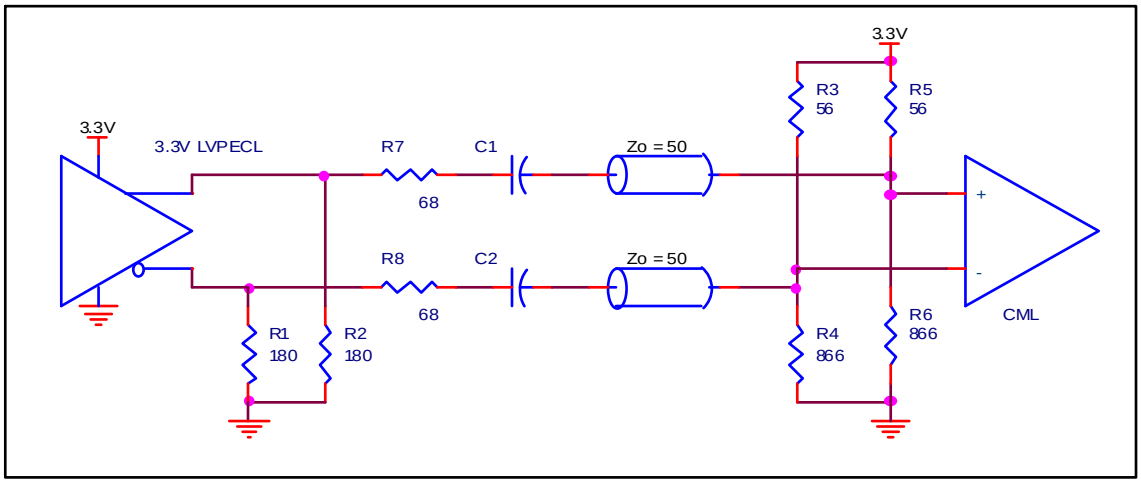


Figure 43. 3.3V LVPECL to 2.5V SSTL 2 Interface with VDD/2 Voltage Source

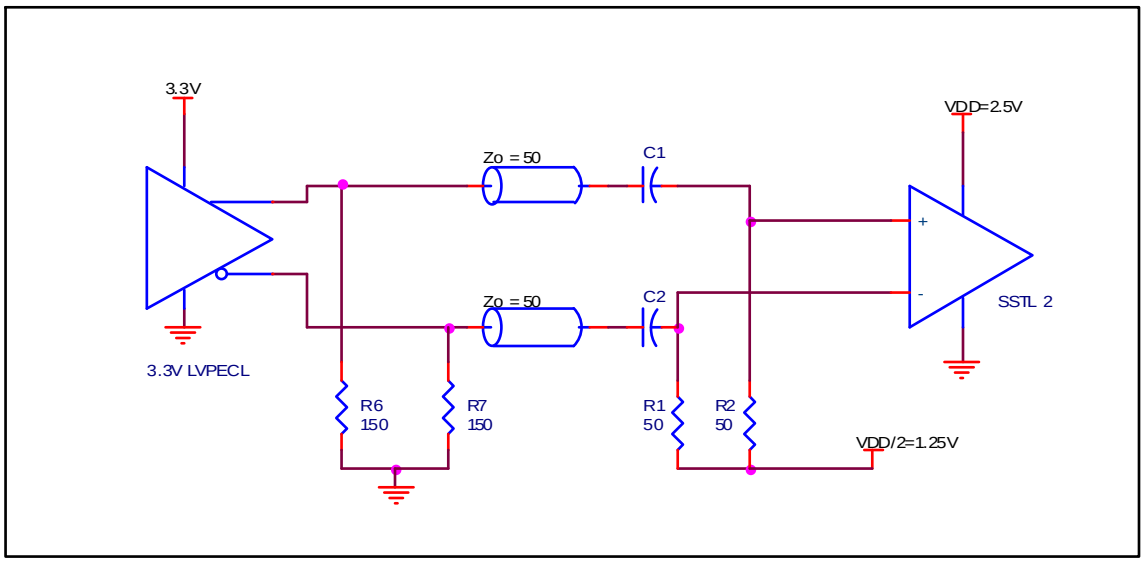


Figure 44. 3.3V LVPECL to 2.5V SSTL 2 Interface without VDD/2 Voltage Source

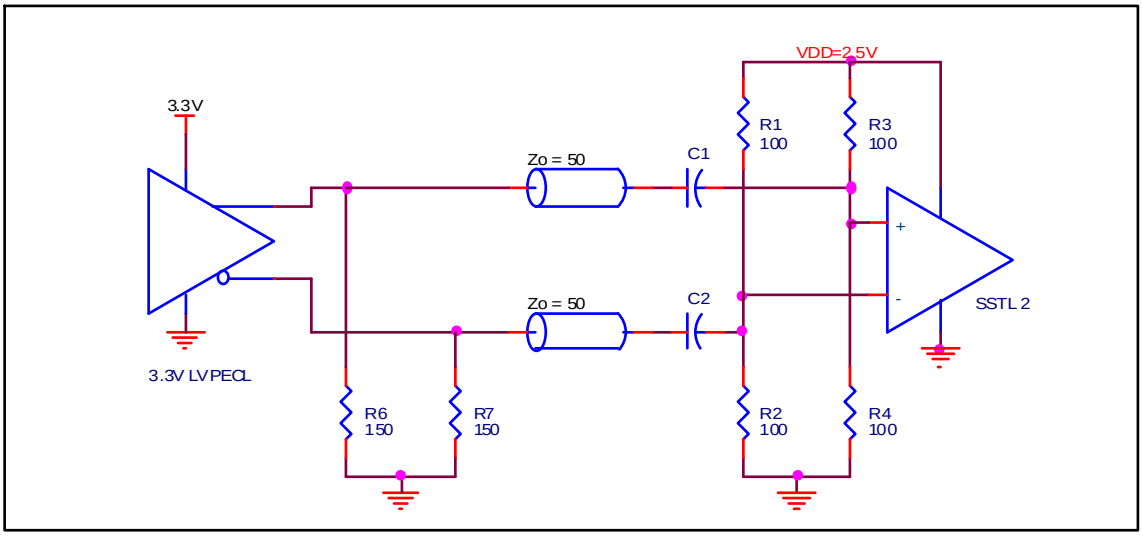


Figure 45. 2.5V LVPECL Standard Termination

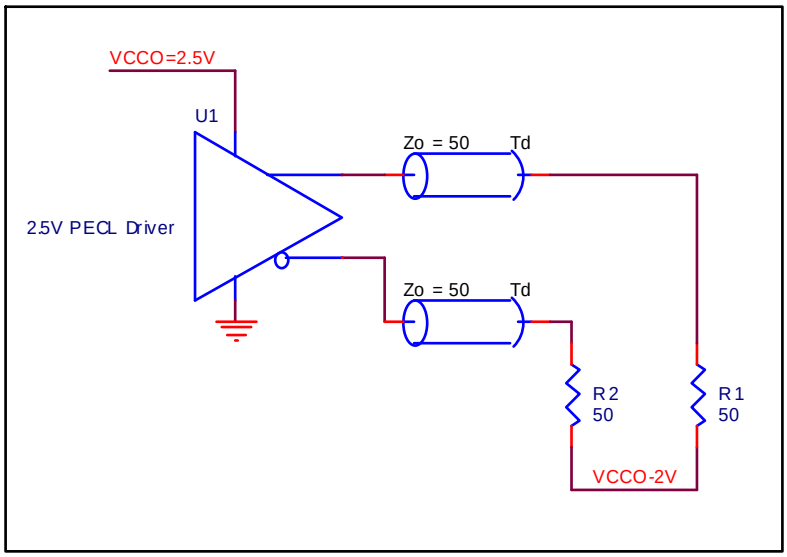


Figure 46. 2.5V LVPECL Equivalent Termination

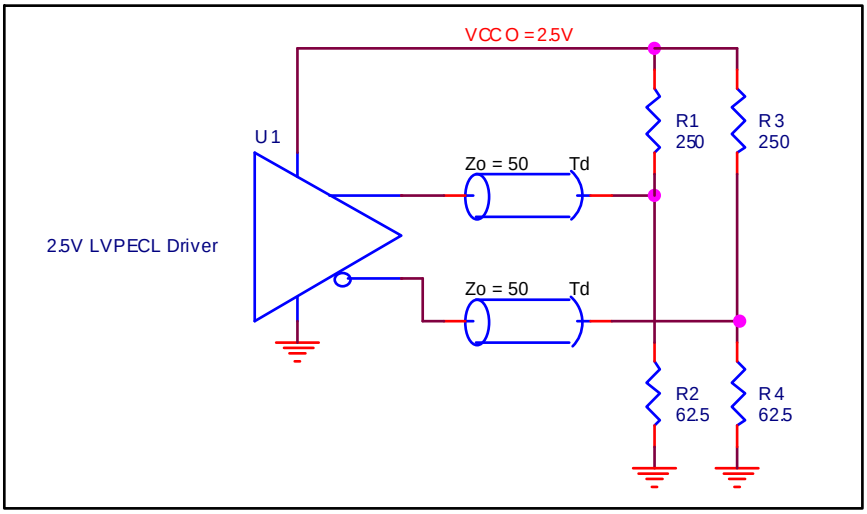


Figure 47. 2.5V LVPECL Equivalent Termination

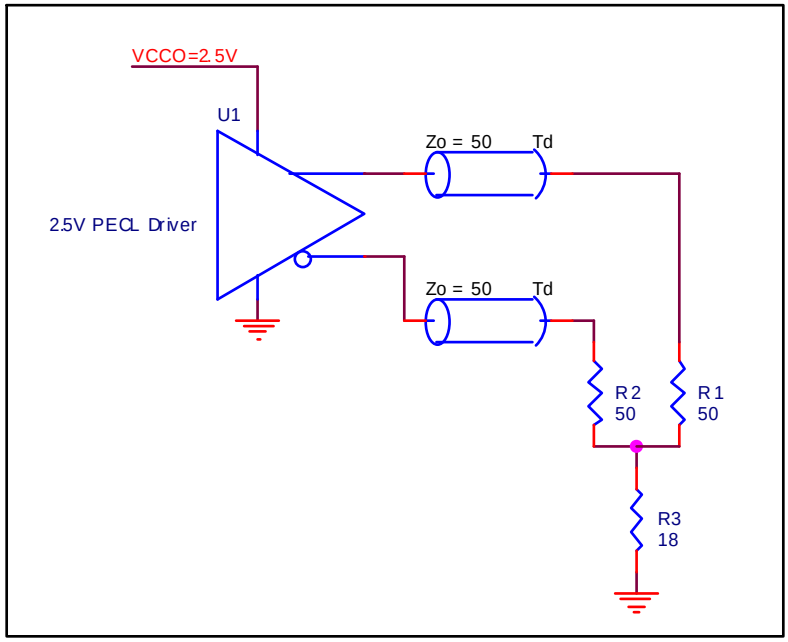


Figure 48. 2.5V LVPECL Termination, No Receiver

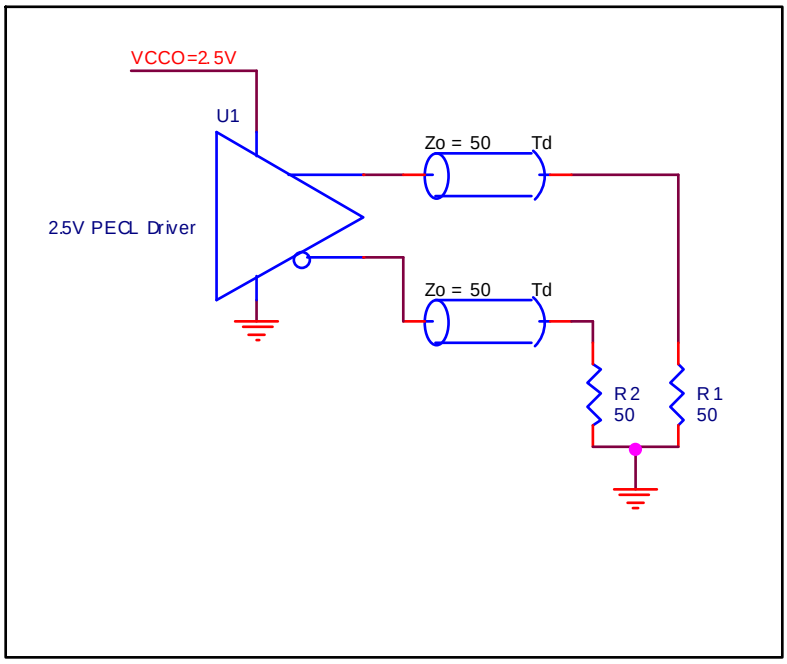


Figure 49. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 1

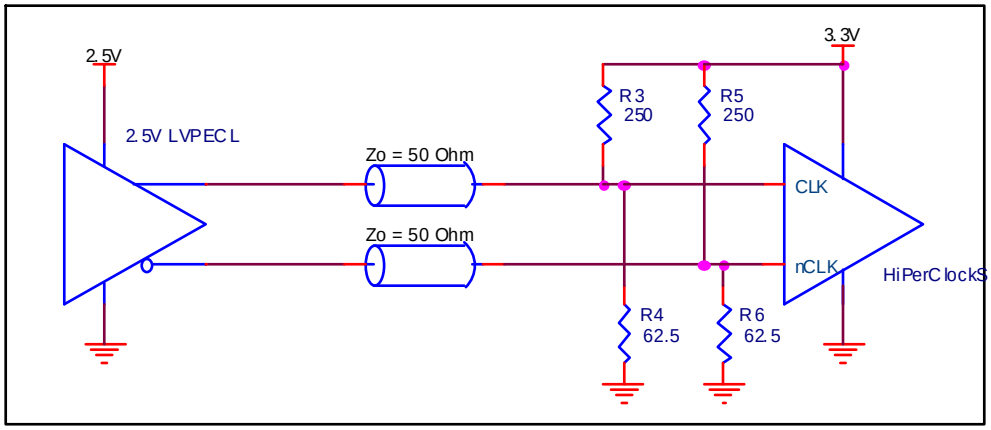


Figure 50. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 2

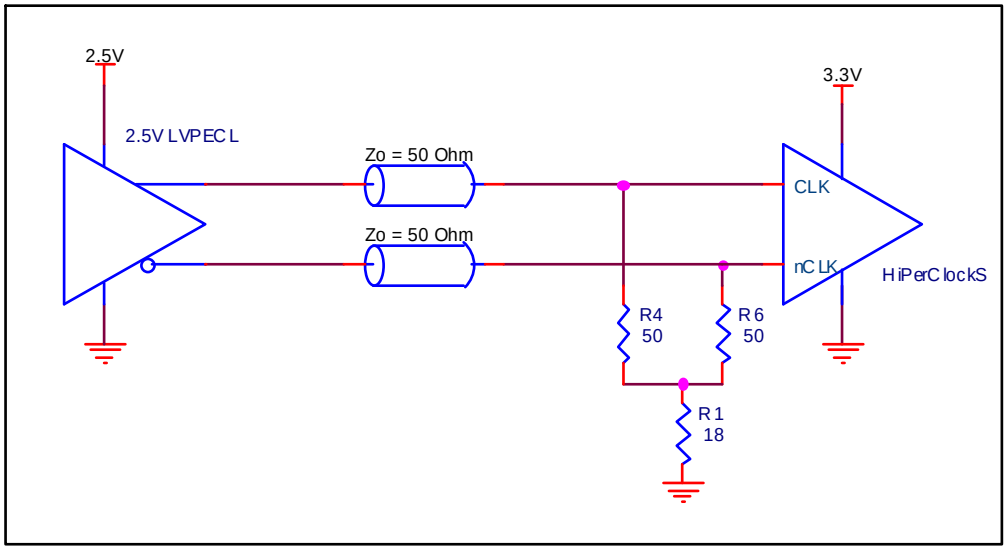


Figure 51. 2.5V LVPECL to Differential Input (CLK/nCLK) Interface, Option 3

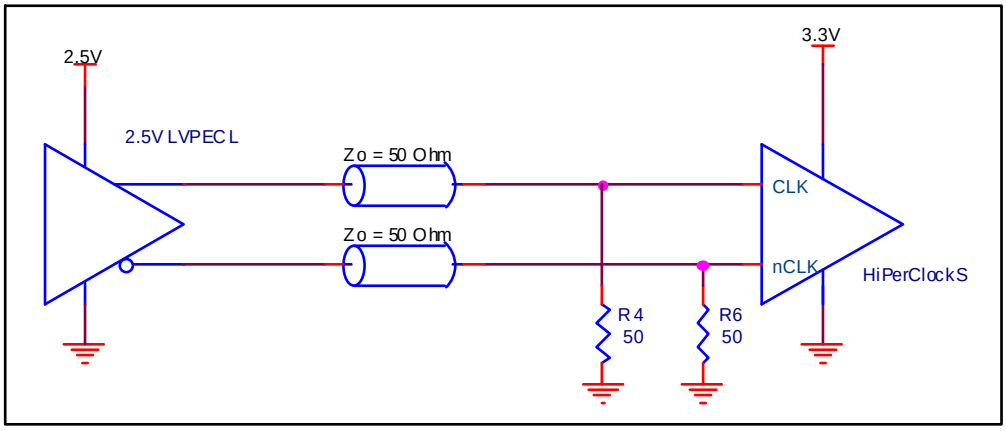


Figure 52. 2.5V LVPECL to 0.8V DC offset Receiver

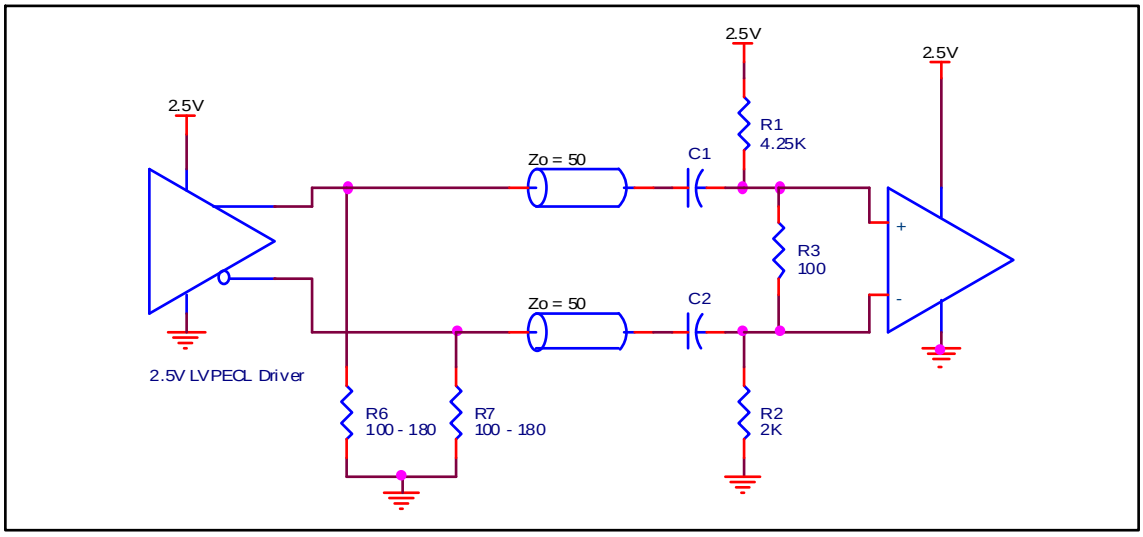


Figure 53. LVPECL, AC-Coupled to Receiver with no DC Offset Requirement

40

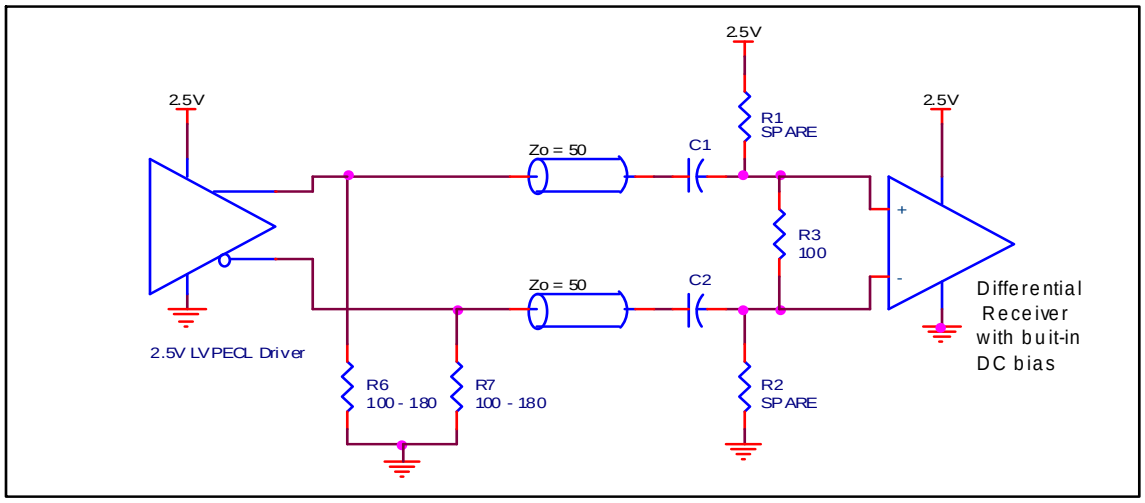


Figure 54. LVPECL to XTAL

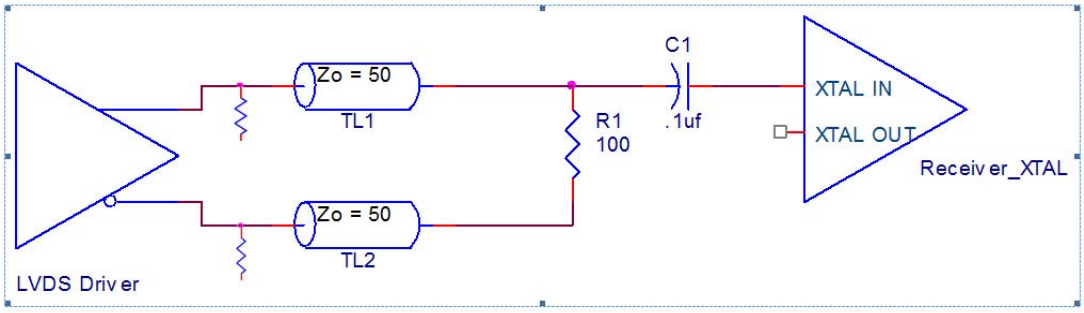


Figure 55. LVPECL Short Trace Termination

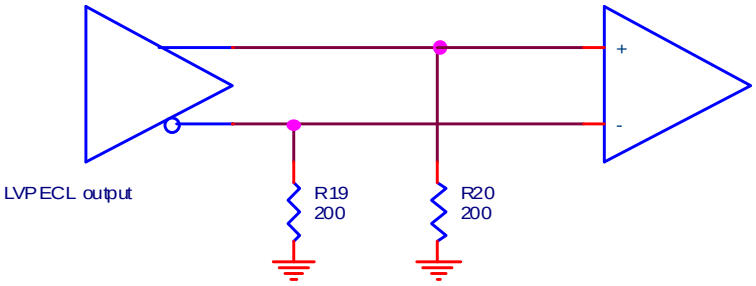


Figure 56. LVPECL to Single-Ended LVPECL, Option 1

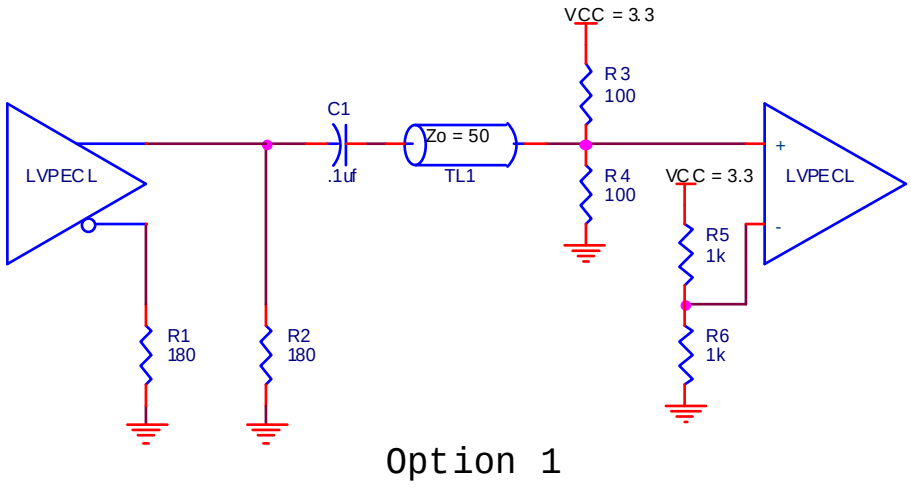


Figure 57. LVPECL to Single-Ended LVPECL, Option 2

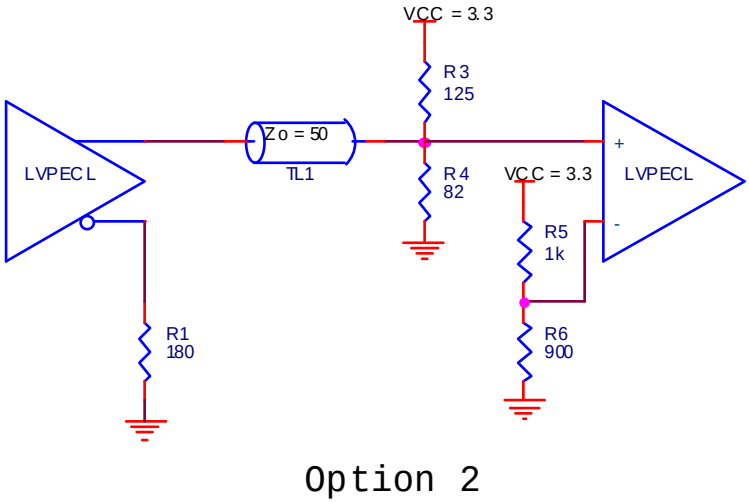
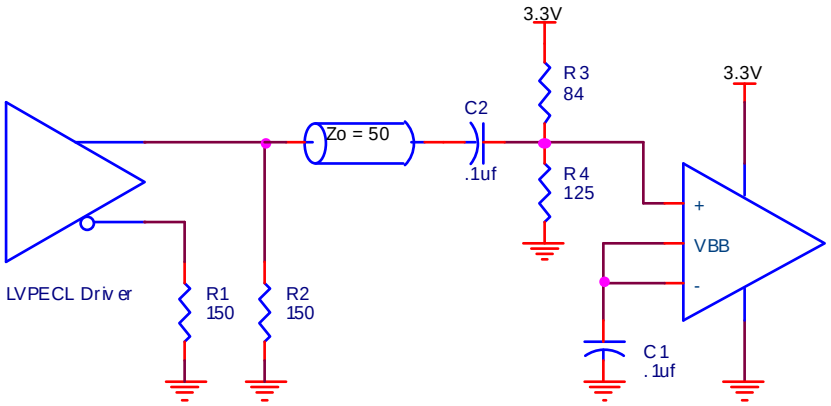


Figure 58. LVPECL to Single-Ended LVPECL with VBB Bias, Option 1



Re-biasing positive side of input to Vcc - 1.3V to match VBB

Figure 59. LVPECL to Single-Ended LVPECL with VBB Bias, Option 2

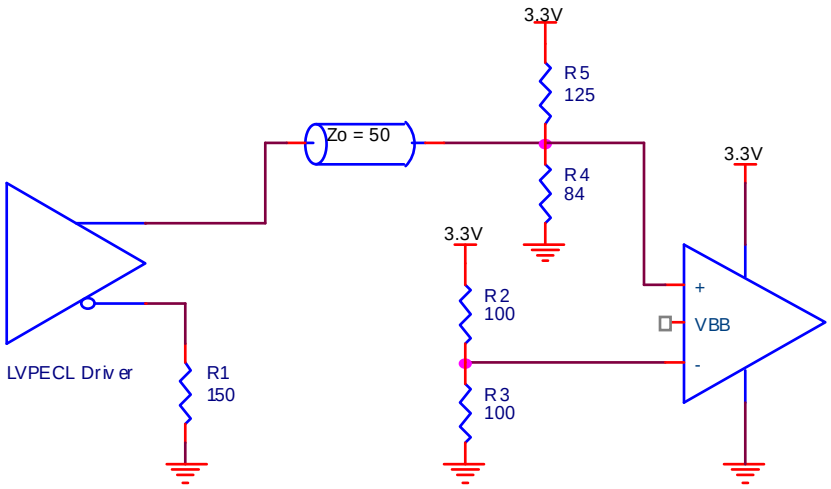


Figure 60. LVPECL to Single-Ended LVPECL with VBB Bias, Option 3

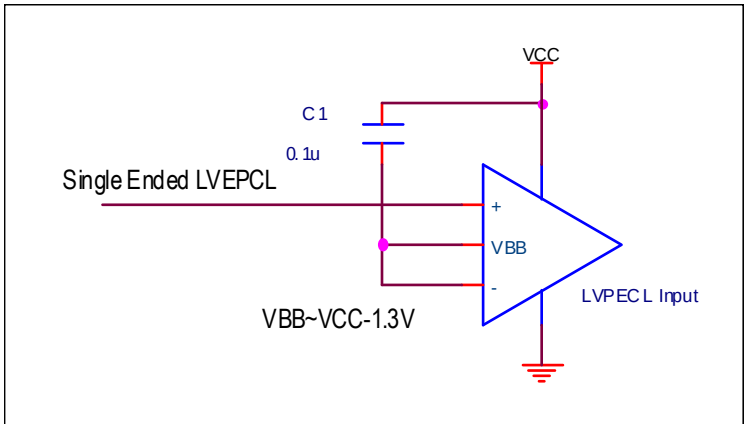
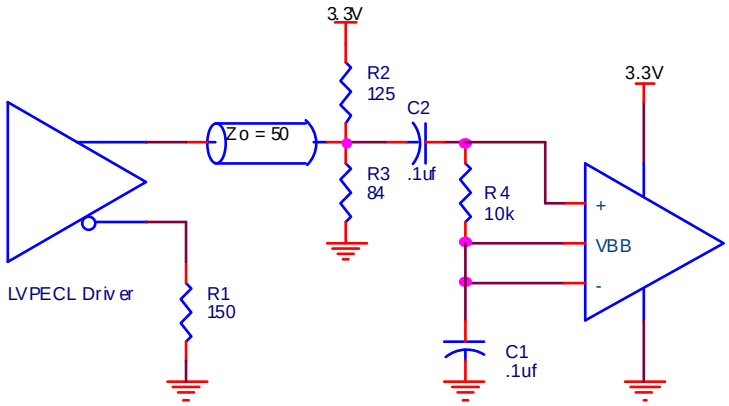


Figure 61. LVPECL to Single-Ended LVPECL with VBB Bias, Option 4



Re-biasing both sides of the input using VBB.

Figure 62. LVPECL to HCSL (DCM)

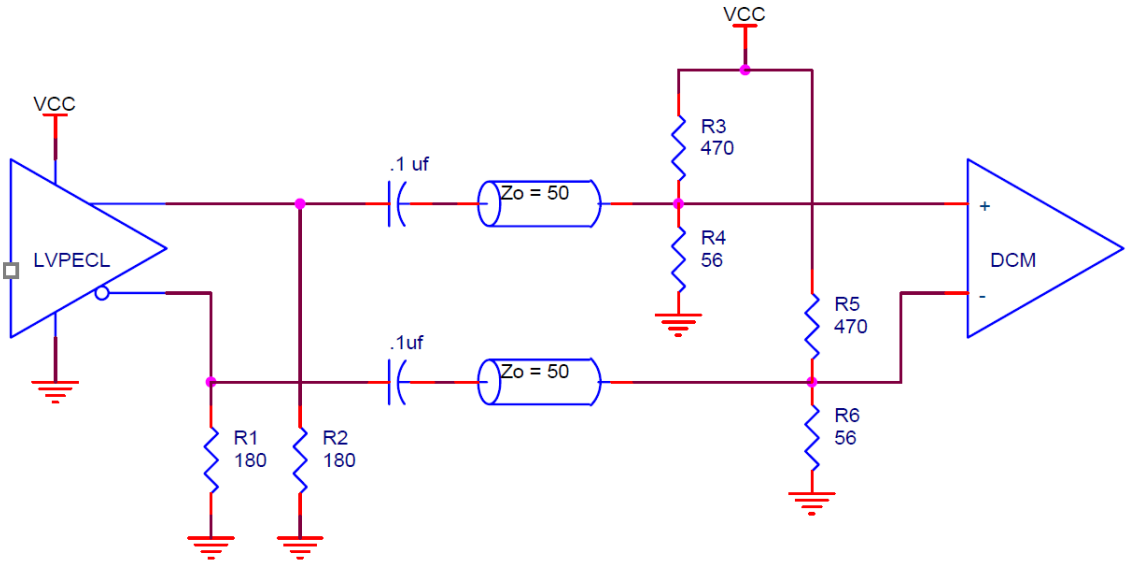


Figure 63. LVPECL Drives Two Receivers

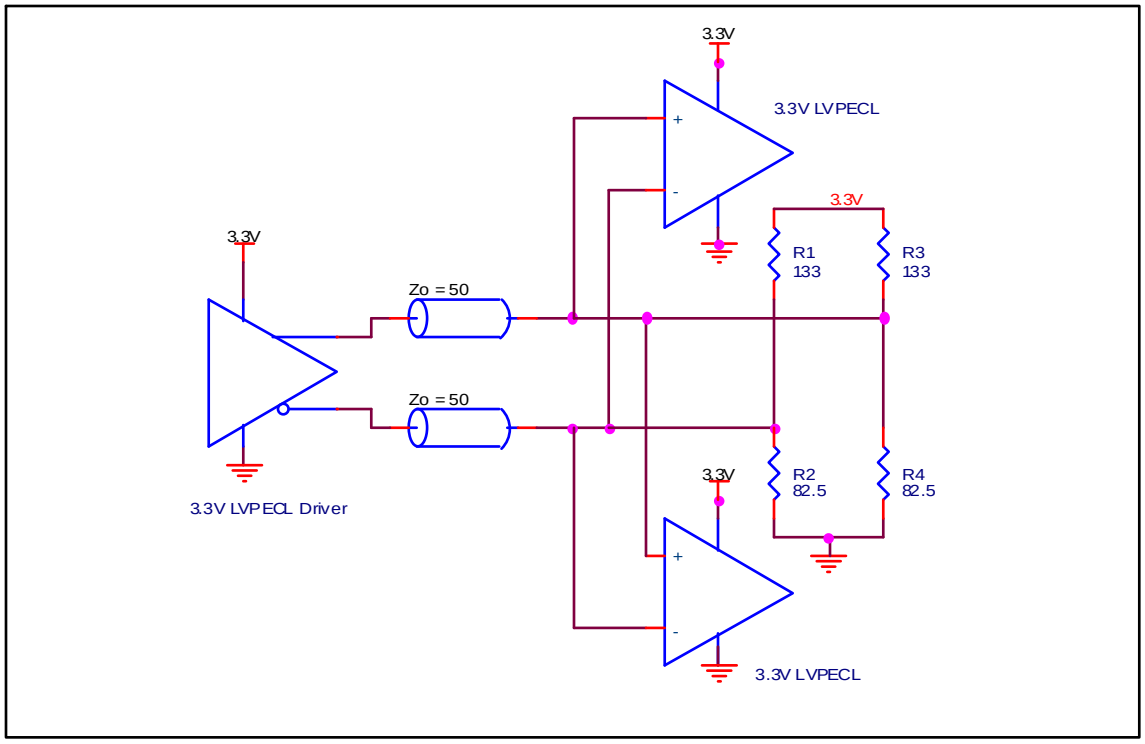


Figure 64. 3.3V LVPECL to AMD8132

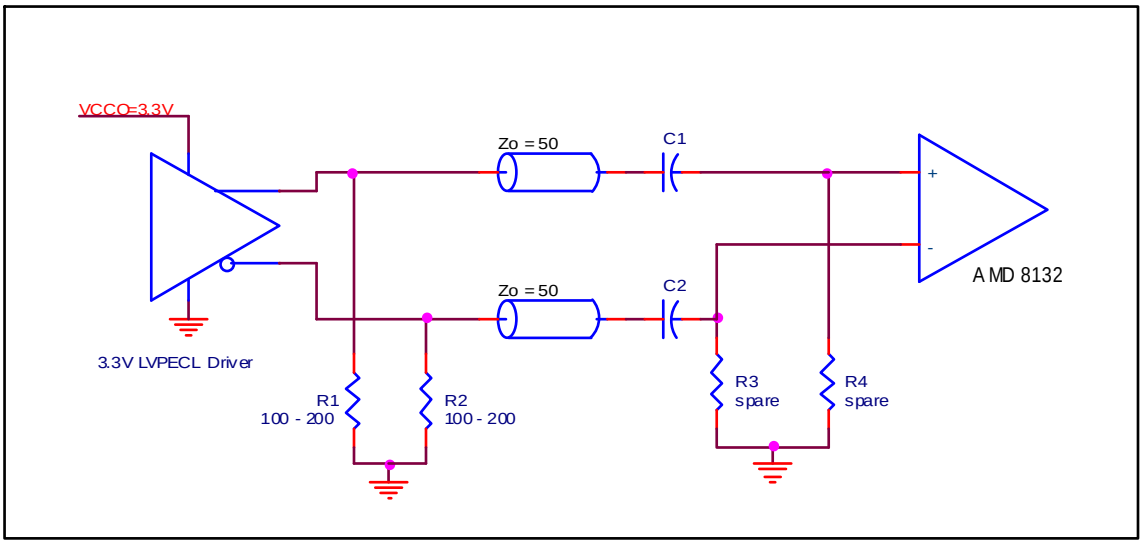


Figure 65. 2.5V LVPEC to AMD8132

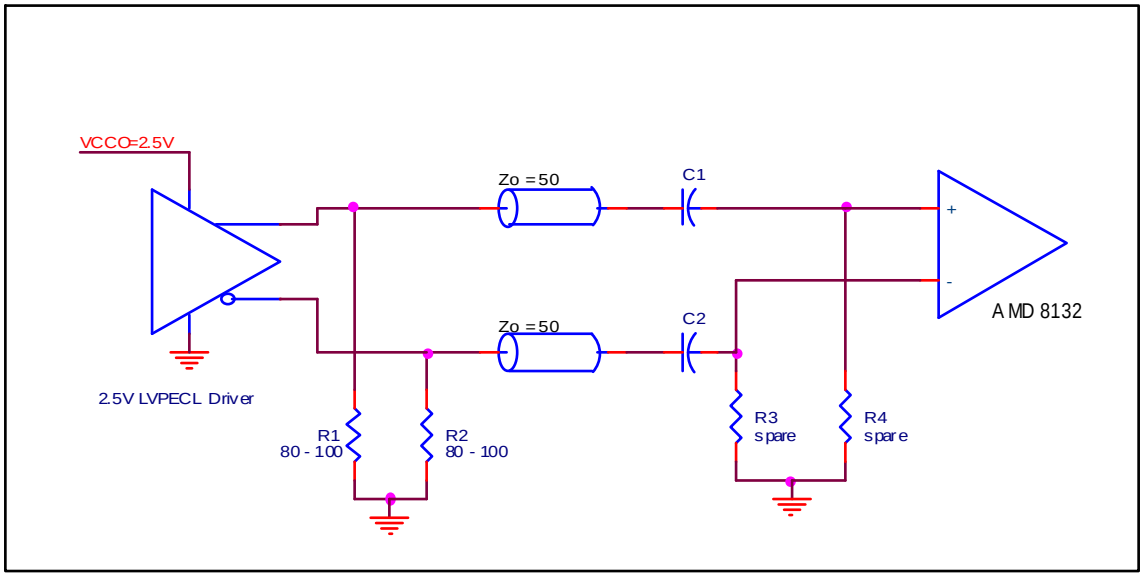


Figure 66. 3.3V LVPECL to AMD K8 CPU CLK Input

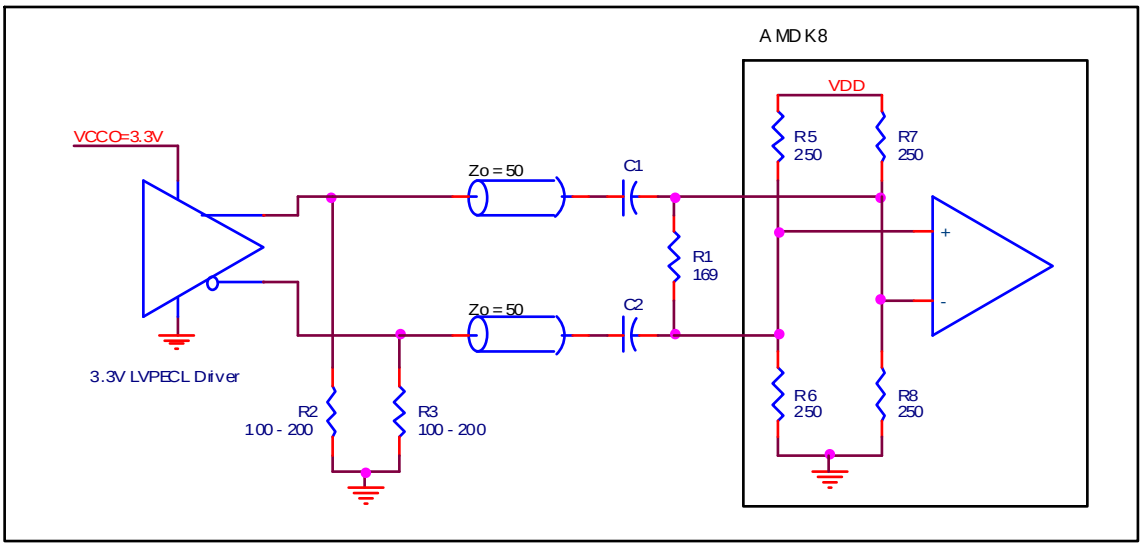
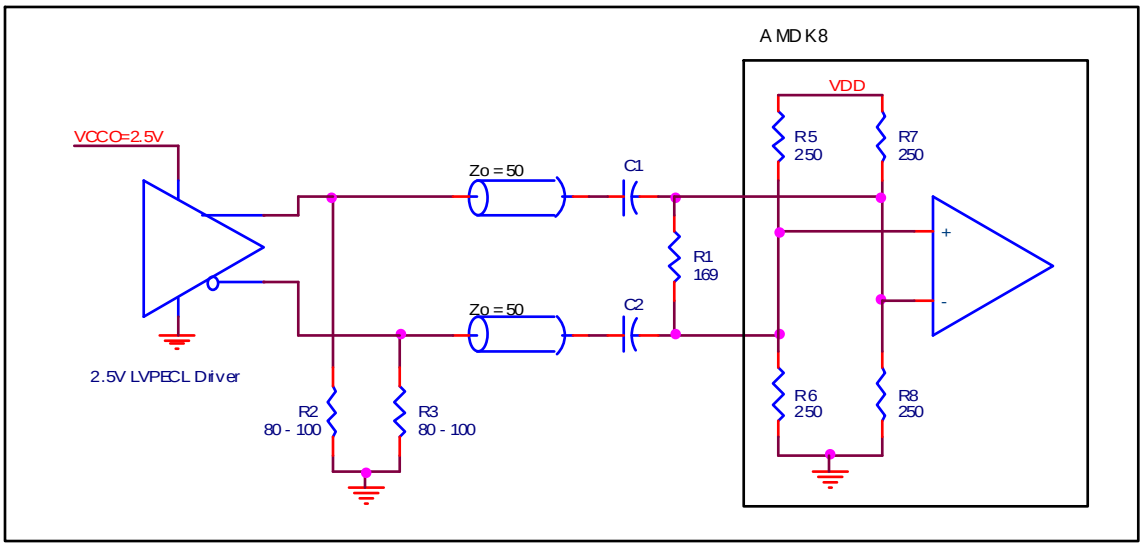


Figure 67. 2.5V LVPECL to AMD K8 CPU CLK Input



LVDS Terminations

Figure 68. LVDS Termination

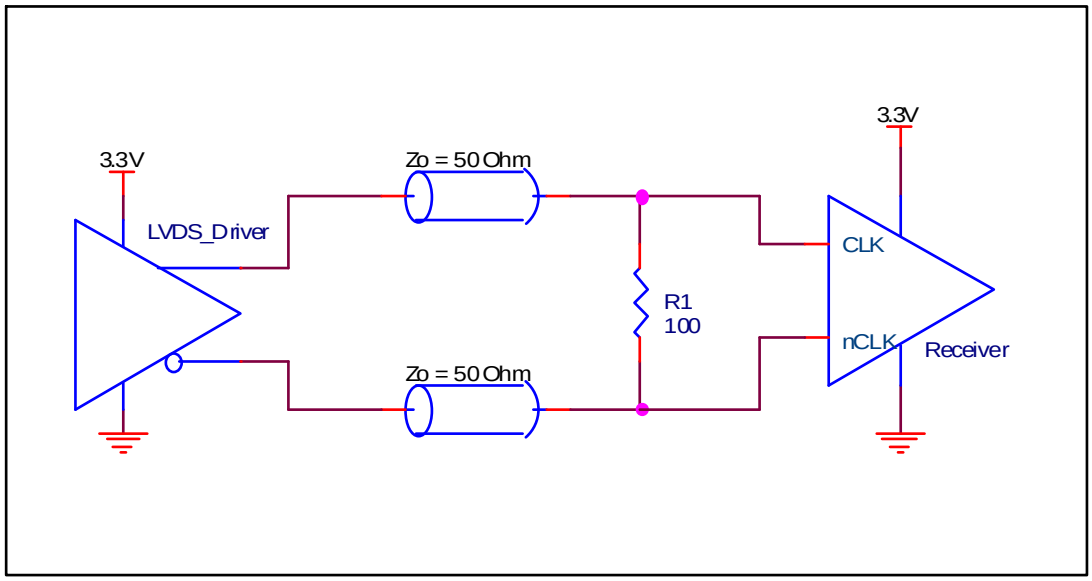


Figure 69. LVDS AC-Coupling, Option 1

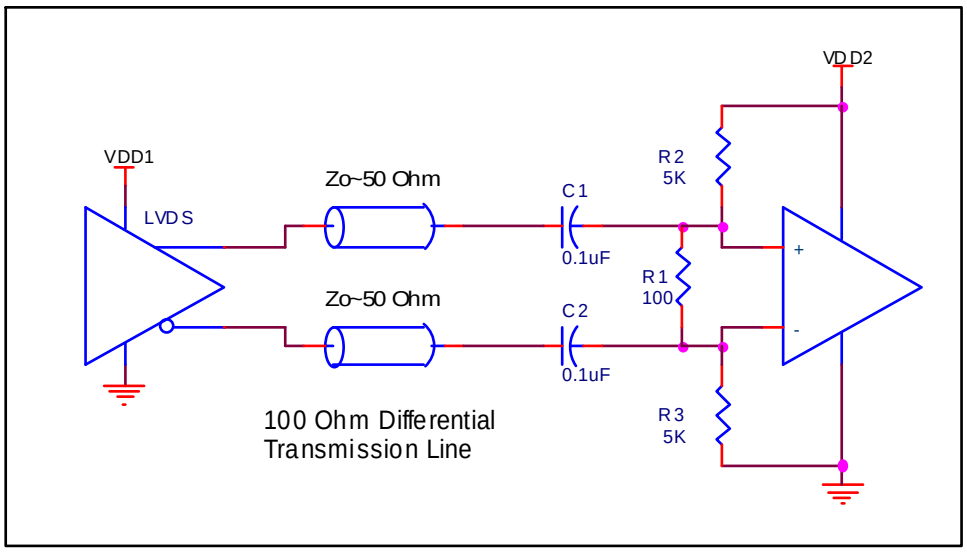


Figure 70. LVDS AC-Coupling, Option 2

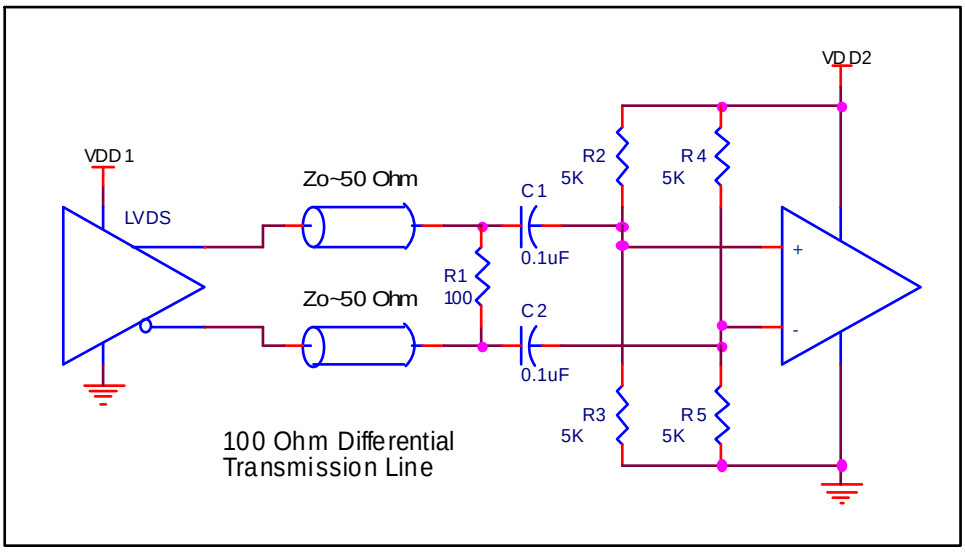


Figure 71. 3.3V LVDS to 2.5 LVDS

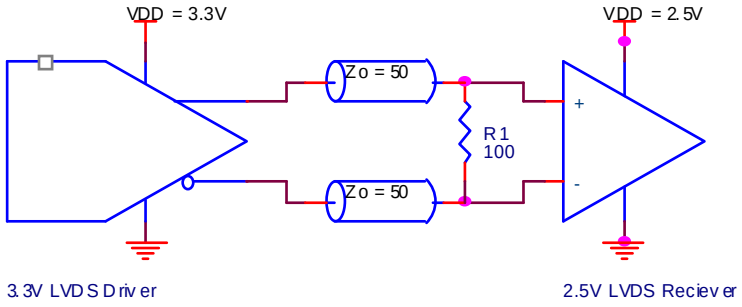


Figure 72. LVDS to CML

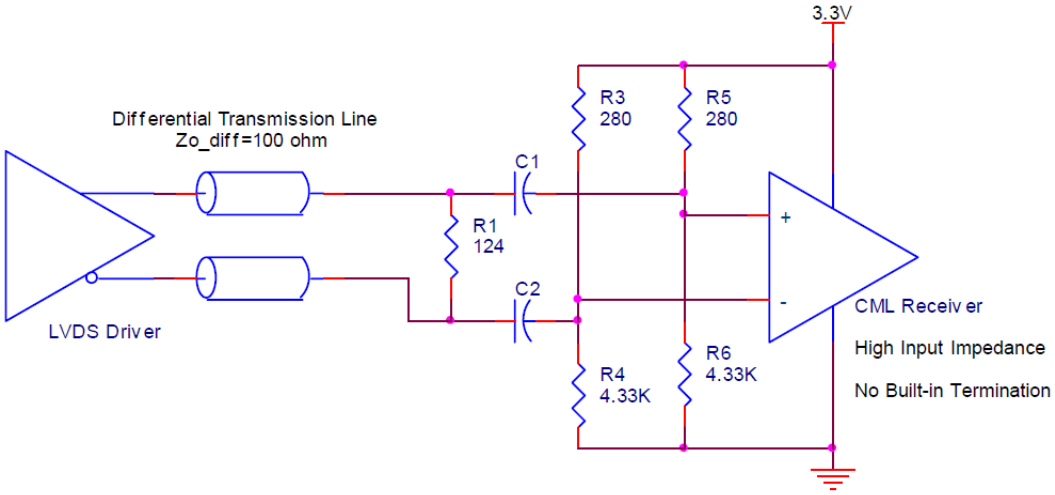


Figure 73. LVDS AC-Coupled to Built-In Termination

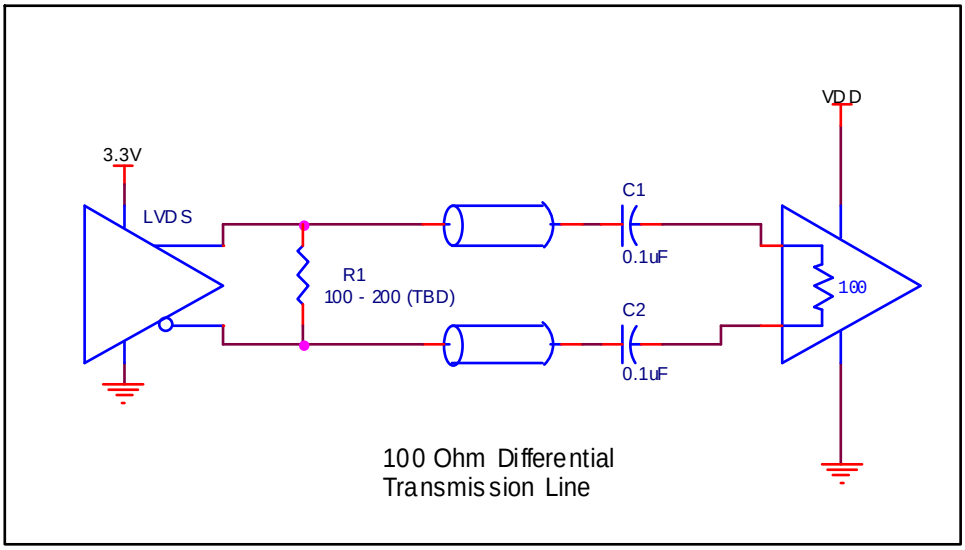
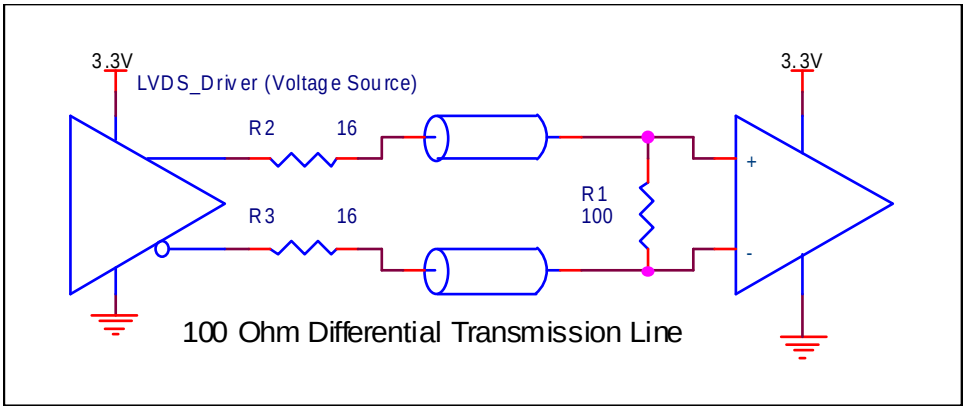
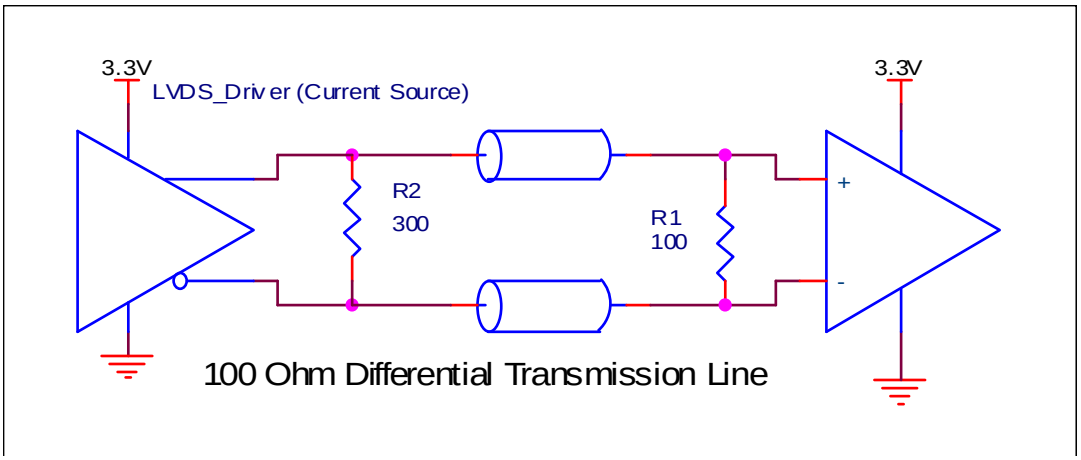


Figure 74. LVDS (Voltage Source) Amplitude Reduction



Increasing R2/R3 reduces the amplitude.

Figure 75. LVDS (Current Source) Amplitude Reduction



Increasing R2 reduces the amplitude.

Figure 76. LVDS (Current Source) to 1.5V VOS

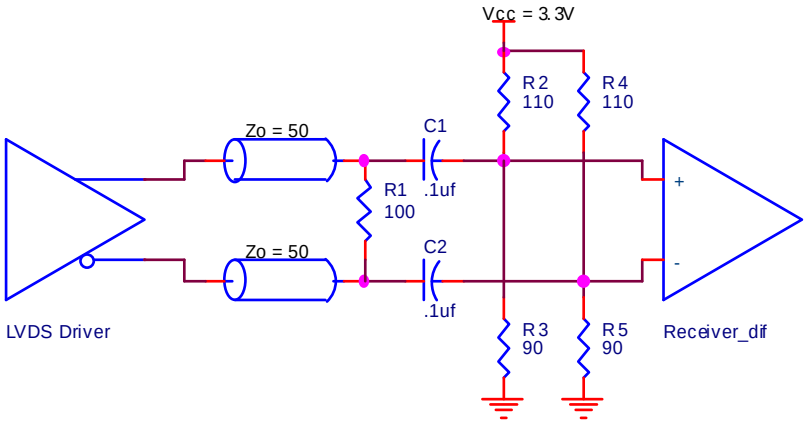


Figure 77. LVDS to 0.6V DC Offset, Option 1

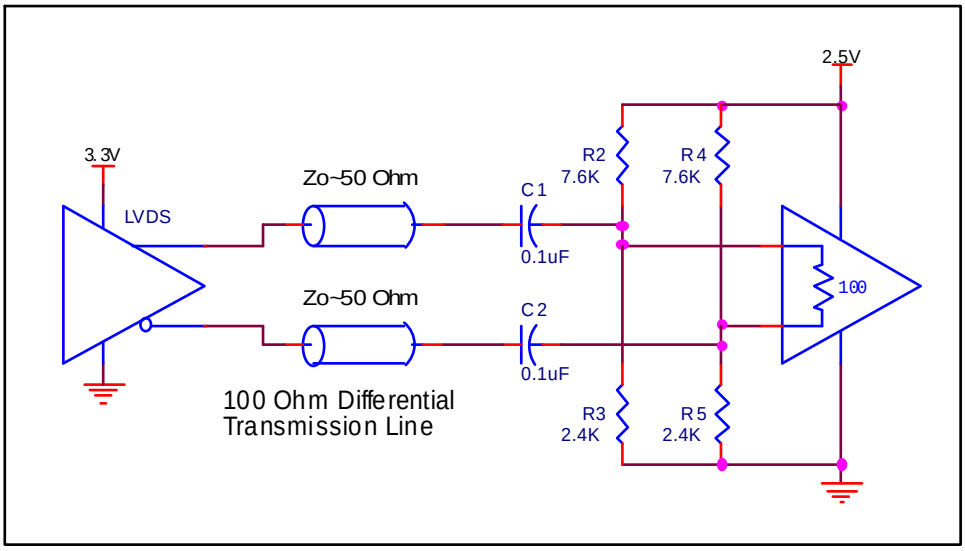


Figure 78. LVDS to 0.6V DC Offset, Option 2

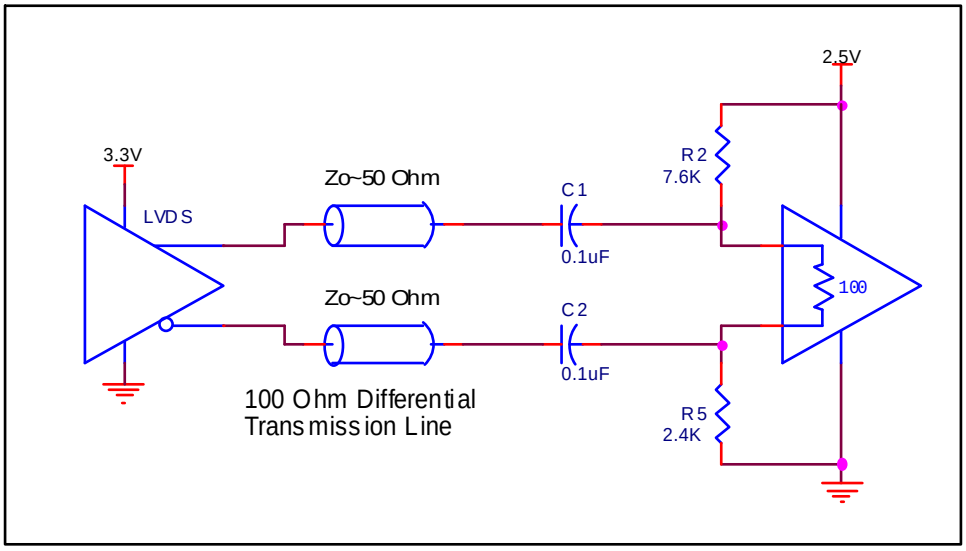


Figure 79. LVDS to XTAL

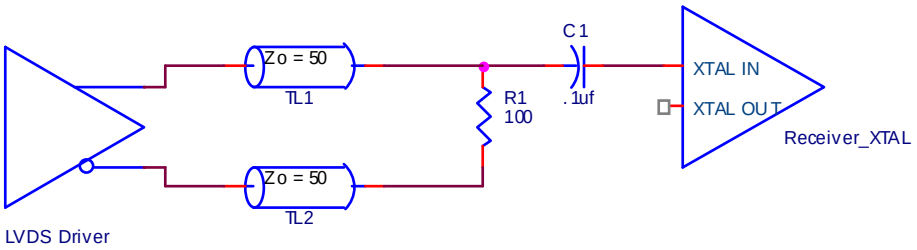


Figure 80. LVDS to IDT PES24T6G2 HCSL Input Interface

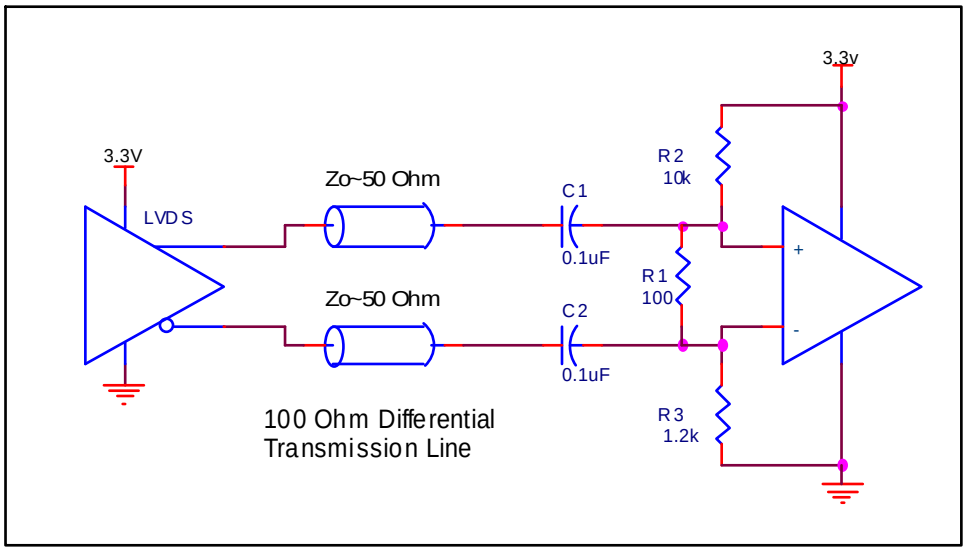


Figure 81. LVDS to PCML

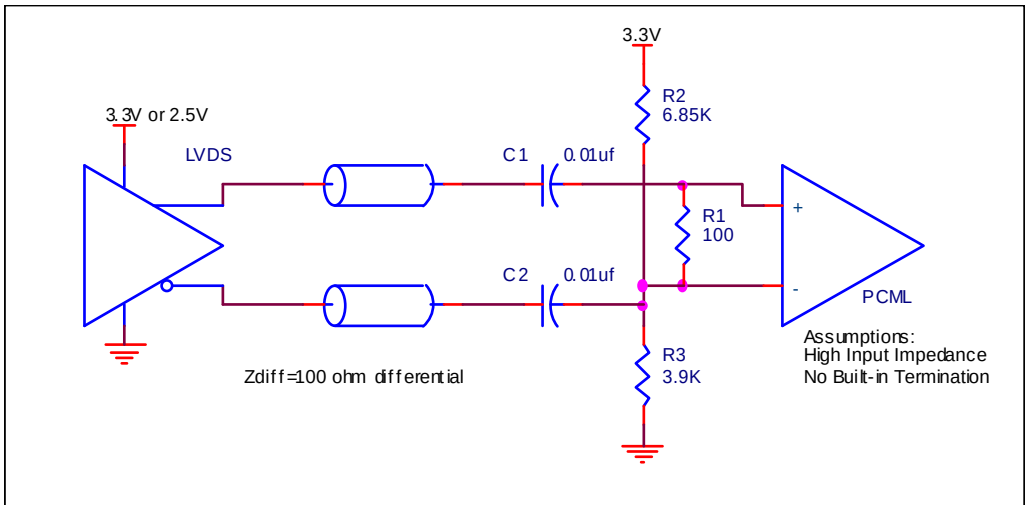


Figure 82. LVDS Differential Duty Cycle Improvement

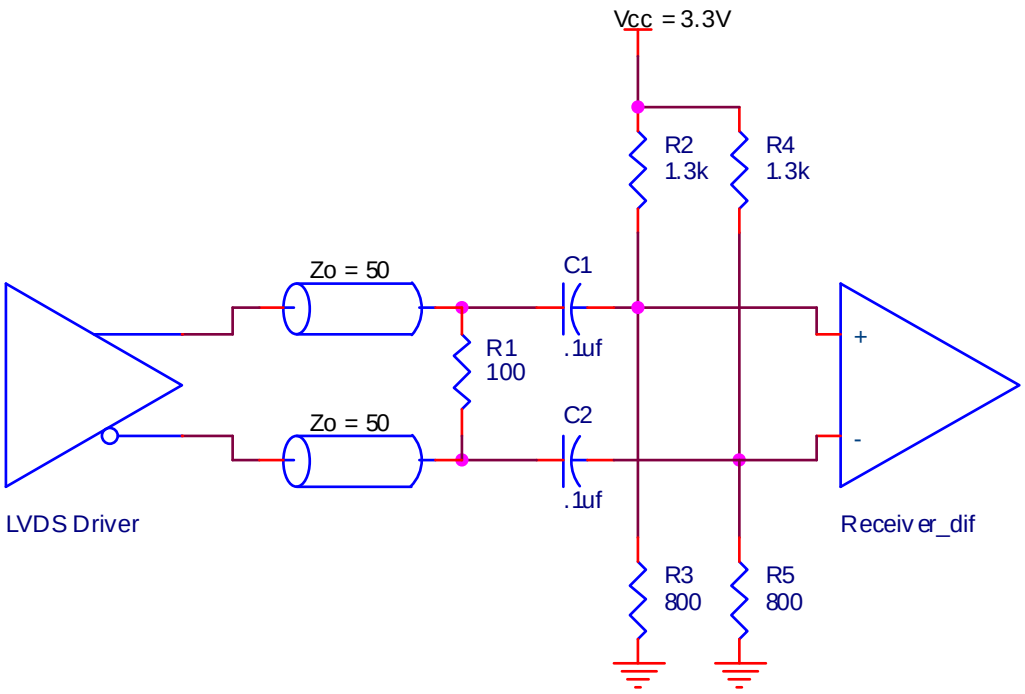
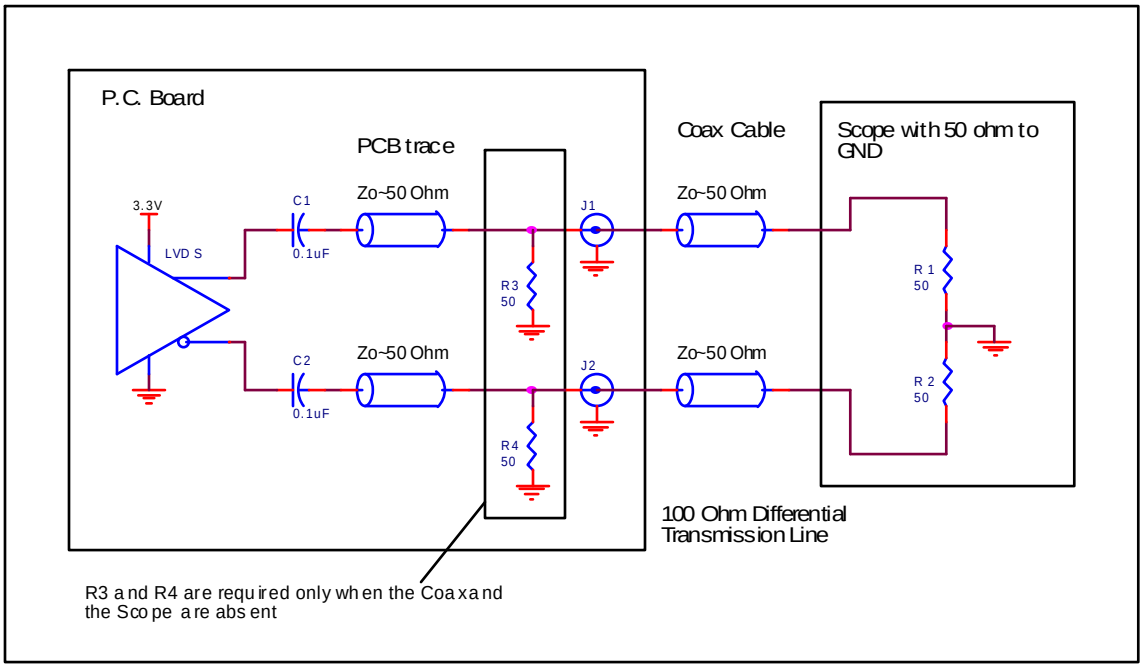


Figure 83. LVDS to 50-ohm Scope, Non-Floating Supply



HSTL Terminations

Figure 84. HSTL Standard Termination

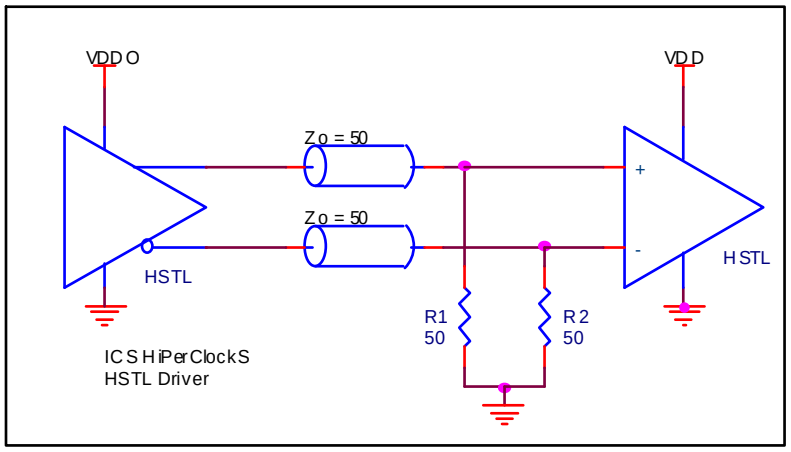


Figure 85. HSTL to 3.3V LVPECL

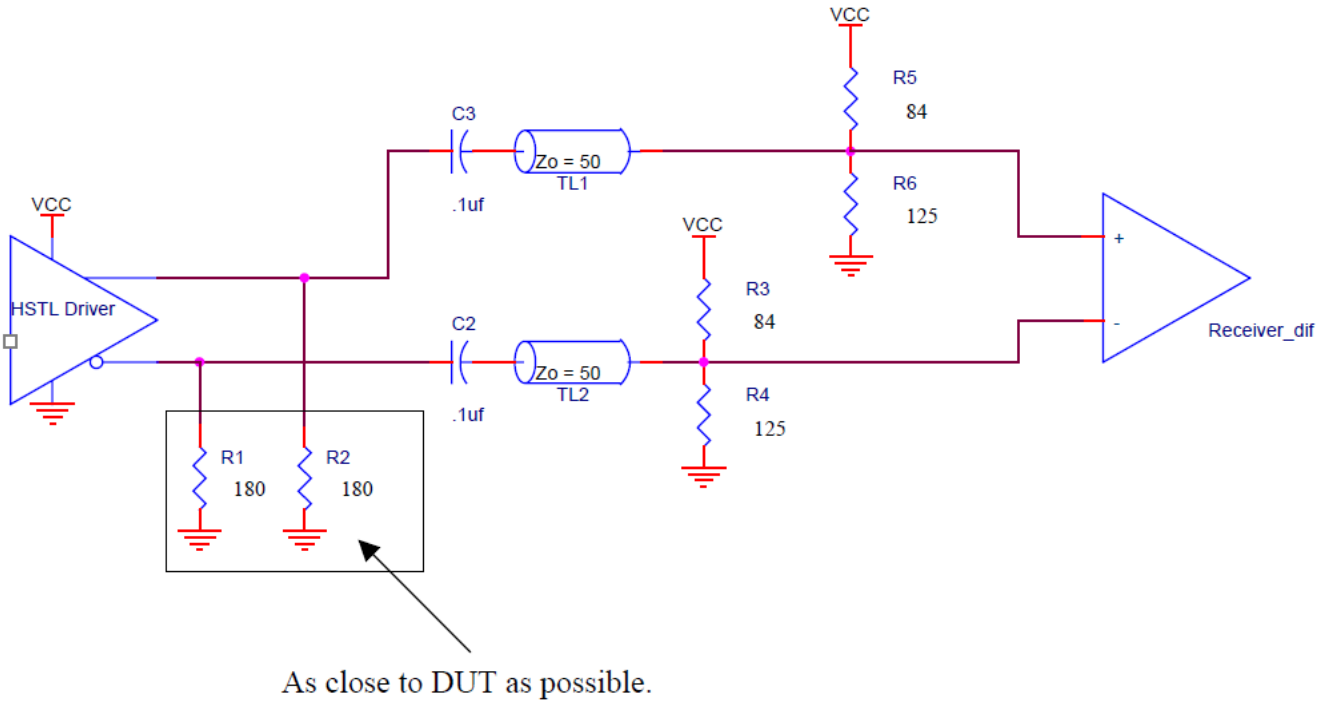


Figure 86. HSTL to Xilinx Spartan 1.8V HSTL II , Option 1

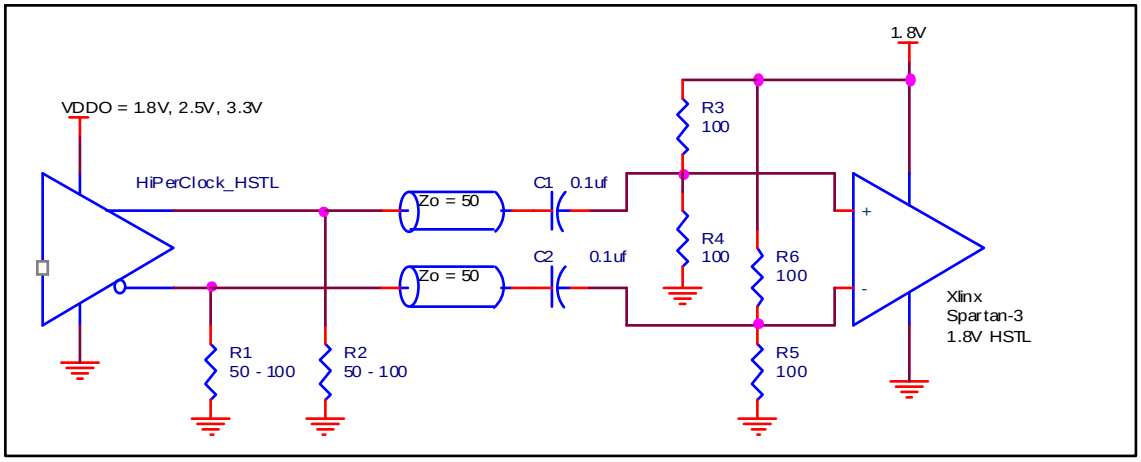


Figure 87. HSTL to Xilinx Spartan 1.8V HSTL II, Option 2

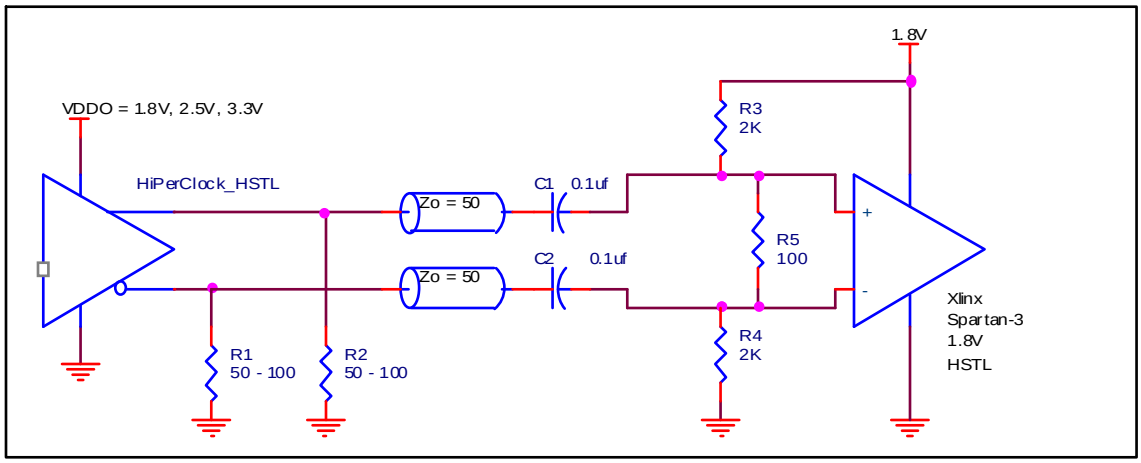


Figure 88. HSTL to LVDS

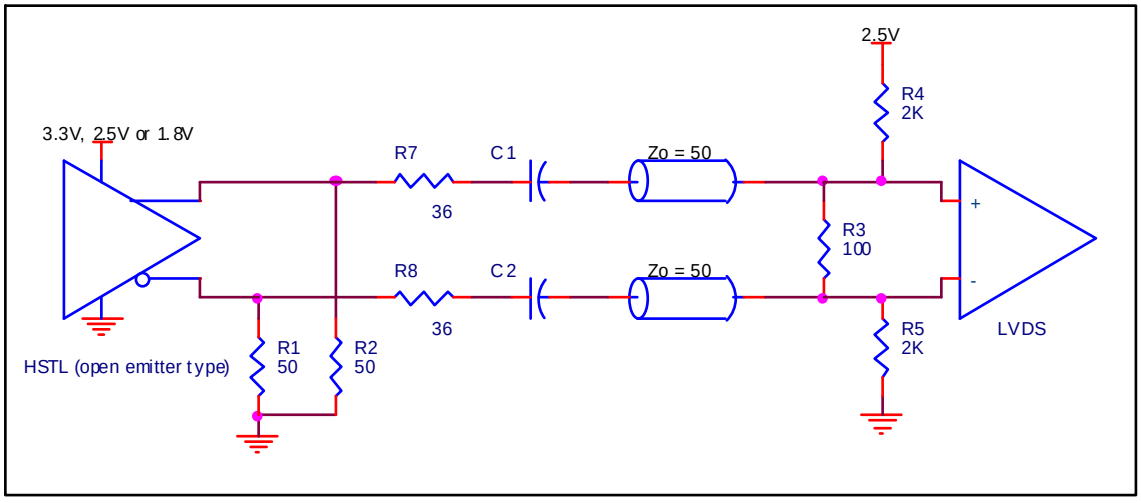
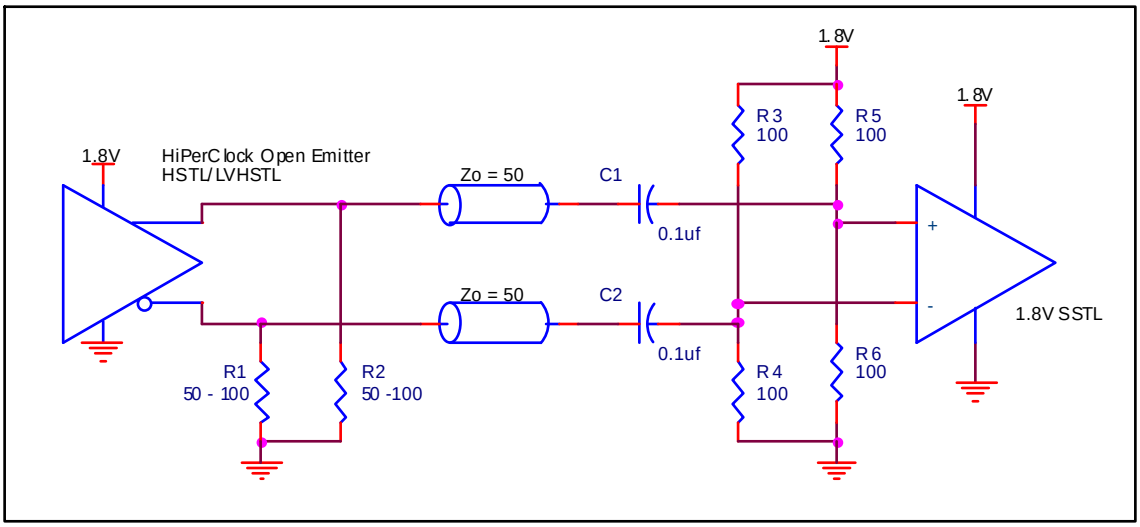
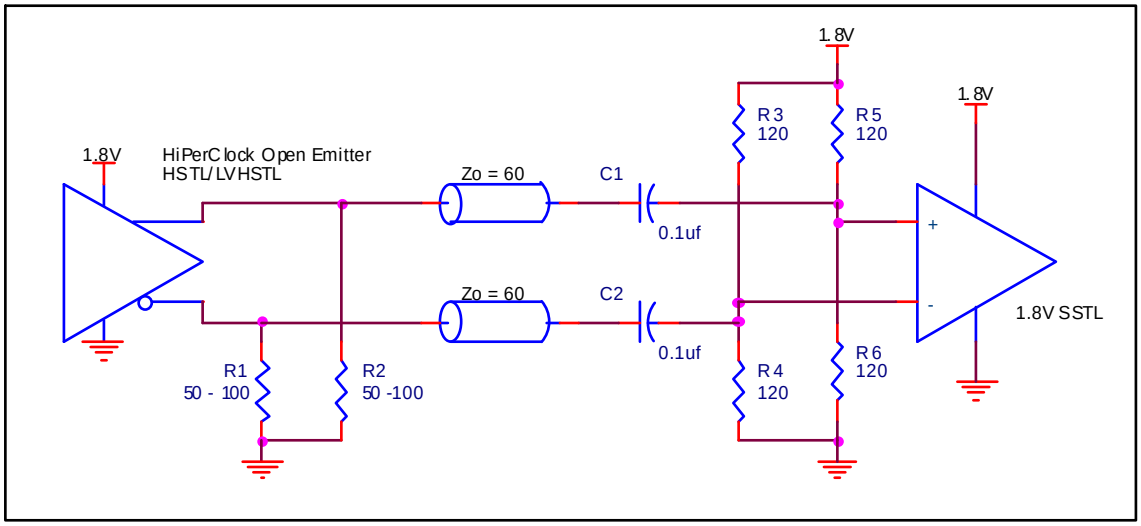


Figure 89. HSTL to 1.8V SSTL, Option 1



Termination for 50-ohm transmission line

Figure 90. HSTL to 1.8V SSTL, Option 2



Termination for 60 ohm transmission line

Figure 91. HSTL to 1.5V HSTL, DC-Couple

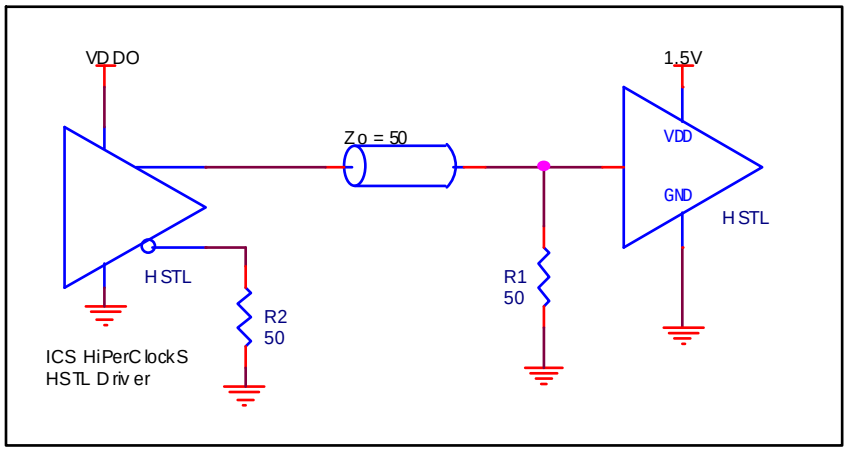


Figure 92. HSTL to 1.5V HSTL, AC-Couple

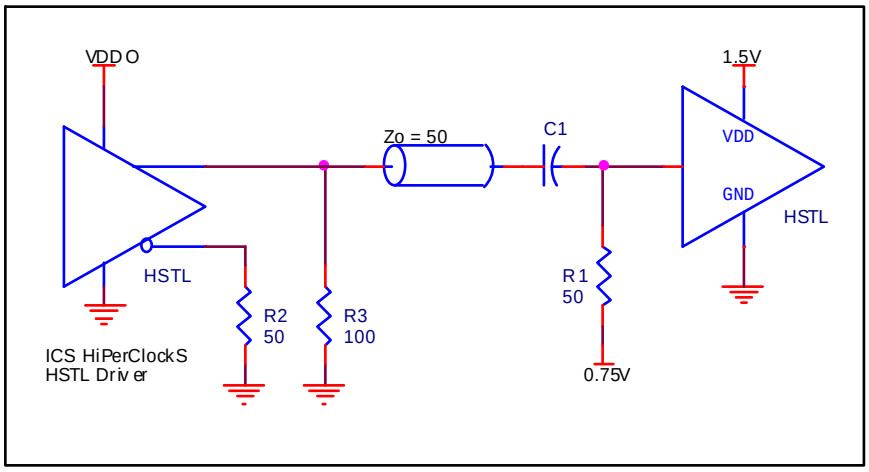


Figure 93. 1.5V HSTL Push-Pull Driver to Differential Input with 0.75V Bias

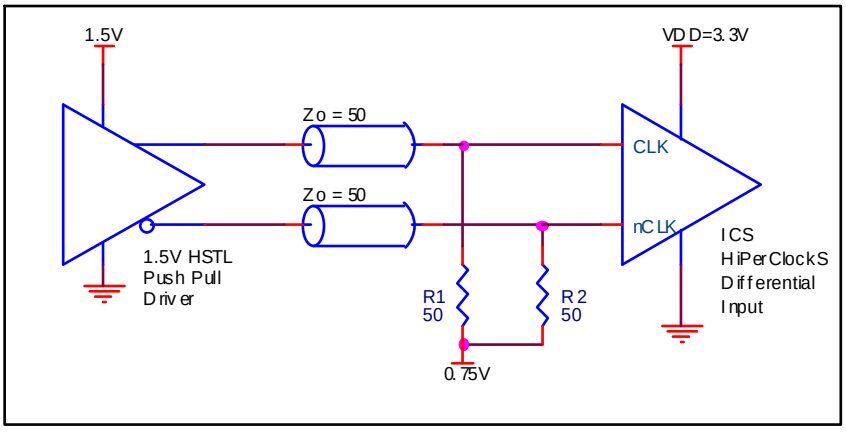


Figure 94. 1.5V HSTL Push-Pull Driver Differential Input Voltage Divider Bias

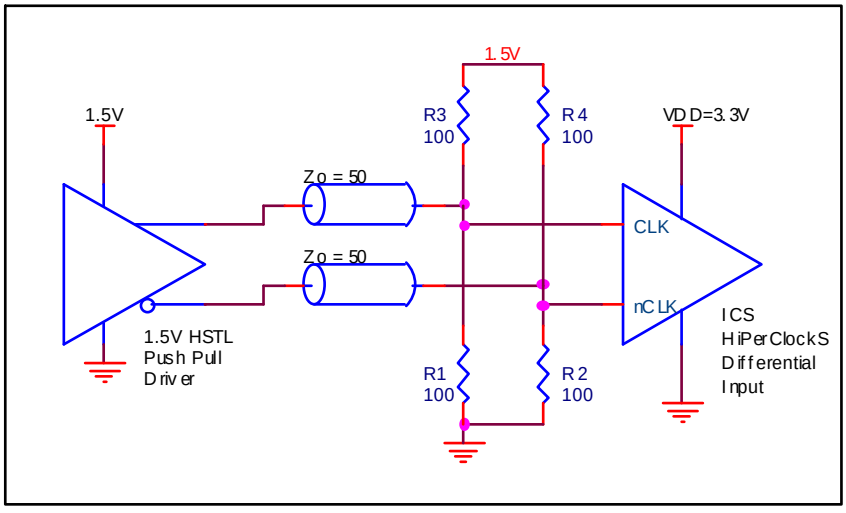
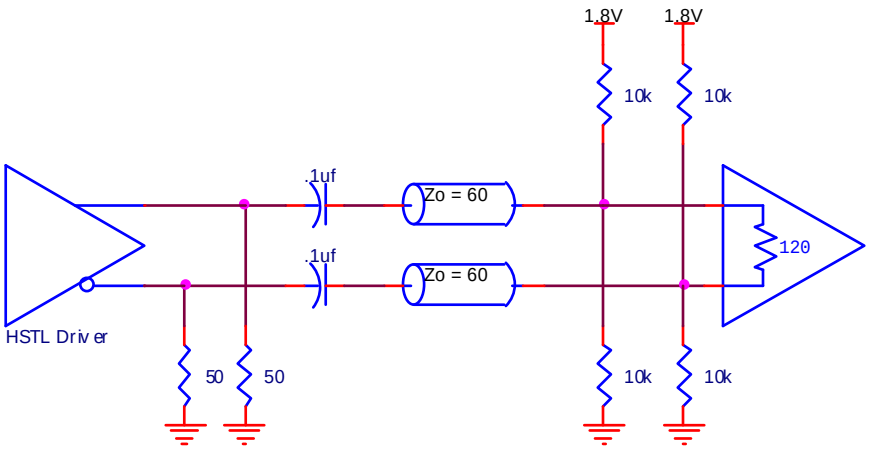


Figure 95. HSTL to DDR2



HCSL Terminations

Figure 96. HCSL to Differential Input Interface with Pulldown at the Driver

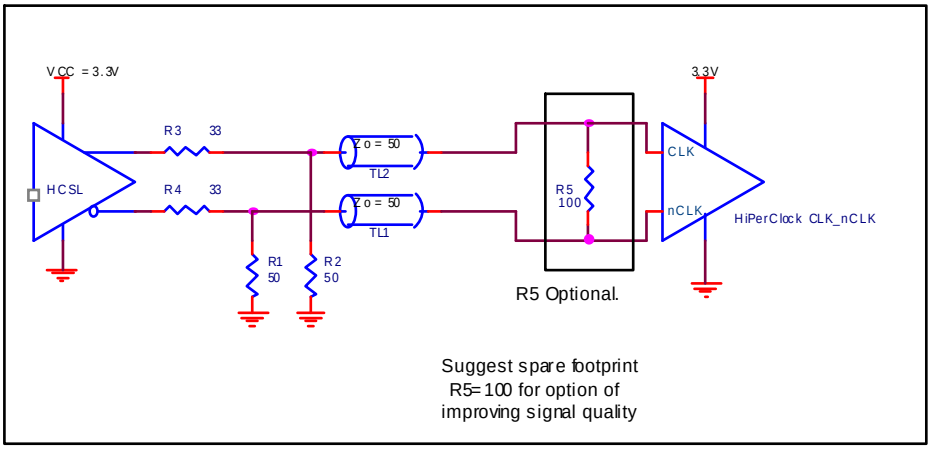


Figure 97. HCSL to Differential Input Interface with Pulldown at the Receiver

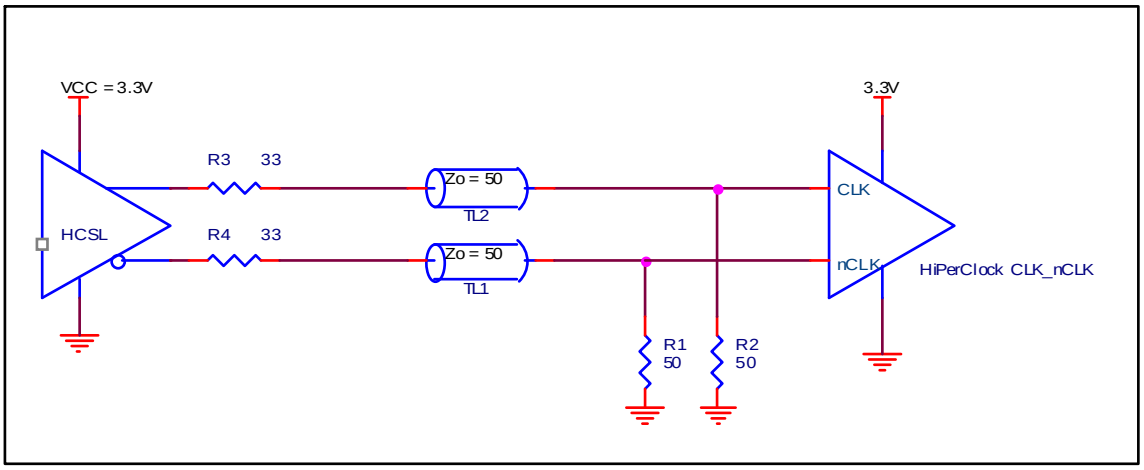


Figure 98. HCSL to LVPECL

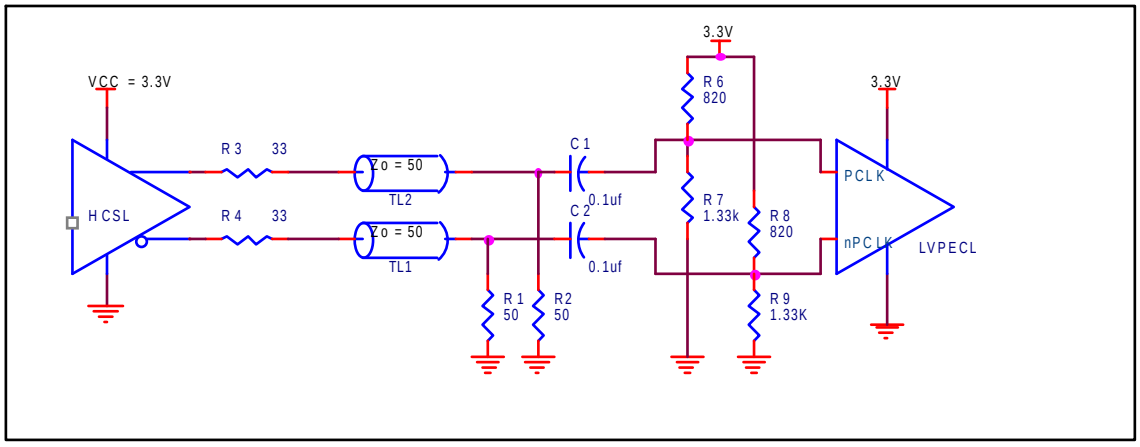


Figure 99. HCSL to IDT Differential PCLK/nPCLK, Option 1

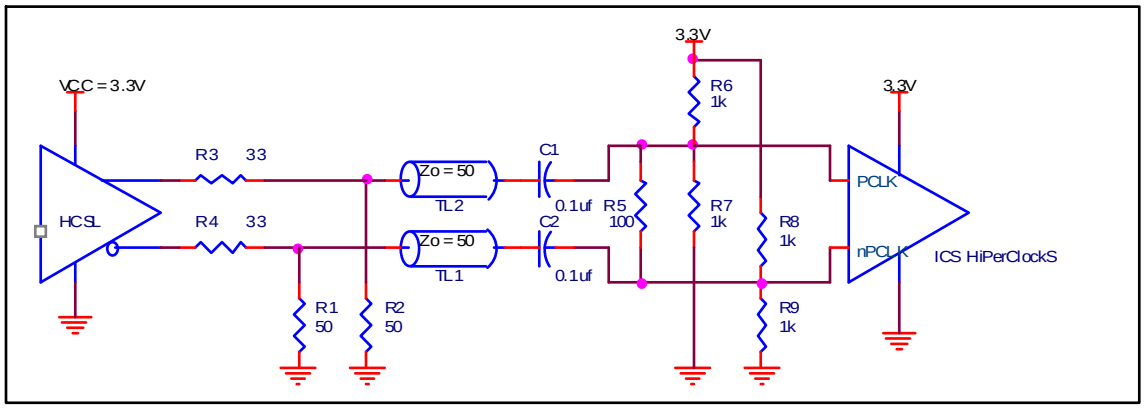


Figure 100. HCSL to IDT Differential PCLK/nPCLK, Option 2

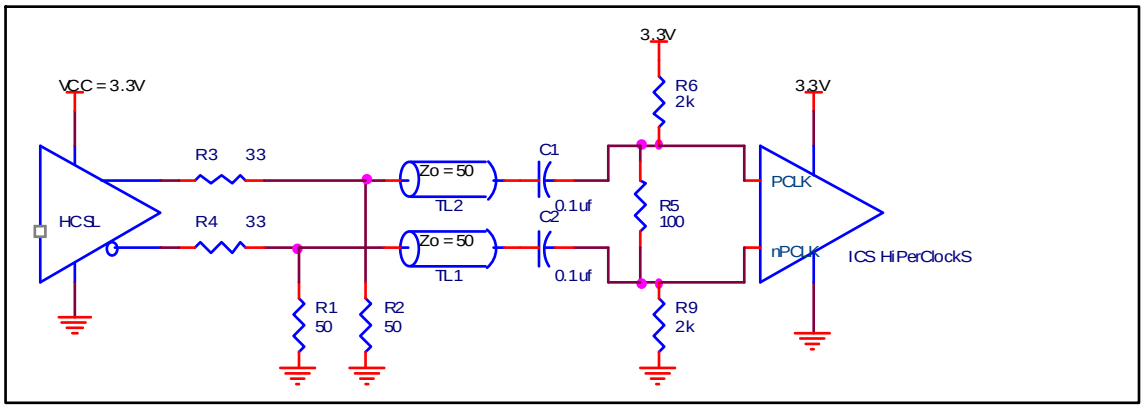


Figure 101. HCSL to IDT Differential PCLK/nPCLK, Option 3

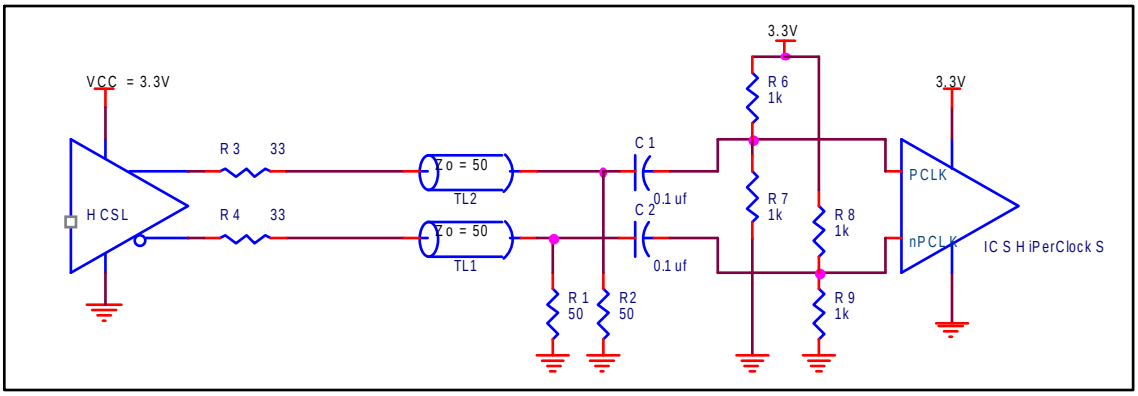


Figure 102. HCSL to IDT Differential PCLK/nPCLK, Option 4

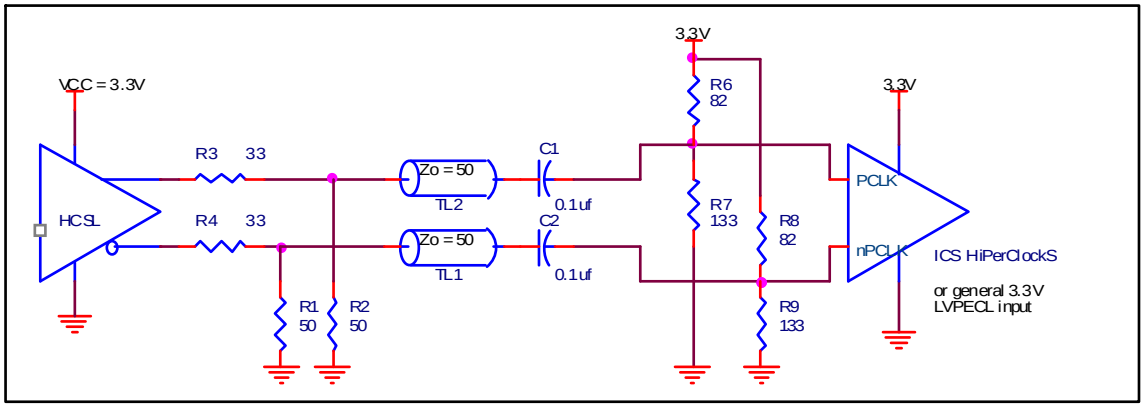
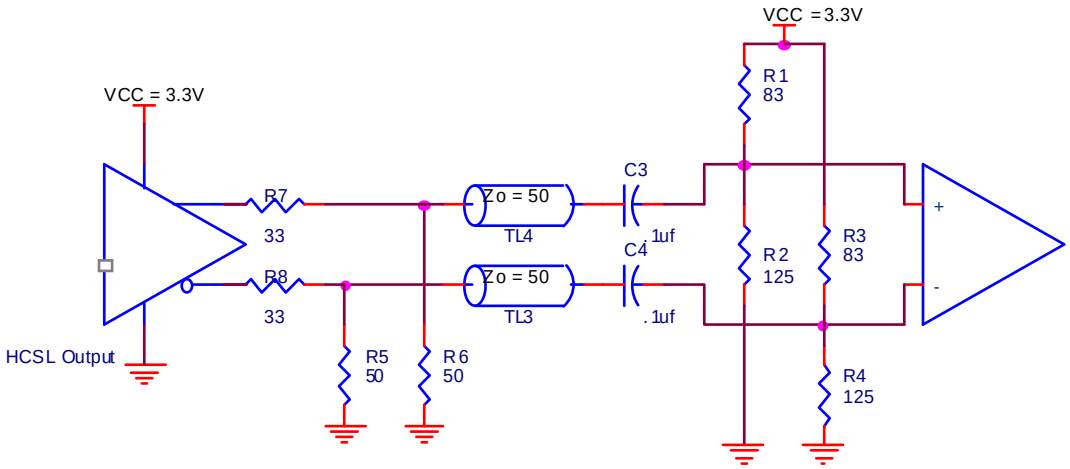


Figure 103. HCSL to 400mV Swing



Reduce R5/R6 values to further reduce the amplitude.

Figure 104. HCSL to 1.5V Differential HSTL Interface

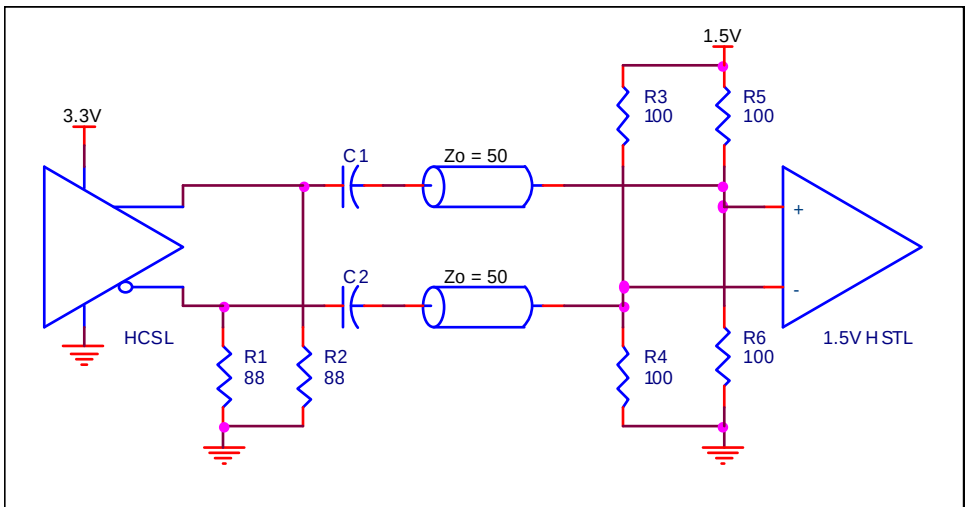


Figure 105. HCSL to 1.8V LVCMOS

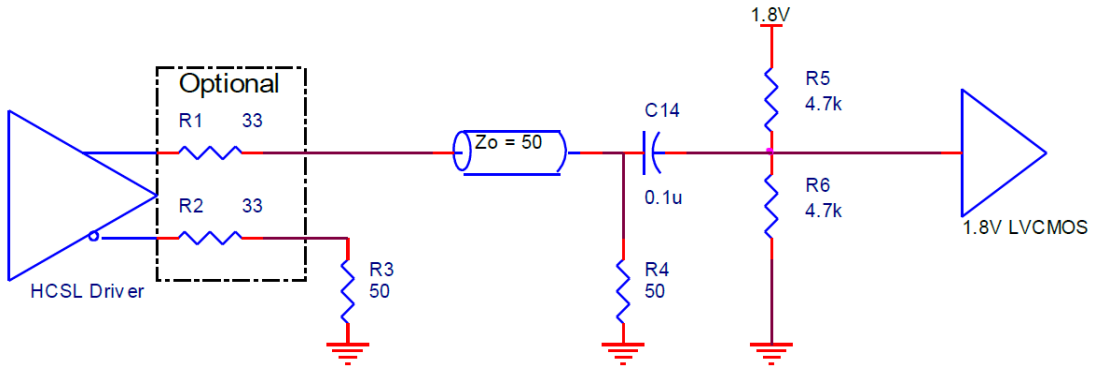


Figure 106. HCSL to Xilinx Vertex 5

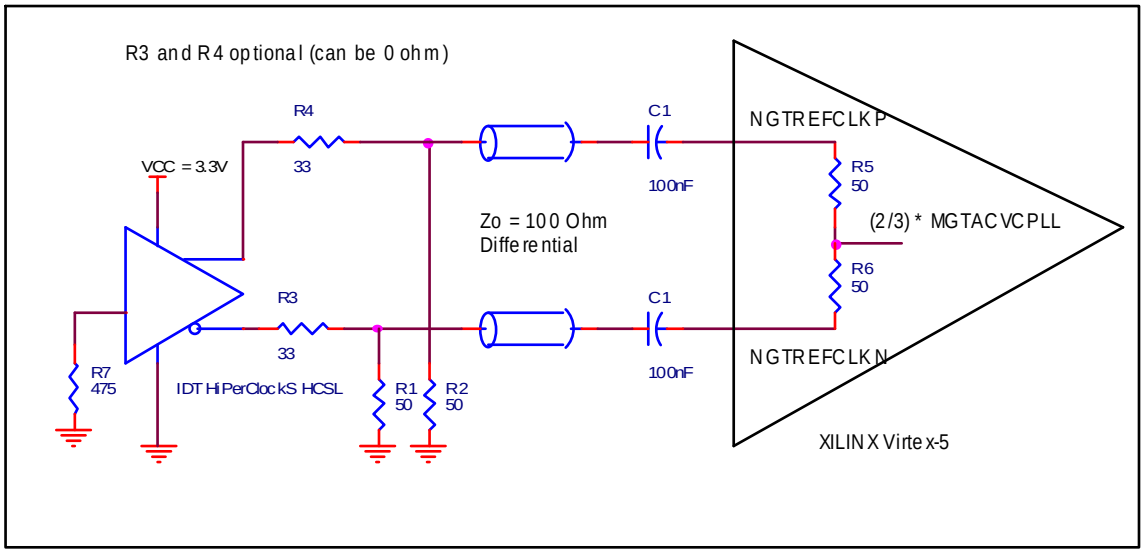
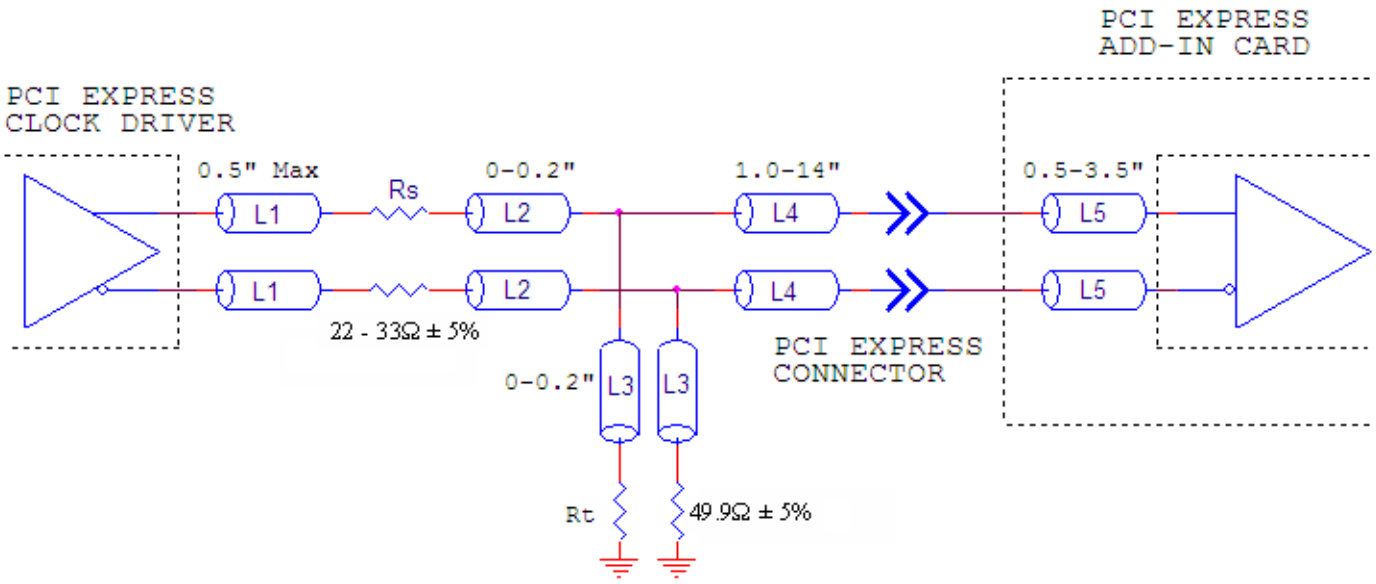
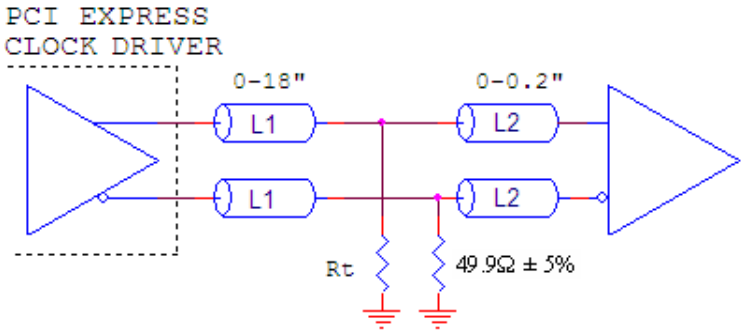


Figure 107. HCSL PCIE Source Termination



Recommended termination for applications which require the receiver and driver to be on a separate circuit board.

Figure 108. HCSL PCIE Receiver Termination



Recommended termination for applications which require a point to point connection and driver and receiver are on the same board.

CML Terminations

Figure 109. CML Standard Termination

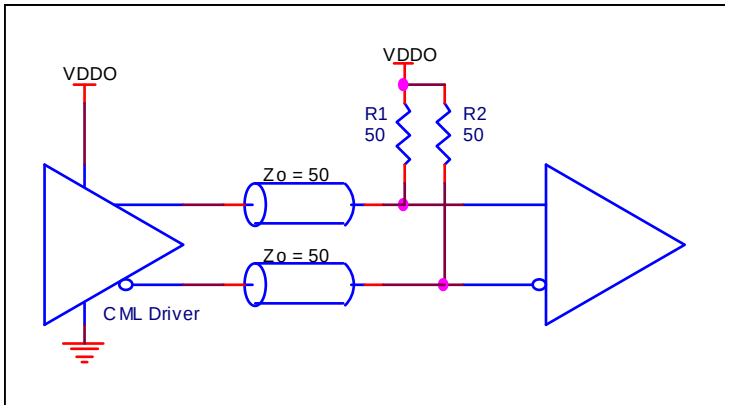


Figure 110. CML to Differential CLK/nCLK

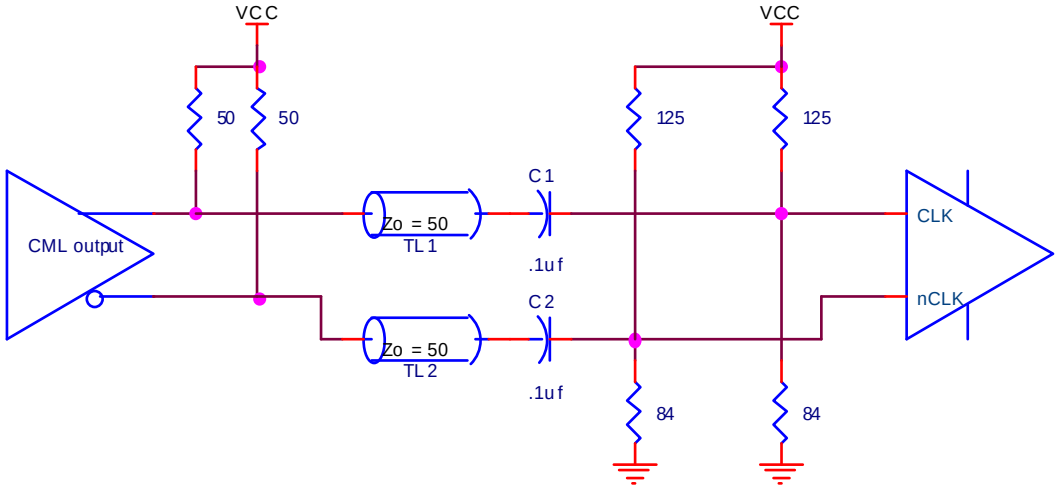


Figure 111. CML to HCSL - Receiver with High Input Impedance

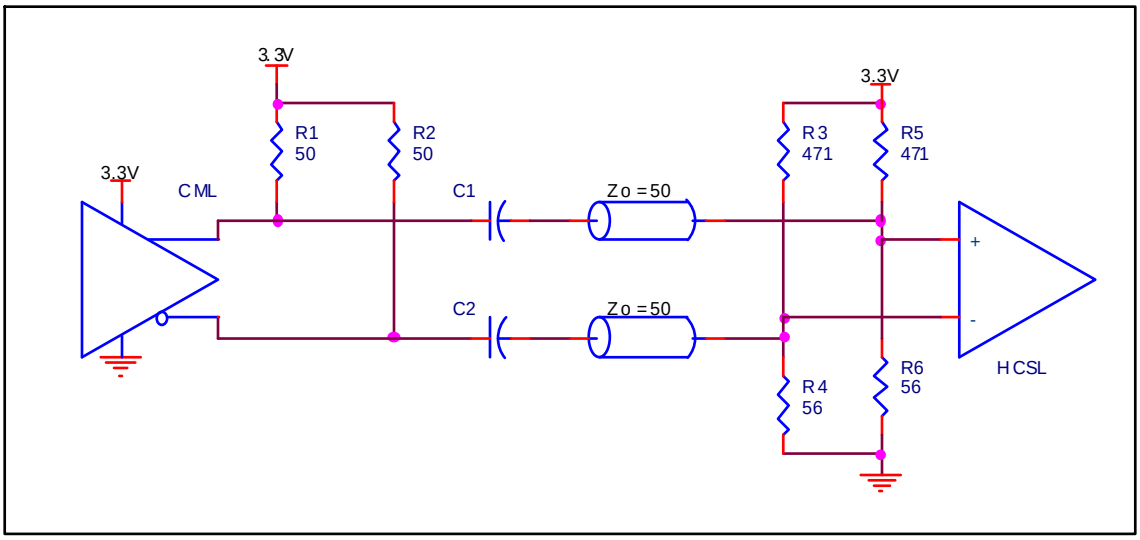


Figure 112. Receiver with Built-in 100 ohm Across

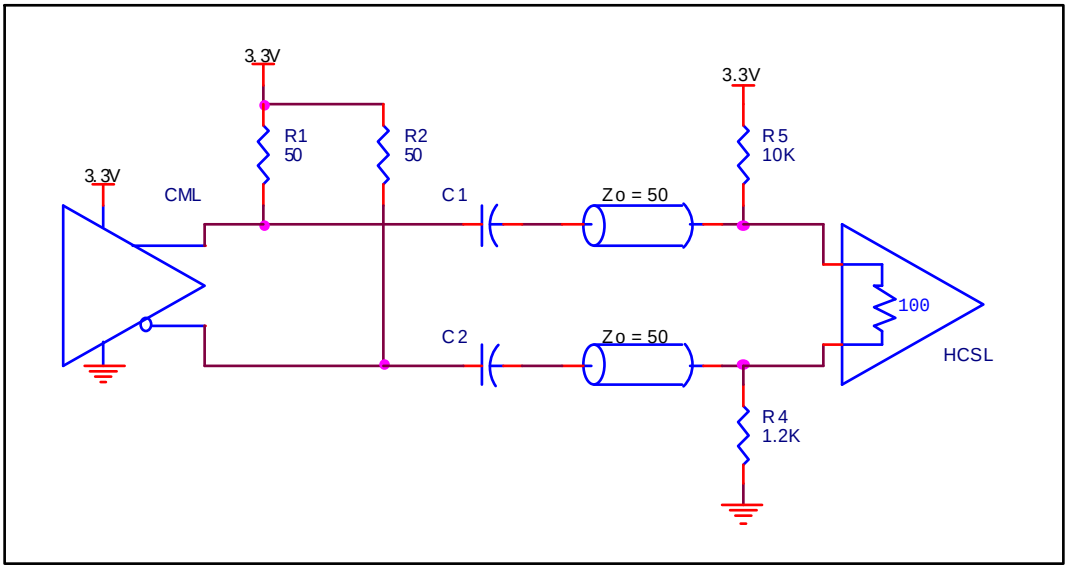
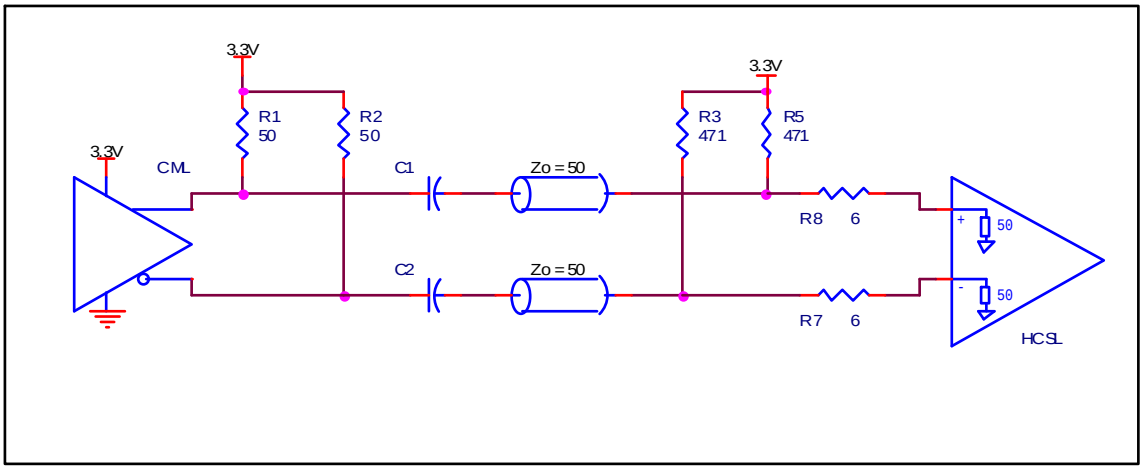


Figure 113. CML to HCSL - Receiver with Built-in 50 ohm to Ground



SSTL Terminations

Figure 114. SSTL 1.8V to Differential PCLK/nPCLK with VBB

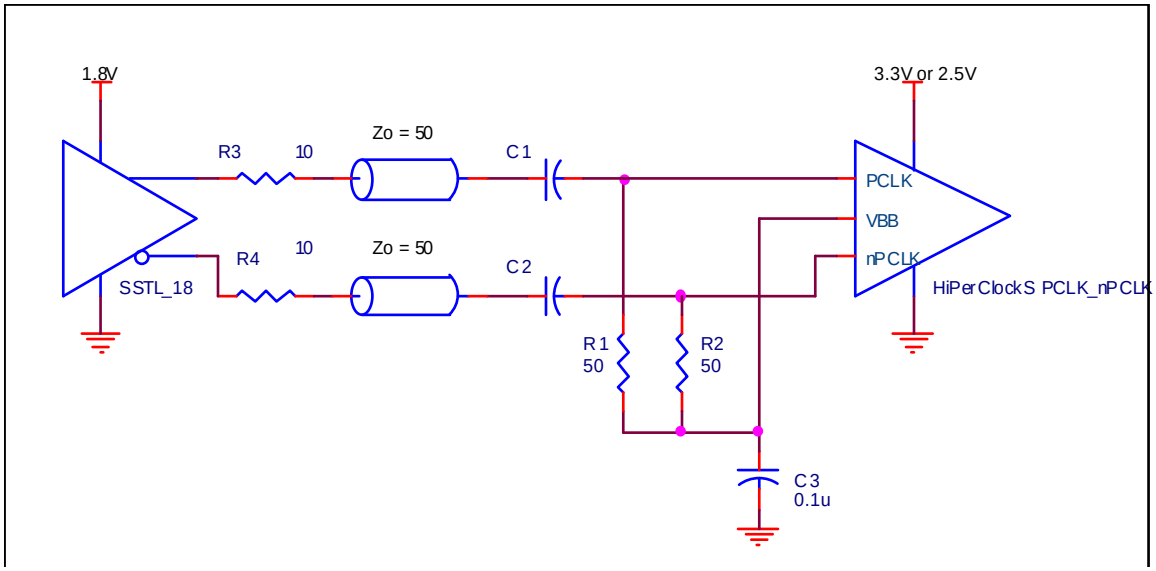


Figure 115. SSTL 1.8V to Differential PCLK/nPCLK, Option 1

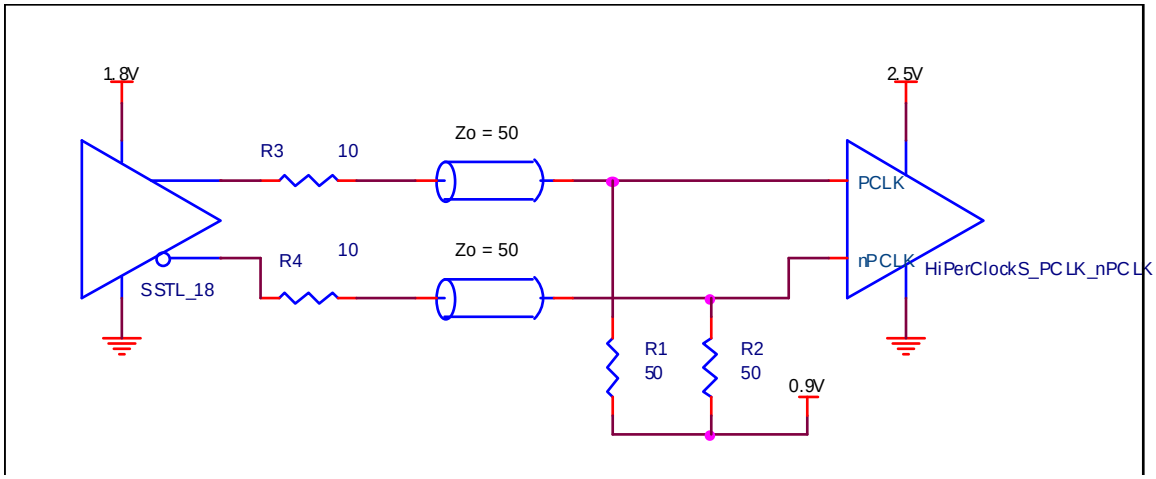


Figure 116. SSTL 1.8V to Differential PCLK/nPCLK, Option 2

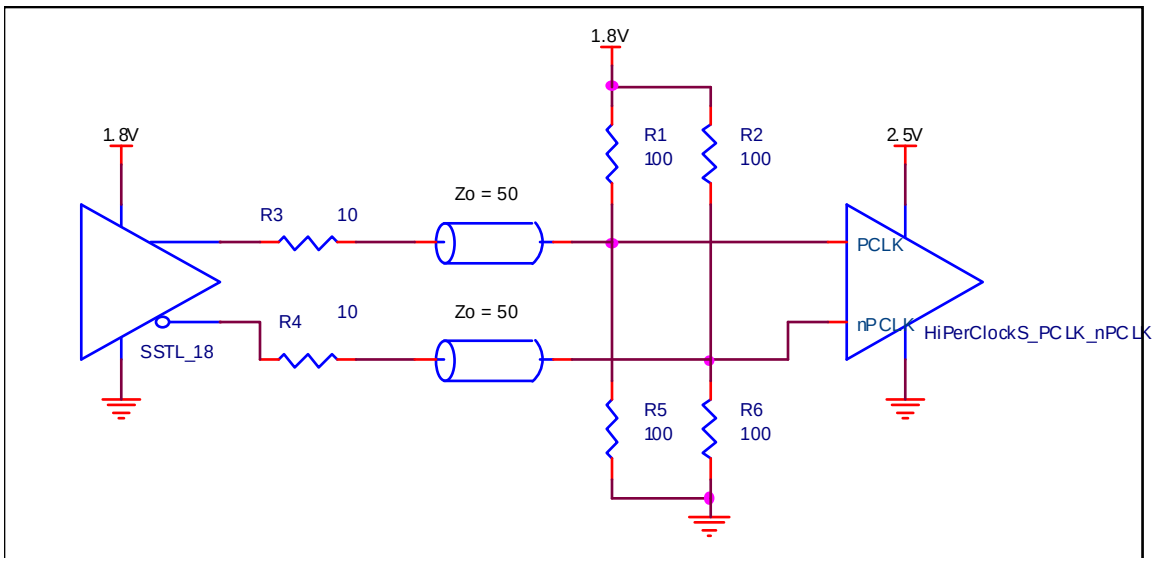
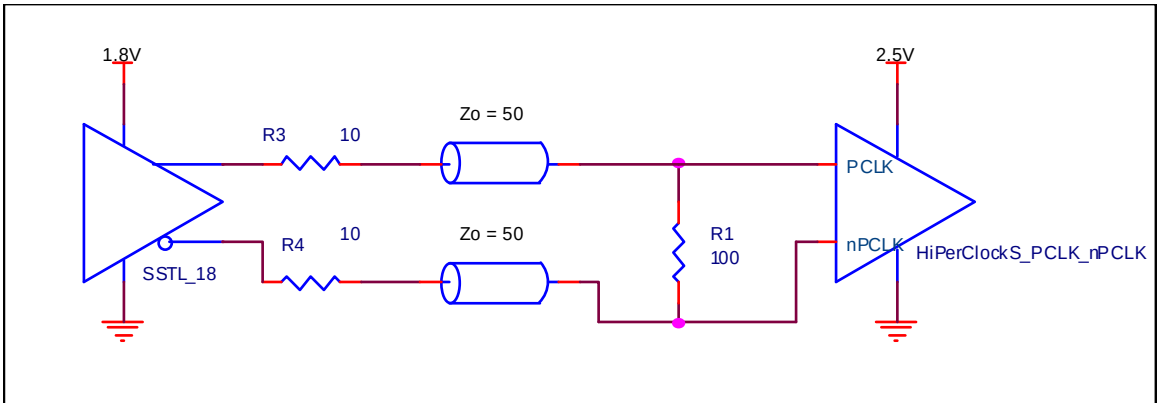
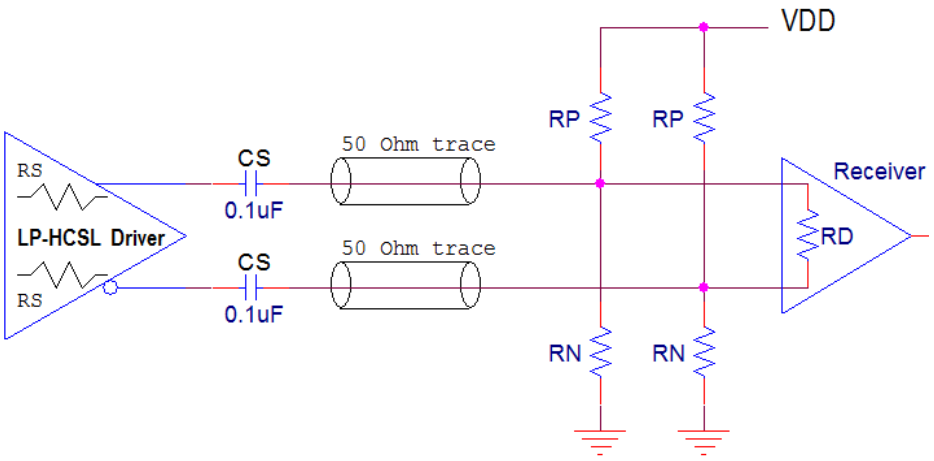


Figure 117. SSTL 1.8V to Differential PCLK/nPCLK, Option 3



Low-Power- HCSL

Figure 118. Universal Network



The above schematic uses a LP-HCSL driver with integrated termination resistors (RS). When using a driver where the termination is not integrated, please add RS=33Ω in series with each pin externally to complete the driver output impedance to 50Ω.

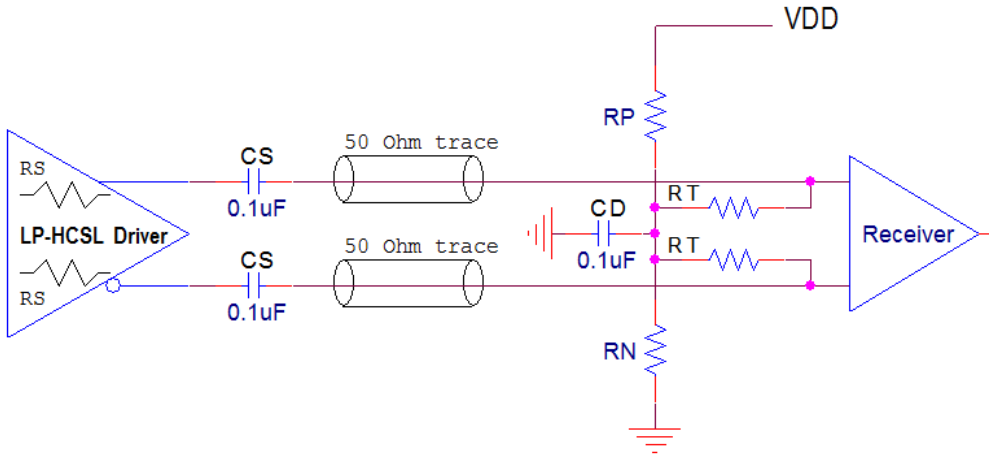
Equations for Figure 118

The Common Mode Voltage depends upon RN, RP and VDD: VCM = VDD × RN / (RN + RP)

The following equation calculates the single-ended swing at the receiver input pins:

VSWING = 800mVpp × (RN // RP // ½RD) / (50 + RN // RP // ½RD)

Figure 119. Universal Network with Amplitude Attenuation



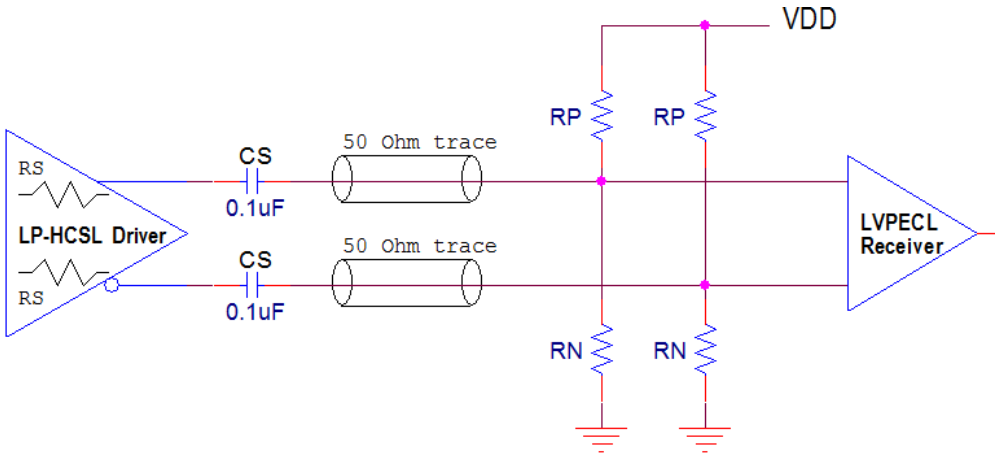
Equations for Figure 119

Common Mode Voltage: VCM = VDD × RN / (RN + RP)

Receiver Input Single-ended Voltage Swing: VSWING = 800mVpp × RT / (50 + RT)

Rewriting to find RT for the required VSWING: RT = 50×VSWING / (800mVpp - VSWING)

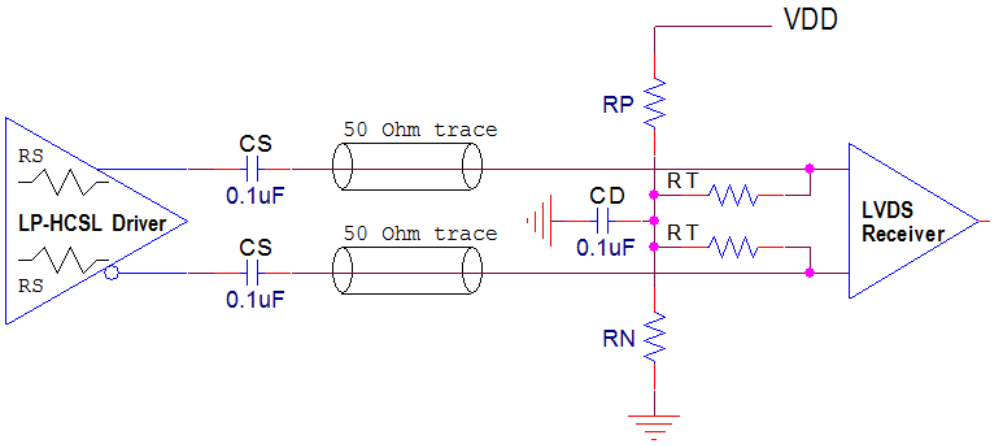
Figure 120. Terminating LP-HCSL to LVPECL with Network



VDD	RP	RN	CS*	V_{SWING}**	V_{CM}
3.3V	2200Ω	3300Ω	0.1µF	771mVpp	1.98V
2.5V	2700Ω	2400Ω	0.1µF	770mVpp	1.18V

* Also add RS=33Ω in series when not integrated in the LP-HCSL driver.
** Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

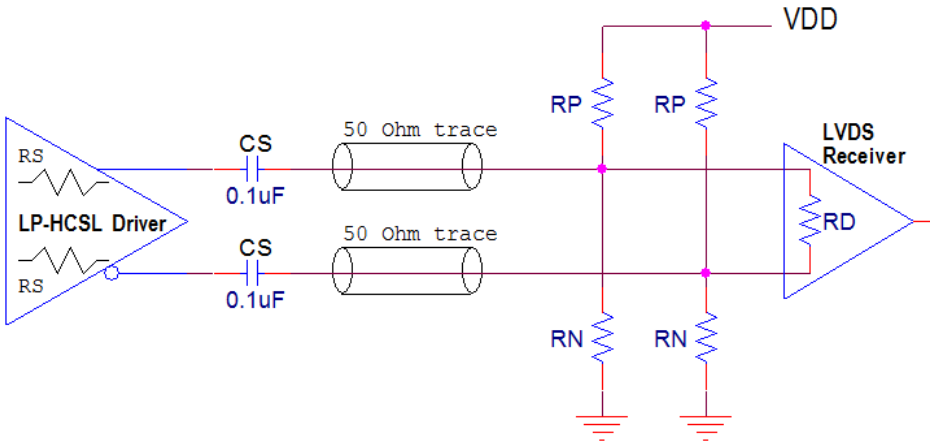
Figure 121. Terminating LP-HSCL to LVDS without Integrated RD



VDD	RP	RN	RT	CS*	CD**	V_{SWING}***	V_{CM}
3.3V	3000Ω	1800Ω	50Ω	0.1µF	0.1µF	400mVpp	1.24V
2.5V	2200Ω	2200Ω	50Ω	0.1µF	0.1µF	400mVpp	1.25V
1.8V	1500Ω	3300Ω	50Ω	0.1µF	0.1µF	400mVpp	1.24V

* Also add RS=33Ω in series when not integrated in the LP-HCSL driver.
** CD is optional for filtering common mode noise in the clock.
*** Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

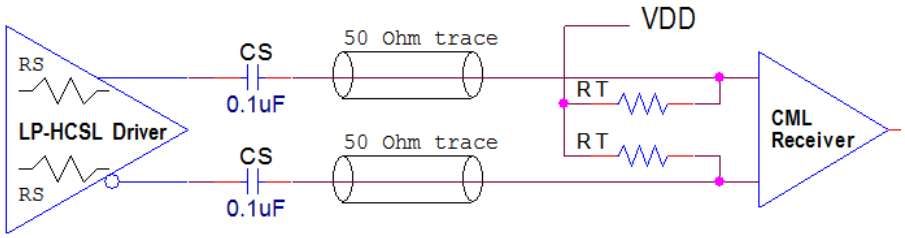
Figure 122. Terminating LP-HCSL to LVDS with Integrated RD



VDD	RP	RN	RD**	CS*	V_{SWING}***	V_{CM}
3.3V	3000Ω	1800Ω	100Ω	0.1µF	391mVpp	1.24V
2.5V	2200Ω	2200Ω	100Ω	0.1µF	391mVpp	1.25V
1.8V	1500Ω	3300Ω	100Ω	0.1µF	391mVpp	1.24V

* Also add RS=33Ω in series when not integrated in the LP-HCSL driver.
** RD is integrated in the receiver so we don't have to assemble it.
*** Single-ended voltage swing, based upon 800mVpp at the LP-HCSL driver.

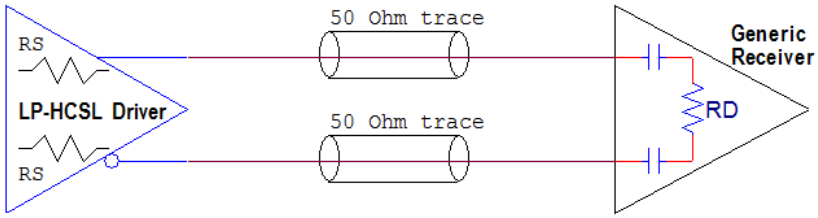
Figure 123. Terminating LP-HCSL to a CML Receiver



RT*	CS**	V_{SWING}***	V_{CM}****
50Ω	0.1µF	400mVpp	VDD

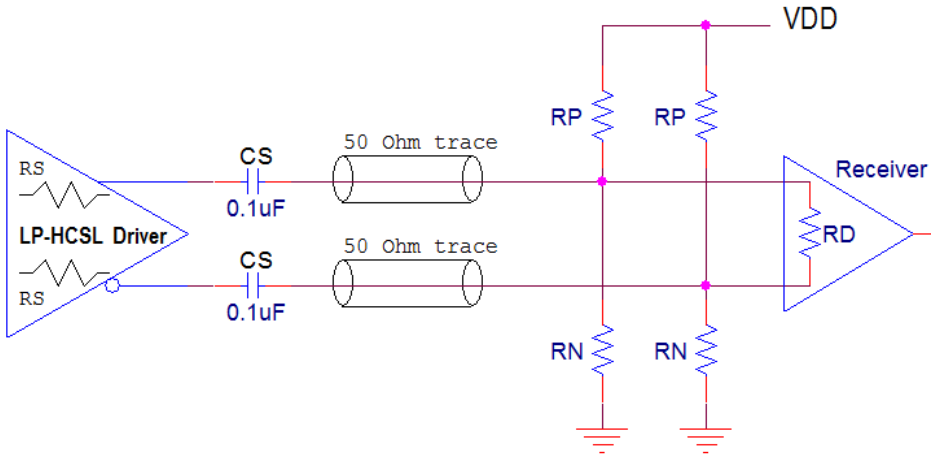
* RT is only needed when not integrated in the CML receiver input.
** Also add RS=33Ω in series when not integrated in the LP-HCSL driver.
*** Single ended voltage swing, based upon 800mVpp at the LP-HCSL driver.
**** VDD is the value used for the CML receiver and does not need to be the same as for the LP-HCSL driver.

Figure 124. Terminating LP-HCSL to a Self-biasing Generic Receiver with On-chip Termination and AC-Coupling



In this case, we can connect the LP-HCSL output directly to the receiver input pins without any additional components. The swing at the receiver input is 400mVpp single ended or 800mVpp differential. Receivers often specify the swing differential.

Figure 125. Terminating LP-HCSL to a Generic Receiver with On-chip Termination

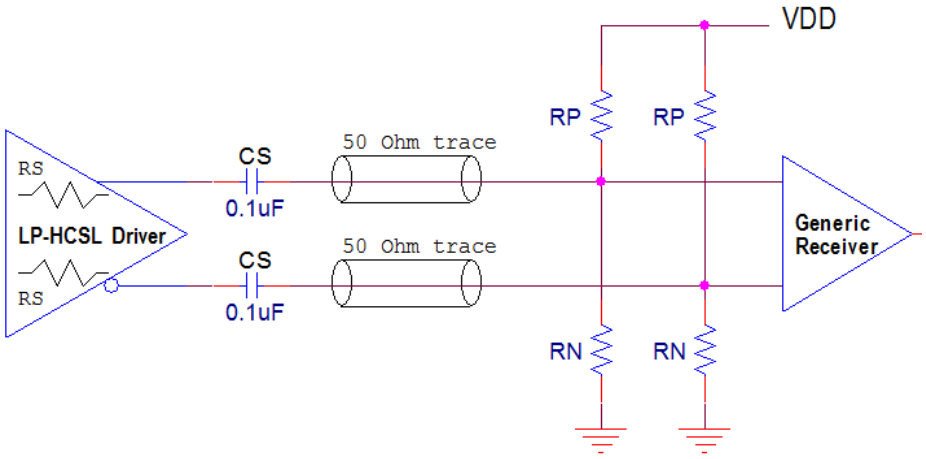


The receiver datasheet may recommend RP and RN values. If not, use the equation on page 2 to find RP and RN values for the required common mode voltage. Make sure that the resistance value for RN and RP in parallel is at least 1KΩ to not load the signal lines too much.

When VDD is for the receiver and the IC's datasheet does not specify a common mode voltage, a good V_{CM} value is 50%VDD. In this case RP and RN can have the same value, for example 2200Ω each.

The swing at the receiver input is 391mVpp single ended with RN = RP = 2200Ω.

Figure 126. Terminating LP-HCSL to Generic Receiver without Termination or Self-biasing



Because generic differential inputs can often handle up to 1000mVpp of swing at the input pins we do not need to attenuate. For noise reasons it is beneficial to make as large a swing as possible.

For RN and RP values, see the previous circuit for a differential input with on-chip termination

Revision History

Table 1. Revision History

Revision Date	Description of Change
March 6, 2017	▪ Updated legal disclaimer
December 9, 2016	▪ Initial release

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(Rev.4.0-1 November 2017)

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