Integrated Device Technology, Inc.

FCT-T DOUBLE-DENSITY LOGIC CHARACTERISTICS AND APPLICATIONS

APPLICATION NOTE AN-146

By Stanley Hronik

INTRODUCTION

IDT's Double-Density product line is comprised of 16, 18 and 20-bit fast CMOS interface parts available in 48 and 56 pin dual-in-line surface mount packages. Double Density Logic offers a small package size, extremely low power dissipation, low leakage, reduced ground bounce and a variety of output drive levels. Double-Density logic is an extension of IDT's Fast CMOS TTL-compatible (FCT-T) line of logic products. Double Density is form, fit, and function compatible with other industry standard logic families, but will provide a significant performance improvement in most applications.

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SCOPE

This application note is intended to be used as a designer's guide to component selection and usage. The data contained within this document is typical data taken at 25ºC and 5.0V Vcc, except where otherwise noted. The data has been derived from component characterization where in most cases, the component selected is an 'FCT16x244T type. The data is intended as a design guideline only. For "guaranteed" specifications the IDT Logic Data Book provides full specifications over Vcc, temperature and process.

DOUBLE DENSITY LOGIC FAMILIES

IDT's 5V Double Density Logic is available in three families, each with specific target applications. Consistent among all of the families is the high speed and very low power dissipation. Pin and functionality uniformity is maintained across the families, allowing plug in replacement if a family transition is required. All FCT logic comes in a variety of speed grades, allowing plug in replacement for performance upgrades or a downgrade for cost savings. The speed grades are uniform across all FCT families including the octal and 3.3V families.

The Double Density FCT Logic families can be divided into three distinct groups:

1) FCT16xxxT, High Drive, -32/64mA
2) FCT162xxxT, Balanced Drive, -24/+24mA
3) FCT166xxxT, BD-Lite, -8/+8mA

High Drive has TTL level outputs with -32/64mA drive capability. High Drive is intended for driving heavily loaded busses and backplanes where significant current levels are required. The TTL level outputs, give lower noise levels and faster switching speeds than can be obtained with similar CMOS rail swing components. High drive has Power-off Disable, making the family ideal for partially powered applications or situations where an interface may become connected/disconnected while powered.

Balanced Drive has TTL level outputs with a drive capability of -24/24mA. Internal series resistors on Balanced Drive reduce the drive and noise levels, giving superior low noise performance on moderately loaded busses. The series resistors are small enough to allow driving a substantial load without sacrificing speed performance, but large enough so that in most applications, additional line termination is unnecessary. The symmetric drive capability will drive a transmisstion line both HIGH and LOW with similar edge rates, solving most line balance problems. Balanced Drive is ideal as a general use family.

BD-Lite (Light Balanced Drive) has TTL level outputs with a drive capability of -8/8 mA. Internal series resistors on BD-Lite provide full series termination, eliminating the need for external series resistors. The internal series resistors are

positioned within the output structure of the component to eliminate almost all ground bounce and other internal component noise. BD-Lite also has symmetric drive levels, giving similar rising and falling edge rates. BD-Lite should be used in point to point applications and other low noise situations such as memory or ASIC driving.

Industrial Temperature and Voltages

Standard Double Density components are specified over the extended industrial temperature range of -40C to 85C. The industrial power supply range of Vcc = 5.0V ±10% is also used, guaranteeing the performance of IDT's components under wider operating conditions than standard commercial parts.

These defined limits for Vcc and Temperature are test conditions under which the components are tested and guaranteed to operate at data sheet specifications. The components will operate beyond these established test limits if kept within the absolute maximum ratings as defined in each data sheet. Typically FCT Double Density components will increase in speed under cold conditions and higher Vcc levels. Double Density tends to slow down under hot conditions with lower Vcc levels.

Gate Array Design Approach

FCT logic is built using standard gate arrays with a "sea of gates". The arrays are uniform across products of similar pin count, but allow a final metal mask variation which gives the unique part type logic characteristics. In addition, the final metal mask allows a selection of output characteristics, allowing a single array type to provide all families including High Drive, Balanced Drive and BD-Lite.

Using the standard gate array approach, IDT maintains a high level of consistency from component to component and logic family to logic family. This eases component qualification for most users because a single qualification makes available a wide variety of products.

DC ELECTRICAL CHARACTERISTICS

Included in the DC Electrical Characteristics are device input and output impedances, drive capabilities and breakdown limitations. The guaranteed DC test limits are shown in the IDT Logic Data Book in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table and OUTPUT DRIVE CHARACTERISTICS table for each component.

When calculating loading, drive capabilities, power dissipation and line termination needs, additional information beyond the data book specifications is often required. This information is supplied here.

Input Characteristics

In addition to the above, Double-Density devices have the advantage of extremely-low input capacitance where typical values range from 3 to 5pF. This makes it possible for a high-impedance source elsewhere on the board to drive many Double-Density inputs. The input structure of all IDT FCT logic is shown in Figure 1. The structure consists of the gates to a P-Channel and an N-Channel FET. A parasitic clamp diode connects the input to ground, but there is no clamp diode to Vcc associated with the input. Components that combine an input with an output (forming an I/O port) may have a clamp to Vcc depending upon the type of output structure selected.

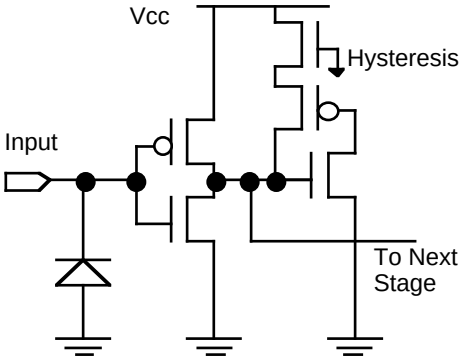

Figure 1, Input Structure

Contained within the input structure is a hysteresis circuit that provides a weak positive feedback into the input causing a small difference between Vih (logic HIGH threshold) and Vil (logic LOW threshold). This helps to reduce noise induced switching and oscillations that may occur when the input voltage level hovers near the input toggle point as it might with a slowly ramping input.

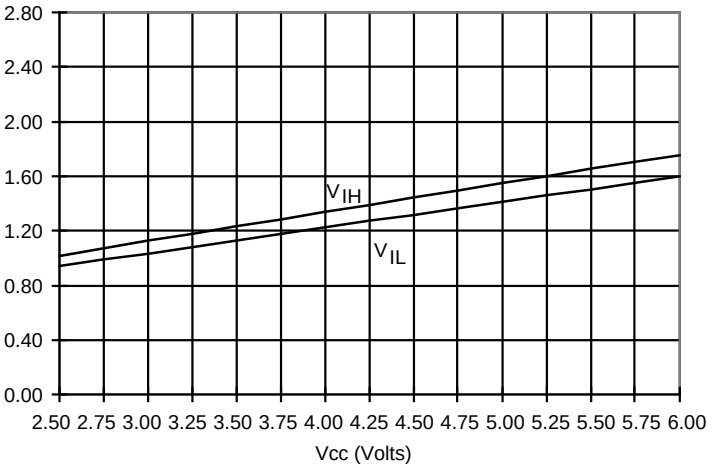

Figure 2, Input Threshold Voltage (Vih/Vil)

The input threshold voltage for FCT-T logic is set at a nominal 1.5V with Vcc = 5.0V. As can be seen in Figure 2, the input threshold will vary relative to Vcc with the input hysteresis causing the slight difference between Vih and Vil. The data sheet limit for Vil is >0.8V and the limit for Vih is <2.0V. These values are guaranteed when Vcc is between 4.5V and 5.5V.

Figure 3 shows the V/I curve for device inputs. As the input voltage drops below -0.7V the effect of the input clamp can be seen as the input current level increases dramatically. Within the normal operating range of -0.5V to 5.5V, the input current typically is >0.1uA. As the input voltage increases beyond the absolute maximum rating (7.0V), the device will begin breakdown. This typically occurs at some level beyond 12 volts and may cause damage to the component.

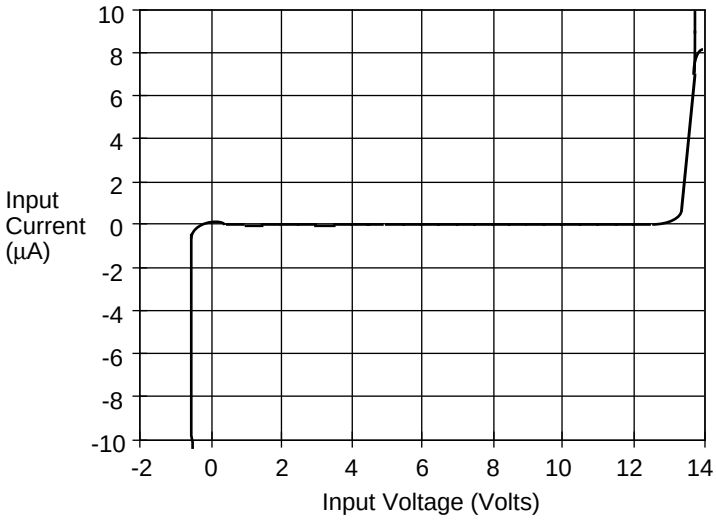

Figure 3, Input Impedance

Operating a device near or beyond the absolute maximum rating may affect the long term reliability of the component.

Unused and Floating Inputs

Because of the high input impedance of CMOS components an input will not drive itself to a valid logic state. Inputs left floating may float near the logic threshold and cause power dissipation as shown in Figure 33. In addition, if the input is picking up a low level, high frequency noise, the input stage may toggle causing the component to oscillate. If the oscillating frequency becomes extreme, the power dissipation of the component may reach high levels, eventually causing device failure.

Special problems may occur with inverting components that have floating inputs. As a floating input toggles the device, the reverse direction of the output switching on an inverter may cause a temporary shifting of the ground reference (ground bounce). A change in ground reference may change the input toggle voltage, causing it to pass back through the floating input voltage. As this back and forth ground shifting continues, the device may go into a high frequency oscillation.

Input hysteresis which is present on all FCT logic should mitigate many of the oscillation effects caused by noise on a floating input, slowly rising/falling input signals, and bounce, but a typical 100mV hysteresis level is not sufficient to fully overcome these effects.

Components that use bus-hold as shown in Figure 4 will automatically drive all 3-state inputs to valid logic states, avoiding floating buses. Bus-hold characteristics are discussed in application Note #AN143.

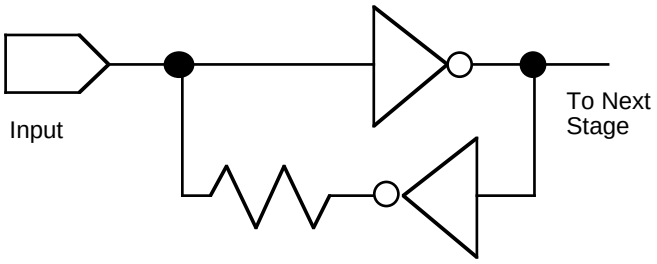

Figure 4, Bus-hold Input Circuit

Unused inputs should be tied directly to Vcc or GND to achieve very low input power dissipation. Using a pull up or pull down resistor of any value (<100KΩ) is also acceptable. Rising and falling input levels of greater than 5 to 10ns should be avoided to insure clean transitions. Slowly rising edges (as may be seen with a large pull up/down resistor) may not produce clean output waveforms, but will cause no component damage. Inputs with bus-hold will retain the last state of the bus and need no additional pull up or pull down resistors.

Output Characteristics

The distinguishing difference among the three Double Density families of 5 volt components is the device output structure. Each family is adapted to provide superior performance in a range of applications. High Drive with a low output impedance is ideally suited to driving heavy busses and backplanes. Balanced Drive is ideal for driving on board busses, memory arrays, and general applications that require low noise levels. BD-Lite is intended for on board, point to point bus driving in circuits that require very low noise levels.

Because Double Density is a CMOS family using CMOS drivers, the V/I characteristics are linear in the region near zero for Vol. The Voh characteristics are also linear throughout the normal operating region. This allows the designer to fairly precisely select termination schemes. Non-CMOS components such as BiCMOS have non-linearities in their drive levels and make termination schemes less precise and more difficult.

High Drive Output Structure

The High Drive output structure is shown in Figure 5. The impedance values shown include the impedance of the associated FET in saturation. The pull down impedance which is approximately 6.5Ω is capable of driving a 64mA load with a Vol level of <0.55 volts.

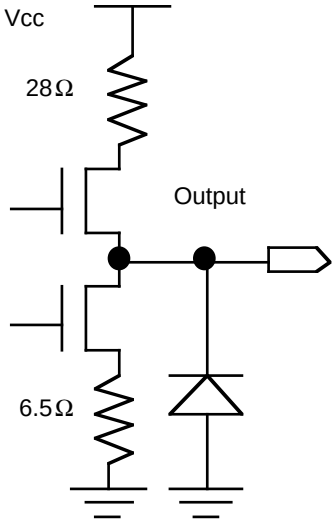

Figure 5, FCT16xxxT Output Structure

Figure 6 shows the VI curve of a High Drive Double Density component in a logic LOW state. Saturation is reached at approximately 260mA with Vol > 2.5V.

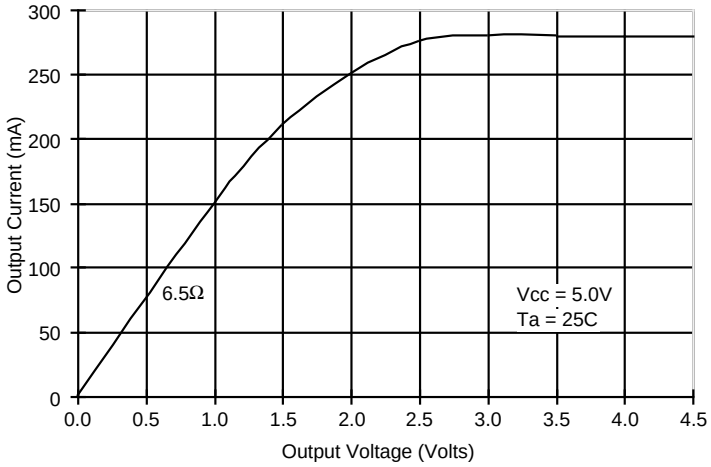

Figure 6, VOL Characteristics of High Drive

Figure 7 shows the logic HIGH impedance for the same component. Saturation is not reached within the test range from -0.5V to 4.5V, but cut off is seen at approximately 3.5V. Cut off is due to the requirement for a gate to source voltage drop of approximately 1.5V to turn the pull up N-Channel FET on. The point of cut off will vary directly with the value of Vcc. Using this voltage drop from Vcc is how TTL logic levels are achieved in CMOS components. For a typical case then, a High Drive component can be modeled as a 6.5Ω resistor to ground for a logic LOW and a 28Ω resistor to 3.5V (Vcc - 1.5V) for a logic HIGH.

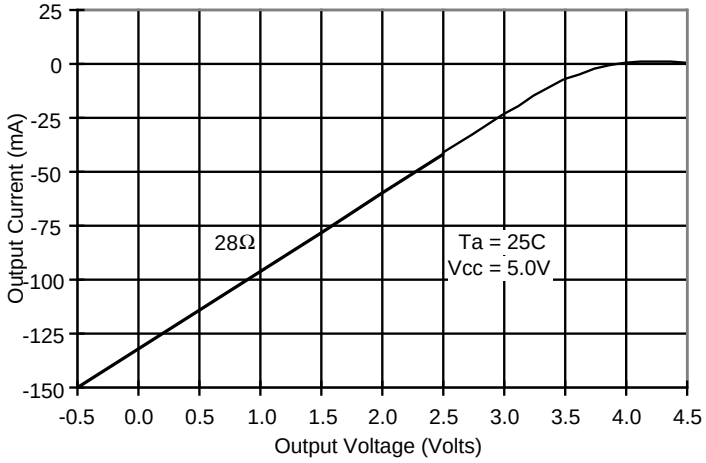

Figure 7, VOH Characteristics of High Drive

High Drive has no clamp diode between either the output or input to Vcc, giving the component "Power-off Disable" capability. Power-off Disable allows use of the component in partially powered or hot insertion applications. A full description of the feature and design techniques can be found in Application Note #158.

Balanced Drive Output Structure

FCT162xxxT logic contains a larger integrated series resistor in the pull down structure than High Drive. Figure 8 shows a schematic of the output structure. The resistor reduces ground bounce, line noise, EMI, and other effects of excessive drive, without degrading device performance. The impedance values shown include the saturation impedance of the FETs.

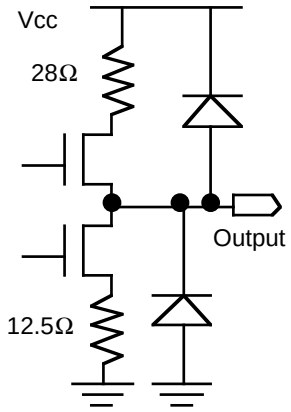

Figure 8, FCT162xxxT Output Structure

The slightly increased impedance gives Balanced Drive enhanced output edge rate control which improves the signal characteristics during transitions and improves the overshoot and undershoot characteristics of the device. Due to differences in the output structure of the Balanced-Drive from that of the High-Drive part, the Balanced-Drive will exhibit about 0.5ns less propagation delay for the HIGH-to-LOW transition than the High-Drive part for loads of less than 200pF.

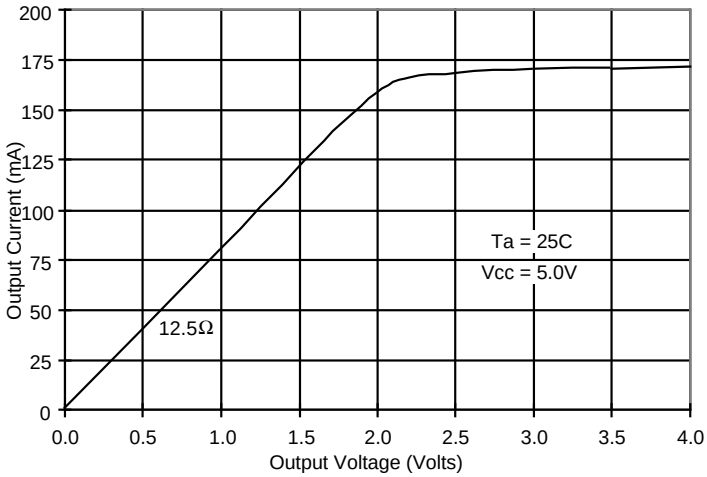

Figure 9, Vol Characteristics of Balanced Drive

Figure 9 shows the V/I curve for Balanced Drive Vol. The slight increase in impedance over High Drive will provide a light series termination without significantly cutting the drive level of the component. The advantage of keeping the impedance modest is the ability to drive a heavier load while maintaining speed. Also first incident wave switching is easier to achieve with a lower output impedance. It may be desirable to add additional resistance or use a BD-Lite part if the application requires full series termination.

The graph of Figure 10 shows the output high characteristics of Balanced Drive. As can be seen in the chart, the pull up impedance is identical to a High Drive component at voltages lower than Vcc. Balanced Drive does have a clamp diode to Vcc, so if the output voltage happens to rise above Vcc, the clamp will forward bias. This prevents using Balanced Drive outputs in Power-off Disable applications. Forward biasing the clamp diode may possibly cause a burnout of the device.

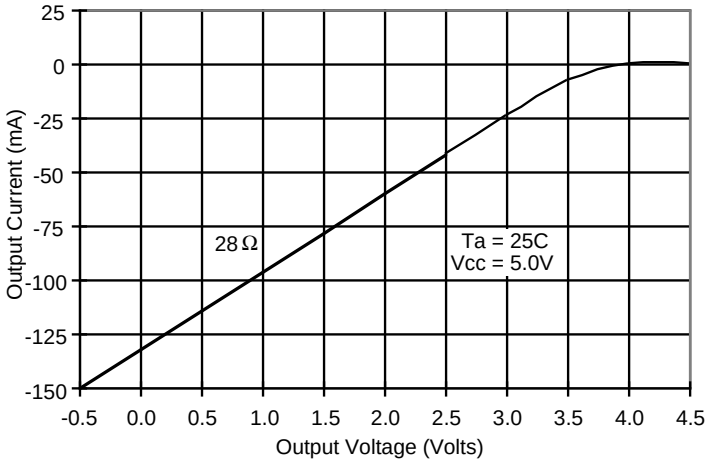

Figure 10, Voh Characteristics of Balanced Drive

The inputs on Balanced Drive have no clamp and therefore can be tied to a powered bus while Vcc is off, unlike the outputs and I/O ports.

BD-Lite Output Structure

FCT166xxxT BD-Lite components approximate adding a 25 ohm resistor to the output of a High Drive component for series termination. The output structure of BD-Lite is shown in Figure 11. An added advantage of placing the resistors internally in the locations shown is that all internal switching currents for the output structure, including crossover currents must pass through these resistors. This significantly cuts internal noise and ground bounce, without having any negative effect over an external resistor. External resistors used for series termination have no effect on crossover currents.

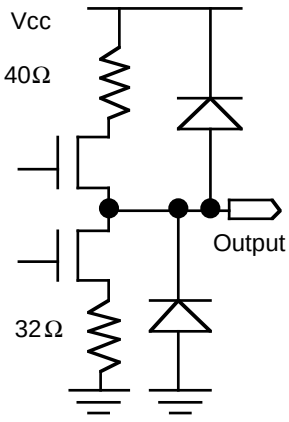

Figure 11, BD-Lite Output Structure

Adding a series resistor either internally or externally will decrease the response time when switching a heavy load. This is an effect of the RC time constant that develops between the driver and the load.

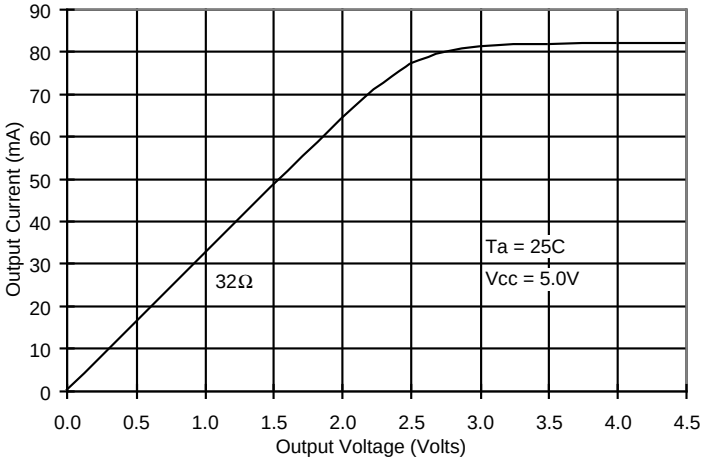

Figure 12, BD-Lite Output Low Characteristics

The Vol characteristics of BD-Lite devices are shown in Figure 12. As can be seen by the figure, saturation current is slightly greater than 80mA and the impedance characteristics are highly linear below 2.5V.

The pull up characteristics of BD-Lite are shown in Figure 13. As can be seen in the figure, the pull up impedance is approximately 40Ω which is significantly higher than the 28Ω of both High Drive and Balanced Drive.

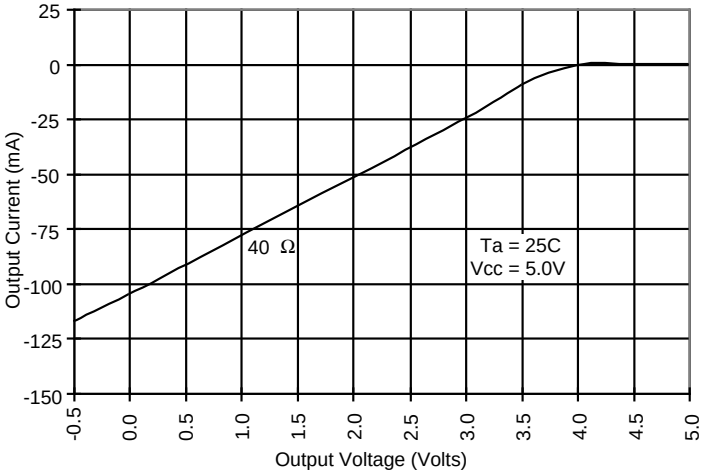

Figure 13, BD-Lite Voh Characteristics

BD-Lite output and I/O ports also have a clamp diode to Vcc, so if the output voltage happens to rise above Vcc, the clamp will forward bias. This prevents using BD-Lite outputs in Power-off Disable applications. The inputs on BD-Lite have no clamp and therefore can be tied to a powered bus while Vcc is off, unlike the outputs and I/O ports.

Temperature Effects and DC Drive

Temperature affects the gain of integrated circuits and will therefore have an effect on the drive level of all circuits. Figure 14 shows how the Voh of a Double Density component will change with temperature while delivering 24mA of current.

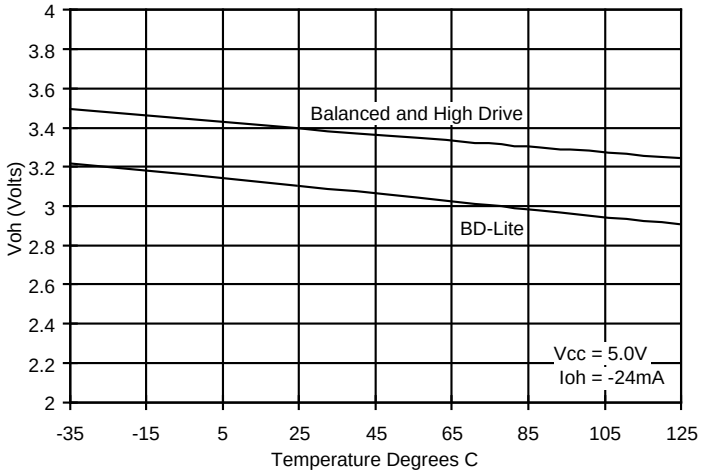

Figure 14, Variation in Voh with Temperature

The Double Density Vol is also affected by temperature. The effect of temperature under a 24mA load is shown in Figure 15.

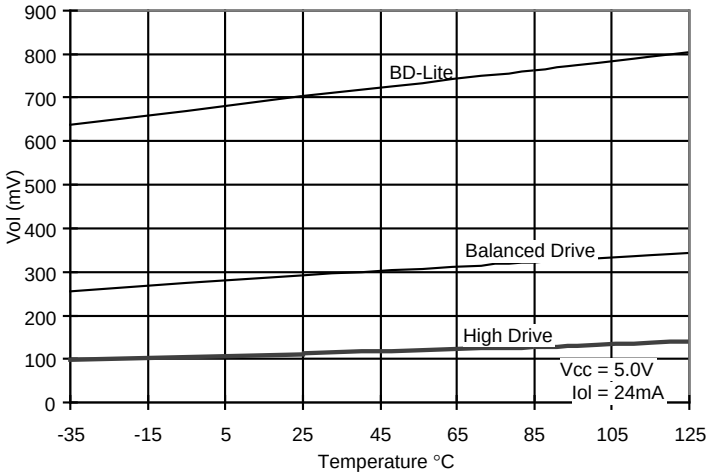

Figure 15, Variation in Vol with Temperature

With the higher output impedance of Balanced Drive and BD-Lite, the effect of temperature on Voh and Vol is proportionately more pronounced than with High Drive, but still at nominal levels.

I/O Port Characteristics

I/O Ports are simple combinations of input and output structures on the same pin. When acting as an output driver, an I/O port will have identical characteristics to a standard unidirectional output port from the same family. When the output driver is 3-stated (High Z) the port will be acting as an input port. When using Balanced Drive or BD-Lite components, the output clamp diode to Vcc will limit the range of the input voltage to Vcc + 0.5V as shown in Figure 16. High Drive I/O ports will have identical characteristics to a unidirectional input port when the output is 3-state.

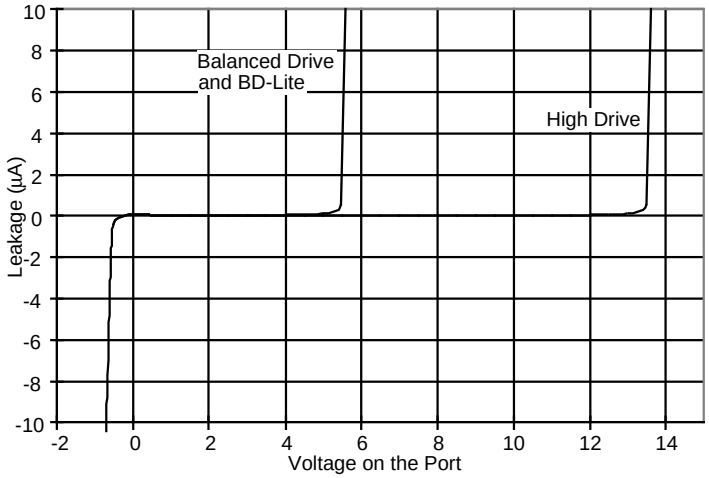

Figure 16, Leakage on an I/O Port in a High Z State

Power-off Disable is possible on any port that allows the pin voltage to rise above Vcc without forward biasing clamp diodes. As seen in Figure 16, High Drive allows the pin voltage to rise above Vcc, giving High Drive the Power-off Disable capability on I/O ports. Balanced Drive and BD-Lite clamp the I/O port to Vcc, limiting the output voltage to Vcc + 0.5V. Therefore Balanced Drive and BD-Lite do not have Power-off Disable capability on their I/O ports.

Connecting Outputs Together

Occasionally in an application where a very strong drive is needed, it is possible to connect two outputs together to double the drive capability of the device as shown in Figure 17. When connecting outputs together certain rules must be followed to prevent potentially damaging the component output structure.

1. The two outputs must be from the same component.
2. The two outputs should be adjacent pins and shorted with a trace between the two pins.
3. The two inputs should be shorted with a trace between the two pins.
4. The two outputs must always have the same state (for instance a counter may toggle state and destroy itself).

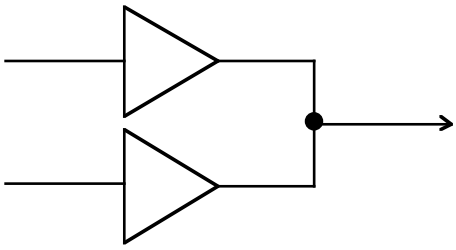

Figure 17, Connecting Outputs Together

When connecting outputs together to achieve higher current levels, care must be taken to not exceed the maximum current level of the component.

Bus Contention

FCT logic cannot be used to perform any type of wire ‘OR’ or ‘AND’ dot functions except when using open drain devices. FCT logic is designed for high performance and has drive levels that are sufficiently strong to cause damage either to the

FCT component or other devices on the bus in the case of sustained bus contention or wire 'OR' operations.

A common system design error is attempting to identify possible bus contention situations by calculating bus timings using "worst case" propagation delays on some components combined with "best case" propagation delays on others. Worst case is found under hot, low Vcc conditions while best case is found under cold, high Vcc conditions. These two conditions are not usually combined in a system, meaning that it is not practical to attempt to calculate system timings using best and worst case conditions within the same timing calculations.

Output disable times are shorter than output enable times in FCT devices, avoiding bus contention when switching with common control signals. In addition, the data book times for both tend to be somewhat lengthy compared to typical delays.

Brief periods of bus contention during switching consisting of a 1 to 2 ns contention during switching should not cause device damage in most cases. During contention the power dissipation will rise to very high levels, possibly causing overheating if the contention is frequent or a significant portion of the duty cycle. Lengthy bus contention of several nsec that may develop from a high speed device such as an FCT being enabled simultaneously with a slow speed device such as an HCT being disabled, may cause device damage.

Comparison with FCT Octals

For completeness, the characteristic pull up and pull down structures of the FCT standard octal components are shown in Figure 18. The Octal High Drive output is very similar to the High Drive Double Density. The Octal Balanced Drive output drive is positioned at a mid point between Double Density Balanced Drive and Double Density BD-Lite. There are no Double Density CMOS rail swing components.

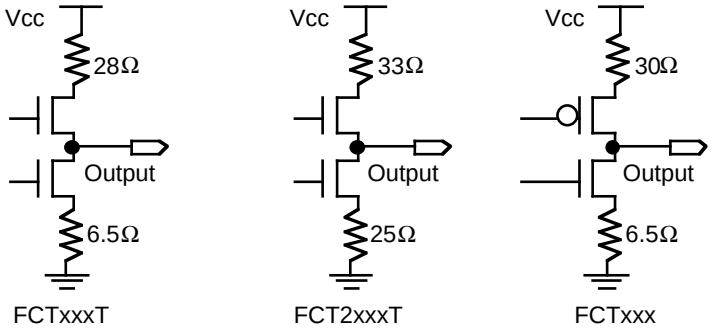

Figure 18, Octal Output Structures

AC Electrical Characteristics

The AC specifications for each component are available in the "SWITCHING CHARACTERISTICS OVER OPERATING RANGE" table in the data sheet for each component. All IDT FCT logic, including Double-Density, Octal TTL, Octal CMOS, and 3.3V come in speed grades which are uniform across all families.

The AC limits of the Double-Density family are specified over the extended commercial (also known as industrial) and military temperature ranges. Vcc tolerance is ±10 % for both commercial and military devices. The limits are based on the worst case operating conditions with Vcc = 4.5V and Ta = 85°C for commercial grade limits and Ta = 125°C for military grade limits. All AC parameters are measured using the industry standard load shown in Figure 19. Propagation delay measurements are taken with the switch open. Enable and disable measurements are taken with the switch closed.

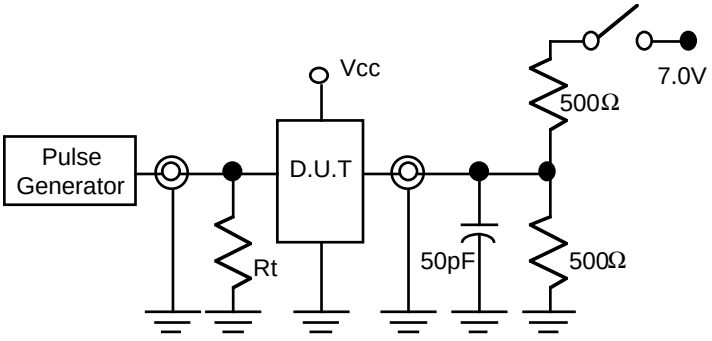

Figure 19, Standard Test Circuit

AC tests are done with a single bit switching and timings may need to be derated for the worst case of 16/18/20-bits switching simultaneously.

Delay as a Function of Supply Voltage

Component propagation delay is sensitive to changes in Vcc. Typically higher Vcc levels will increase component speed and reduce propagation delays.

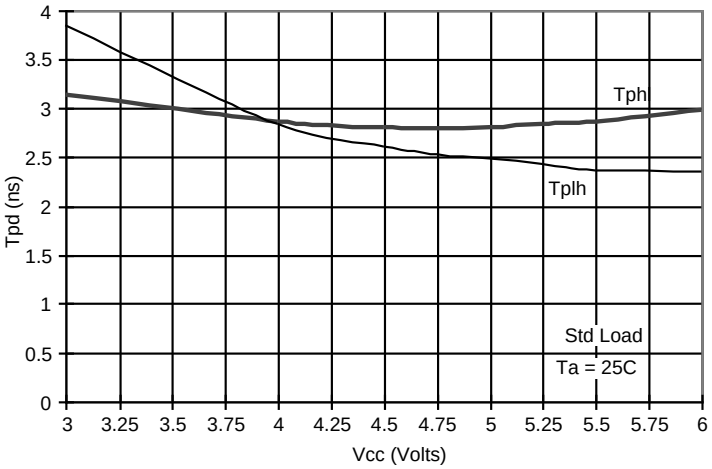

Figure 20, Tpd vs. Vcc (High Drive)

Figure 20 shows the effect of Vcc on the propagation delay of a High Drive component. The propagation delay is fairly linear in the normal operating range, but as Vcc lowers significantly it can be seen that pull up begins to have difficulty achieving the logic high condition.

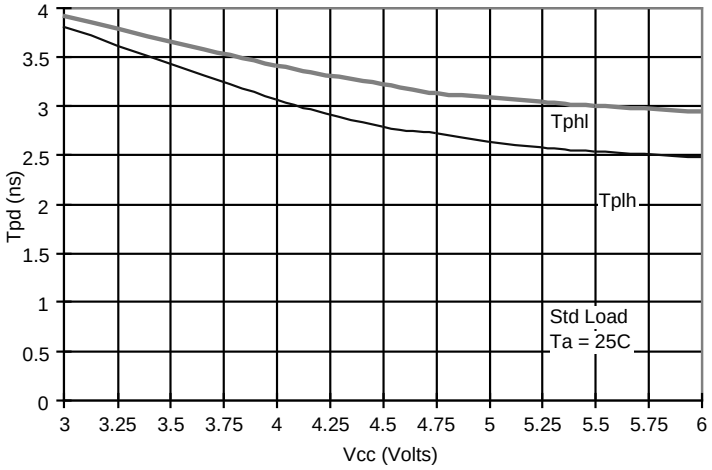

Figure 21, Propagation Delay vs. Vcc (Balanced Drive)

The Balanced Drive of Figure 21 shows excellent stability in the propagation delay relative to changes in Vcc. The Double Density Balanced Drive family from IDT is possibly the best family in the industry for stable, predictable performance under any condition.

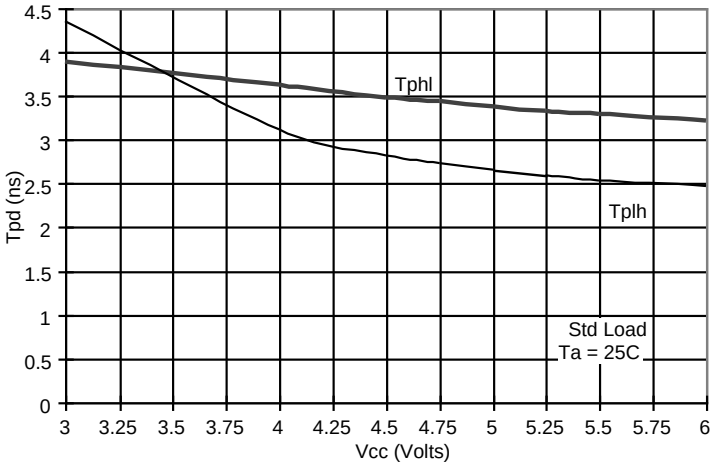

Figure 22, Propagation Delay vs. Vcc (BD-Lite)

The BD-Lite component shown in Figure 22 demonstrates high performance over a wide variety of Vcc levels, despite having a much higher output impedance than either High Drive or Balanced Drive.

Performance Under Temperature

Propagation delay will vary with changes in temperature. Typically these variations are small compared to variations in Vcc, but they are present and do have an effect. As the temperature rises, the propagation delay will increase. As the temperature lowers, the component will demonstrate improved speed performance.

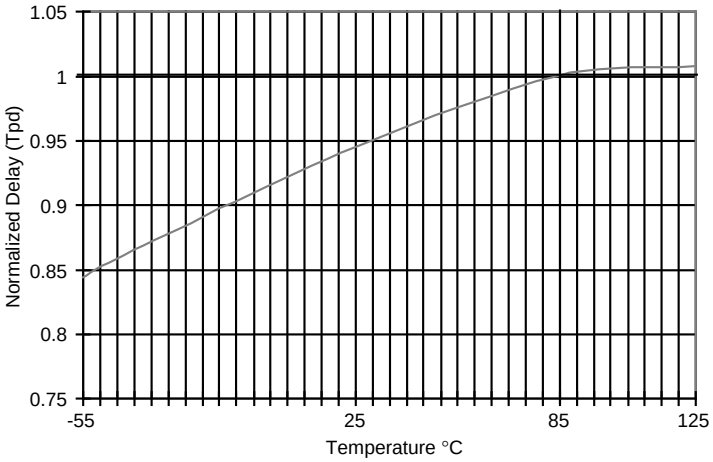

Figure 23, Normalized Delay vs. Temperature

Figure 23 shows how the propagation delay will vary with temperature. The variation is fairly consistent regardless of component family (Balanced Drive, High Drive and BD-Lite).

The data book specifications are guaranteed between -40° and 85°C for all Double Density components except military which have a wider range. To ease calculations, Figure 23 has been normalized to 85°C. The data book limits have been set for testing purposes only and do not imply a failure to operate outside of these ranges. FCT logic will operate easily at -55°C, but may exhibit performance levels faster than the data sheet limits. The maximum temperature of the component die should be 150°C, beyond which component degradation may occur (metal migration). The die temperature will be affected by both the ambient temperature and the component power dissipation. Die temperature can be calculated using the thermal data in section 4 of the IDT Logic Data Book and the POWER SUPPLY CHARACTERISTICS table in each data sheet.

Rise and Fall times

When calculating transmission line effects, it is necessary to know the rise and fall times of the drivers under the intended load. As the load increases, the rise/fall times will increase (slowing the edge), reducing the need for line termination. Wherever possible, BD-Lite or Balanced Drive should be used to avoid the faster, noisier edge rates.

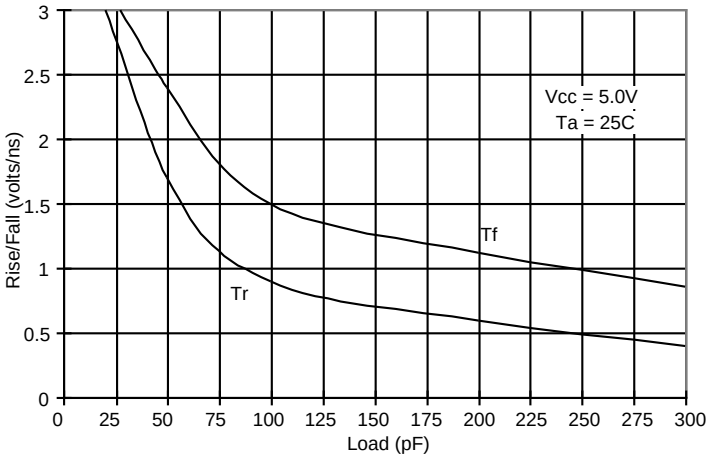

Figure 24, Rise/Fall Time, Hi Drive (FCT16xxxT)

The rise and fall times for a Double Density High Drive component are shown in Figure 24. While theoretically the device will approach infinite slew rate as the load approaches zero, the loading of the component output structure and mounting will prevent reaching zero.

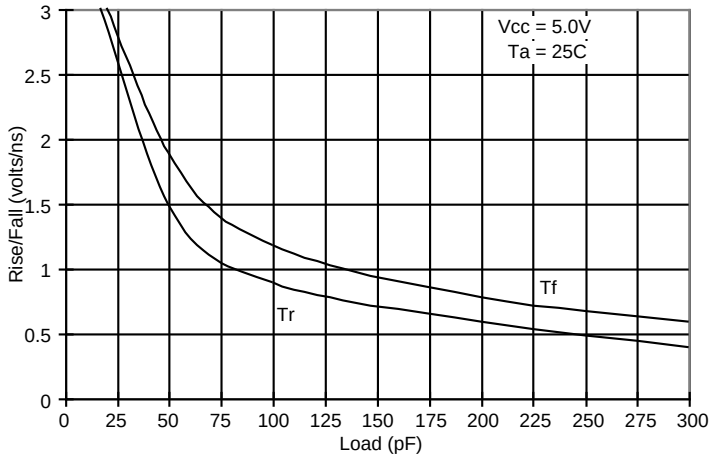

Figure 25, Rise/Fall Balanced Drive (FCT162xxxT)

Figure 25 shows the rise/fall time for a Balanced Drive component. The effect of the additional internal series resistor in the component pull down can be seen as the falling edge is slower under load than for High Drive.

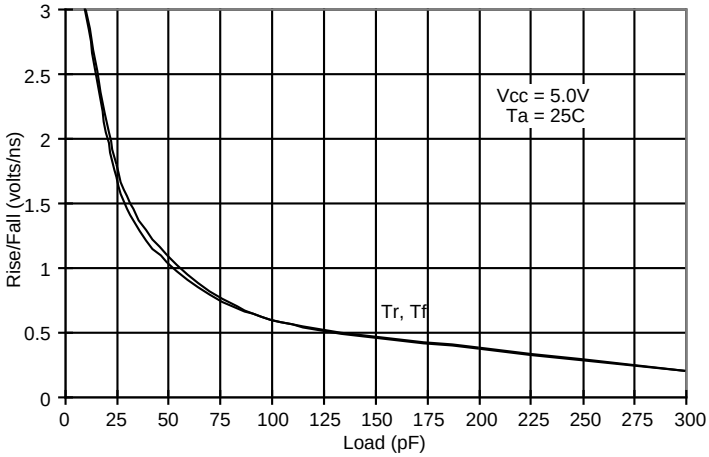

Figure 26, Rise/Fall Time BD-Lite

Figure 26 shows rise and fall times for a Double Density BD-Lite component. The edge rate of BD-Lite is significantly reduced by the higher output impedance of the component. BD-Lite is equivalent to adding a 25Ω series resistor to the output of a High Drive component for the falling edge. The increased impedance slows the drive capability into a capacitive load and slows the edge rate. Since the edge rate for BD-Lite is quite slow, it is rare for BD-Lite to need additional line termination.

In applications where the load is less than 100pF and achieving first incident wave switching in a distributed load is not important, BD-Lite in most applications will give significantly superior low noise performance than either High Drive or Balanced Drive. Integrating the termination resistors into the I/O structure eliminates almost all ground bounce and internal switching noise.

BD-Lite will not overcharge a transmission line and will avoid excessive noise reflections and over/undershoot.

Delay as a Function of Load

Data sheet performance specifications are based on an industry standard load of 50pF and 500Ω, unless otherwise noted. Realistic loads are typically capacitive only (unless DC terminated) and in most cases will be something other than 50pF.

As the load on an output increases, the effective delay through the component will increase. This is primarily because of the increase in the rise and fall time of the device output delaying the time the signal will cross the logic threshold. Secondarily the increased load may exceed the current supplying capacity of the component temporarily, adding additional delay while the load charges.

Figure 27 through Figure 29 show the change in propagation delay as a function of external load. These characteristics are essentially linear and can be extrapolated for heavier loads. Loads above 400pf may draw significant current levels when switching at high frequencies and the designer must be careful not to exceed the maximum power dissipation specifications.

The following examples are for a typical FCT16x244T type component. Other components respond similarly except there may be an additional propagation delay due to the

normal internal delay of the component. The internal delay is not affected by load; therefore, the slope of the line in Figure 27, Figure 28, and Figure 29 will remain constant for all parts of the same drive type, but the t_{PD} intersect point will shift higher or lower according to part type.

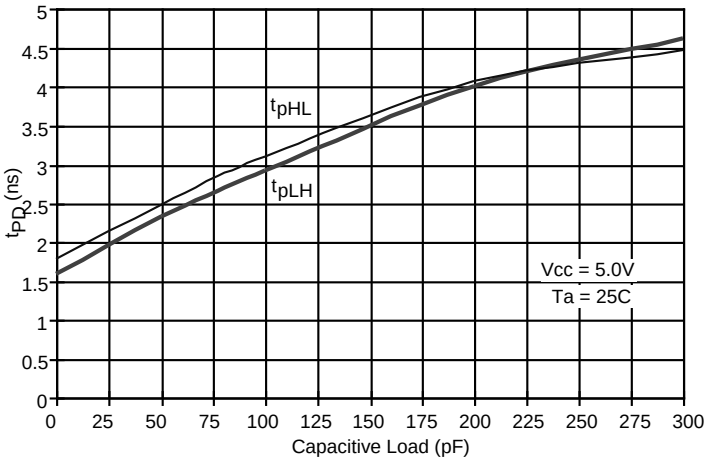

Figure 27, Delay vs. Load High Drive (FCT16244T example)

Figure 27 shows how the effective propagation delay of a High Drive component will increase with an increase in load. The High Drive has a lower output impedance than Balanced Drive and BD-Lite and therefore will be less affected by loading. The derating for High Drive is approximately 1.2ns per 100pF.

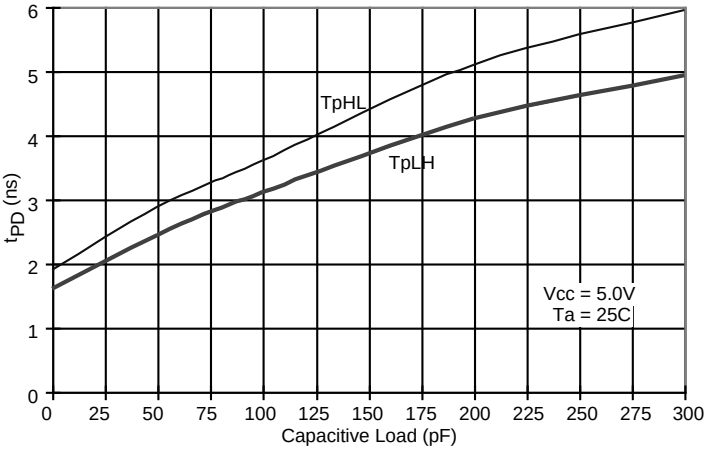

Figure 28, Delay vs. Load Balanced Drive

The Balanced Drive delay as shown in Figure 28 will be more affected by load than High Drive. The increased output impedance of Balanced Drive causes a larger RC time constant, particularly in the LOW to HIGH transition. Because of the longer delay under heavy loads, Balanced Drive is less suited to driving heavy loads than High Drive. The Balanced Drive derating is aproximately 1.5ns per 100pF.

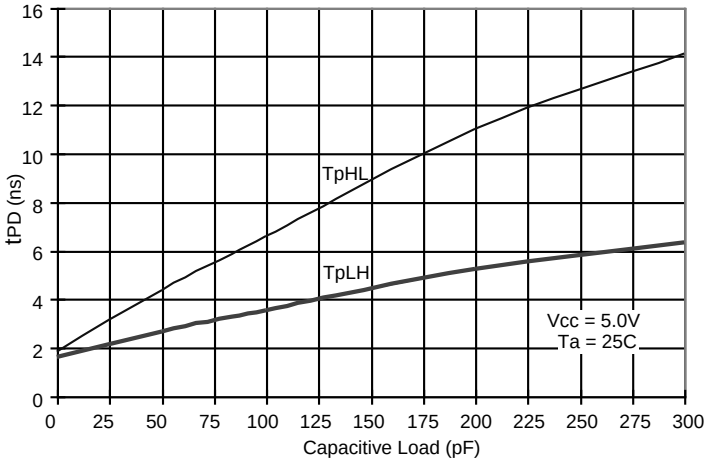

Figure 29, Delay vs. Load BD-Lite Output

The BD-Lite shown in Figure 29 has a higher output impedance than either Balanced Drive or High Drive. The family was designed for point to point line driving or driving light loads. BD-Lite is recommended as an excellent, very quiet family for loads of less than 100pF, but increasing the load beyond 100pF will tend to significantly slow the response of the component. BD-Lite has a higher derating at approximately 4.5ns per 100pF.

Number of Outputs Switching

The number of outputs switching can affect the propagation delay of a component due to the switching currents in the package ground and Vcc leads. Components with lower drive levels will be less affected by this phenomena than higher drive level components. This phoenomena primarily affects octal components due to the use of only one GND and one Vcc pin on the package. The net result of all bits switching in an octal component may be up to a few hundred pico seconds additional propagation delay. Double Density components with eight GNDs and four Vcc pins have multiple routes for current, plus a higher ratio of GND to output pins. The switching speed of double density components will not be significantly affected by multiple outputs switching, especially if the component is a Balanced Drive or BD-Lite.

Output Enables

Figure 30 shows an example of how the enable time of a Balanced Drive component will vary with temperature. A high drive part of the same speed as balanced drive will have almost identical response time in the enable to HIGH direction, but will have a faster response in the enable to LOW direction than shown.

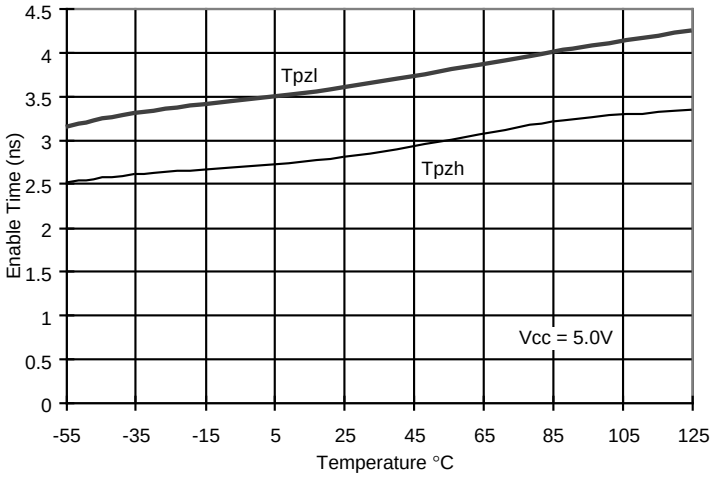

Figure 30, Enable Time vs Temp (FCT162244T)

Disable times will have a variation relative to temperature, the same as shown for Enable times. The slope of the disable curve will be approximately the same as shown in Figure 30 for enable, except the overall delay will be shorter.

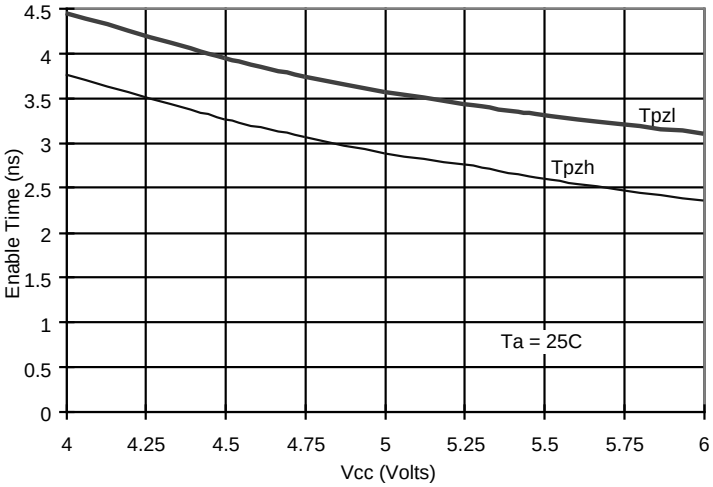

Figure 31, Enable Time vs Vcc (162244T)

BD-Lite enable and disable times will be longer than either High Drive or Balanced Drive. The effect of temperature and Vcc variations on the enable and disable times of BD-Lite will be similar to those shown in Figure 30 and Figure 31 for Balanced Drive with speed increasing at cold temperatures and high Vcc. Speed decreases at hot temperatures and low Vcc.

Setup and Hold Times

In clocked components there is a point at which the data must be stable prior to the clock edge to guarantee that the data is clocked into the register on the clock edge. There is then an input hold time after the clock to guarantee that the clocking is complete and the changing input data will not be clocked into the register.

For most IDT octal registered and latched components, the toggle point where changing input data will be clocked into the register/latch is with the data preceding the clock by about 0.5ns (T_{SU} =0.5ns and T_H = -0.5ns). The toggle point is device specific and will be affected (minimally) by Vcc, temperature and process variations. Generally the data book specifications allow a conservative testing window around the toggle point of 3ns or more (e.g. T_{SU} = 2.0ns, T_H = 1.5ns for an FCT162374CT). For E-speed components, this window is usually much tighter (e.g. T_{SU} = 1.5ns, T_H = 0ns for an FCT162374ET).

Skew

Skew reflects the worst case propagation delay difference between the different outputs. Skew results from design (routing/placement), process and packaging specific to the device.

Because of a lack of legitimate skew specifications, there is a tendency among designers to compute the difference between the maximum and minimum propagation delay specifications and use this number as the worst case skew. This is not a realistic measure of skew because the maximum (worst case) and minimum (best case) delays occur under mutually exclusive conditions of temperature, power supply voltage and process. In order to provide the user with the skew information, Double-Density devices have an output skew specification of 0.5ns maximum between outputs on the same device. There is no tested skew specification between parts, but if a user is concerned about maintaining tight skew tolerances between parts, selecting the fastest speed grades available will provide the tightest skew levels.

Metastability

Metastability is a state that may occur in clocked registers when the input data is transitioning through the input toggle point simultaneously with the clocking of the device. Theoretically, the indeterminate state is clocked into the device. Through the device, indeterminate states are reached and an indeterminate (middle voltage) state is driven to the output. This middle voltage state is held until the device can resolve whether it is going to drive HIGH or LOW. While theoretically it is possible for any component whether it is bipolar, BiCMOS or CMOS to exhibit metastability, the characteristic is pronounced only in very slow, low gain devices.

Because of the high speed nature of FCT logic, metastability is not a problem. The high gain of the input translator will quickly resolve level issues prior to clocking, and any levels not determined at the input will be resolved in the clocking stage.

Undershoot and Overshoot

Undershoot and overshoot in Double Density components can cause false switching, register upset, and device damage if the overshoot/undershoot is excessive. In addition, busses that interface memory devices will likely cause memory upset and data loss if undershoot is excessive.

When viewing undershoot and overshoot with an oscilloscope, the engineer should be aware that adding a scope probe to a device output that is switching may cause an observable undershoot due to the inductive kick of the device bond wire interacting with the capacitive load of the scope probe.

The maximum limitation for undershoot and overshoot is the Absolute Maximum Rating specification for DC Output

Current of -60 to 120 mA, given in all Double Density data sheets. As the voltage drops below the clamp diode voltage of about 0.7V, the current level will increase exponentially. The lead inductance of the component will limit the current for very brief periods, allowing undershoot beyond the clamp voltage. The best way to determine whether an undershoot level or duration is damaging to a component is to use the package parameters found in the SPICE model, and modeling the undershoot to determine the current seen at the die.

As a very crude guideline under transient conditions, the device is expected to withstand an overshoot of 7V or an undershoot of –3V for 20ns regardless of clamp diodes. While the part should not sustain damage from these overshoots and undershoots, it is possible that false switching may occur if there are device inputs sitting at a marginal voltage level or if other marginal conditions exist.

EMI/RFI Problems

EMI and RFI problems are characteristic of very high speed components with fast edge rates that are driving long busses or transmission lines. When developing systems that must maintain low levels of EMI and RFI, reducing the drive level of the high speed components will reduce the noise radiation. Balanced Drive and BD-Lite will radiate less energy and cause less radiated noise than similar families with strong output drivers. Some families that use BiCMOS drivers have output impedances as low as 2Ω which will cause significant radiated noise.

Power Dissipation

FCT-T has the lowest power dissipation of any available logic 5V logic family, making it ideal for low power and battery operated systems that require 5V components. The limiting factor in power dissipation is the component die temperature which should be limited to less than 150°C to avoid metal migration and component damage. The component die temperature is affected by the combined ambient temperature and power dissipation which can be calculated using the thermal data in section 4 of the Logic Data Book and the POWER SUPPLY CHARACTERISTICS in each data sheet (particularly note 6).

Contained within each component data sheet is an ABSOLUTE MAXIMUM RATING for power dissipation. Since the failure causing mechanism is die temperature rather than power dissipation, this specification should be regarded as a guideline only. Using heat sinks or airflow the maximum power dissipation can be increased. Under hot conditions (>70°C) the maximum power may be limited to a level lower than the data book specification. Figure 32 gives approximate values for the amount of power that would need to be dissipated to bring the die to 150°C in various packages with the ambient temperature of 25°C and 70°C in still air with no heat sink.

Package	Description	θja	θjc	PT Ta = 25	PT Ta = 70
SSOP (PV)					
SO48-1	48-Pin SSOP	110	55	1.56W	1.00W
SO56-1	56-Pin SSOP	100	55	1.79W	1.14W
TSSOP (PA)					
SO48-2	48-Pin TSSOP	93	50	1.34W	0.86W
SO56-2	56-Pin TSSOP	84	50	1.49W	0.95W
CERPAK (E)					
E48-1	48-Pin CERPACK	68	12	1.84W	1.18W
E56-1	56-Pin CERPACK	63	11	1.98W	1.27W

Figure 32, Calculated Power for Selected Packages to Bring the Die Temperature to 150°C at 25°C and 70°C Ambient Temperatures

The power dissipation in high speed logic is broken into three separate identifiable sections. The first is component leakage (Icc) which is present whenever the component is powered. The second section is leakage due to floating inputs (ΔIcc). The third section is power dissipation due to device switching (I_{CCD}). In addition to these three, there is also power dissipation due to output loading which must be calculated by the system designer.

PD(unloaded) = Vcc x Ic

Power dissipation in an unloaded device is
where I_C = Total power supply current

$$I_c = I_{cc} + \Delta I_{cc} \times DH \times NT + I_{CCD} \times ND \times f$$

where NT = Number of TTL level inputs
DH = Duty cycle of TTL level input
ND = Number of switching bits
f = Switching Frequency

(1)Icc - Static or quiescent power supply current, specified at Vin = GND or Vcc.

(2) ΔIcc - Power supply current through input translator for TTL level logic high inputs, specified at Vin = 3.4V.

(3)I_{CCD} - Dynamic power supply current due to switching of internal circuitry and outputs.

The total power supply current for unloaded conditions is the sum of these three components.

Leakage Currents (Icc)

IDT Logic has the lowest leakage currents in the industry with typical leakage levels lower than 1μA. This makes these components ideal for battery operation and other very low power applications. When comparing with FAST or other Bipolar families that have very heavy leakage levels, using an FCT family may allow the reduction of system power requirements.

Input Leakage (ΔIcc)

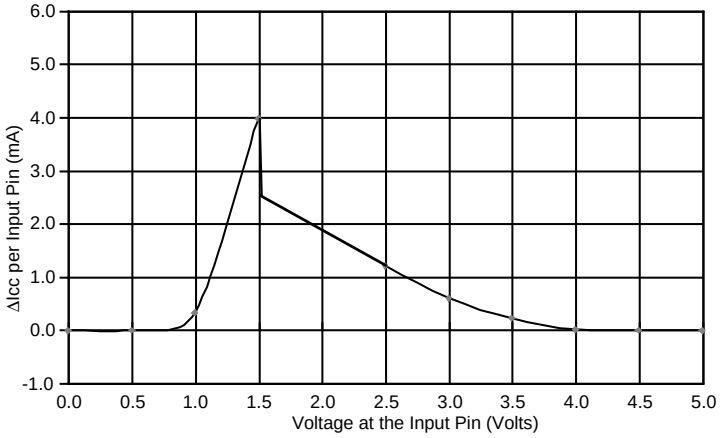

Figure 33, ΔIcc vs. Input Voltage

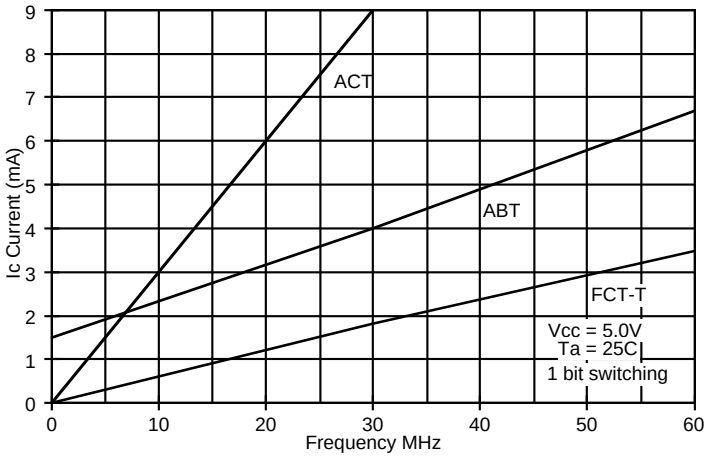

Figure 34, Ic vs. Frequency

Looking at Figure 1, the input structure consists of a P-Channel and an N-Channel FET stacked on top of each other. When device inputs are held at levels other than Vcc or GND, both FETs will partially turn on allowing a leakage directly from Vcc to GND (crossover current). The amount of leakage for a typical device input is shown in Figure 33. In order to maintain low power dissipation, device inputs should always be held either HIGH or LOW at levels away from the areas of high leakage.

Data sheets describe ΔIcc as the current associated with TTL level inputs and specify ΔIcc in mA per input at 3.4V (TTL level). When calculating power dissipation, this parameter is multiplied by the duty cycle high and the number of inputs at 3.4V to arrive at an average current over time that this parameter adds to the total current.

During switching, the input will pass through the threshold causing higher input crossover currents than at steady state, but these currents are part of the dynamic switching currents (Iccd) and should not be added a second time as input leakage.

Dynamic Switching Current (I_{CCD})

The last component is I_{CCD} or the dynamic switching current. This component of current represents the charging and discharging of the internal gate capacitance, crossover currents, and the charging and discharging of the device output drivers with no load. I_{CCD}, which is specified in terms of μA/MHz/bit, is dependent upon the switching frequency and the number of bits switching. IDT's FCT logic has the lowest dynamic switching currents in the industry. These switching currents are lower than any bipolar, BiCMOS, or other CMOS family.

Since I_{CCD} is the internal switching current and is measured in an unloaded state, the three FCT families (High Drive, Balanced Drive, and BD-Lite) all have a similar I_{CCD} of approximately 60μA/MHz for each bit switching. I_{CCD} is not a measure of the switching current caused by the load.

Figure 34 shows the effect of I_{CCD} on Ic for the FCT-T Double Density families and compares the parameter to other available 16 bit families. Bipolar and BiCMOS components (ABT is BiCMOS) will have a DC offset due to the leakage currents when the outputs are low. CMOS components like FCT and ACT have negligible leakage levels.

The output drivers of a device are responsible for a large portion of the dynamic power dissipation. If a device is being switched with the output drivers disabled (3-state), I_{CCD} will be significantly reduced.

The standard method of measuring switching current is by measuring Ic (current entering the Vcc pins) while toggling one input and one output only. To avoid driving a board pad capacitance or radiating energy from a loose pin, the switching output pin is cut off. All other inputs are tied to Vcc or GND.

Some manufacturers specify C_{PD} or dynamic power dissipation capacitance which can be used to calculate I_{CCD} as follows:

$$I_{CCD} \text{ (in } \mu A/MHz/bit) = C_{PD} * Vcc$$

Many manufacturers do not specify switching current in any form, making accurate power calculations impossible with their components.

Current Due to Loading

Adding loading to the output of a component will increase the current flowing into the power power pin of the device. Most of this current will flow directly from the output into the load, causing power dissipation in the load. Any voltage drop between Vcc and Voh or GND and Vol will cause additional power dissipation within the component. This power dissipation is dependent upon the characteristics of the load.

Figure 35 gives an example of how the current through the Vcc of the device will increase over frequency under a 50pF load on one pin. The power from the increased current will be dissipated partially in the driving component and partially in the load.

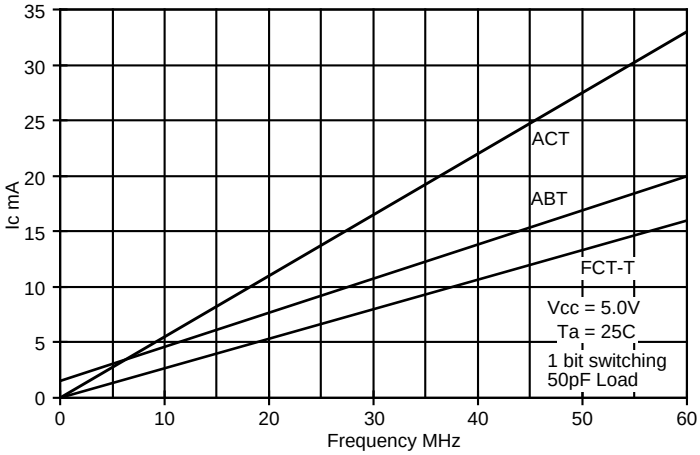

Figure 35, Supply Current under Load

CONCLUSIONS

FCT Logic provides both performance and flexibility which is unequaled in the industry today. In addition to the high performance and low power dissipation which is common to all FCT families, there is a variety of choices, allowing the designer to adapt the component to his application. Through component selection FCT logic is capable of driving everything from a heavy backplane to a very lightly loaded quiet point to point signal. Speed grade selections allow a designer a cost/performance tradeoff, all within the same logic family. These benefits combine to make FCT the most widely used, universal, high performance family.