PLL LOCK INDICATOR

APPLICATION NOTE AN-237

INTRODUCTION

A PLL lock detector is implemented on the following device families: TurboClockII, TurboClockII Plus, TeraClock and Programmable Clock. The output of the lock detector is available on the LOCK pin. The lock circuitry monitors the phase difference between the reference clock REF and the feedback clock FB. The lock signal indicates "Lock", when the clocks REF and FB are phase locked. It is possible for excessive jitter to cause a loss-of-lock indication, even if REF and FB are locked and no system-level errors (i.e. bit errors) are occurring. This application note will describe in detail the operation of the lock detector circuit and provide recommendations to avoid such false loss-of-lock indications caused by excessive jitter.

DESCRIPTION OF LOCK DETECT FLOW CHART

The lock detector can be simplified down to three counters: LCount (lock count), ULCount (unlock count), and ULWindow (observation window). The state transition diagram is shown in figure 1, next page. LCount and ULwindows are clocked by REF. LCount resets to zero when it reaches its maximum count (i.e. 512 for the 5T2010) or if there is a cycle for which $\Delta\phi$ > tlockϕ. ULWindow resets when it reaches its maximum count (i.e. 256 for 5T2010). ULCount resets when ULWindow resets. ULCount is incremented for every REF cycle for which $\Delta\phi$ > tlockϕ. If LCount reaches its final value then LOCK is asserted. If ULCount reaches its maximum value, LOCK is de-asserted.

The PLL is defined as locked (LOCK output pin is asserted) if the phase difference between the reference clock REF and the feedback clock FB ($\Delta\phi$) is less than a predefined value (tlockϕ) for LCount consecutive clock cycles. It is defined as out-of-lock (LOCK output pin is de-asserted) if there are more than ULCount occurrences where $\Delta\phi$ > tlockϕ within ULWindow consecutive clock cycles. The values of these three counters and tlockϕ are shown in the Phase Difference table below. Note that this is not a sliding window of 'ULWindow' consecutive cycles. At the start of a new ULWindow consecutive cycle window, the ULCount starts from zero (see figure 2).

PHASE DIFFERENCE VALUES

Device Part Number	tlockϕ (ps)	LCount (max)	ULCount (max)	ULWindow
TurboClockII: 5V995/5T995/5V9955/5T9955	2.3ns	128	1	128
TurboClockII Plus: 5V996	540ps	512	4	256
TeraClock: 5T9010/5T9110/5T2010/5T2110	540ps	512	4	256
Programmable Clock: 5T9890/5T9891/5T9820/5T9821	540ps	512	4	256

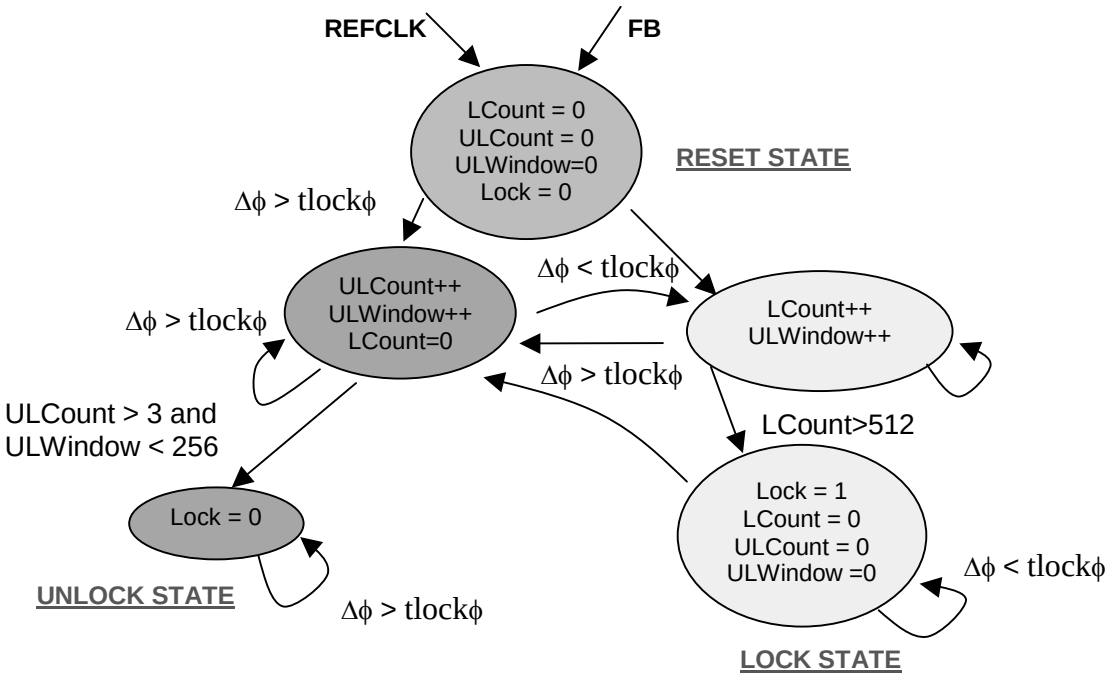

Figure 1: Lock Detector State Transition Diagram

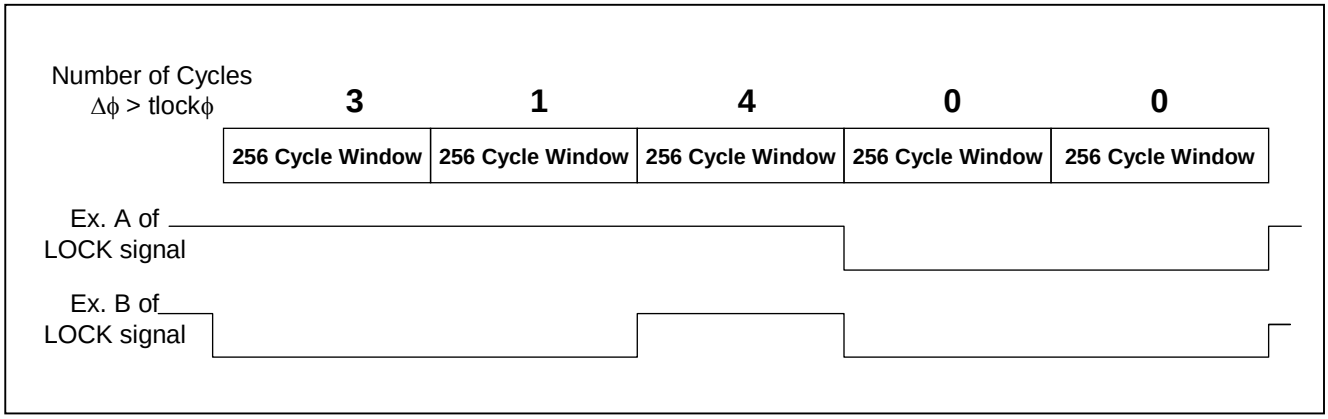

Figure 2: Example of Lock Pulse Width

APPLICATION EXAMPLES AND TEST RESULTS

Phase jitter tjit (ϕ) (shown in figure 3) is the deviation in t(ϕ) for a controlled edge with respect to a t(ϕ)mean in a random sample of cycles in accordance to the Jedec spec 65A.

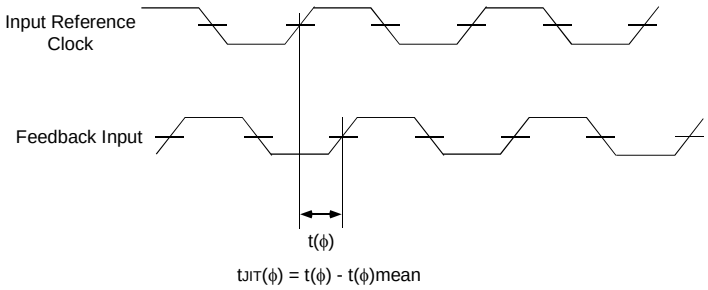

Figure 3: Phase Jitter

t(ϕ) is a random sample
t(ϕ)mean is the average of sample and cycles measured on the controlled edges.
tjit(ϕ) = | t(ϕ) - t(ϕ)mean |

In a real system, excessive phase jitter can be due to poor phase noise in the PLL and/or noise on the power supply. The propagation delay variation caused by the power supply noise in the clock buffer will add to the instantaneous phase shift on the feedback pin of the PLL.

Figure 4 shows a bench setup used to look at the possible effects of jitter on the LOCK pin. The 19.66MHz output of a SMY02 signal generator was used as reference clock for the IDT5T2010. The IDT5T2010 was a 2.5V zero delay buffer that could multiply the frequency by 1-6, 8, 10, or 12, and had 3.3V tolerant inputs. The IDT5T2010 was configured to multiply a 19.66MHz clock input by 3 to generate a 58.98MHz output. Since the input clock was 19.66MHz, 512 cycles equaled 26us.

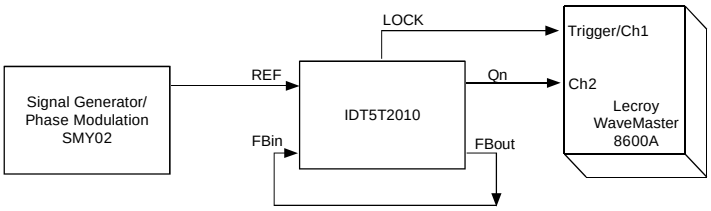

Figure 4: Lab Experiment Setup

In order to be able to control the amount of phase noise injected into the clock inputs, a signal generator with phase modulation capabilities was used as the reference clock input in this test. The test setup was used for exercising and observing the LOCK pin behavior. The frequency was set to 19.66MHz with phase modulation from 0 to 2 radians. The part was set to multiply the input frequency by 3 to generate 58.98MHz outputs. The Lecroy Oscilloscope was triggered off the LOCK pin.

The outputs of the LOCK pin with increasing amount of phase modulation are shown in the scope screenshots (figures 5 to 8). The results are summarized in the Test Results table below. The LOCK output is always high when there is less than 0.2 radian or 1.6 ns phase modulated at 19.66MHz. With .5 radian or more of phase modulated at the reference clock REF, the LOCK output went low for 26us (or 512 Ref clock cycles) at 19.66MHz and then came back high, even though the output is still in locked condition (as shown in figure 6). It's important to note that the exact amount of time that LOCK remains low due to excessive phase noise is completely random. Experimentation showed that it tended to go low for 26us, but occasionally it went low for 52us.

TEST RESULTS

Ref Clk Cycle	Input Phase Modulation	Equivalent Phase Shift	Lock Indicator Level
51 ns	0.2 rad	1.62ns	HIGH
51 ns	0.5 rad	4.06ns	HIGH-LOW; LOW cycle ~ 26 us (approximately of 512*51ns)
51 ns	1.0 rad	8.12ns	HIGH-LOW; LOW cycle ~ 26 us (approximately of 512*51ns)
51 ns	1.6 rad	12.99ns	Switching HIGH-LOW-HIGH
51 ns	2.0	16.24ns	LOW

If the LOCK pin is to be employed as an indication of excessive phase jitter, it can be used as-is. However, to use the LOCK pin as an indication of frequency lock, or some gross clock problem, a glitch filter should be implemented to avoid the false loss-of-lock indication caused by jitter. The glitch filter can be constructed to filter out pulses of the desired duration on the LOCK pin. As seen in the example above, phase noise of greater than 0.2 radians will cause the LOCK pin to temporarily go low for a minimum of 26us. A glitch filter can ignore such temporary LOCK pin conditions. Depending on the desired use of the LOCK pin, the designer can use this filter to adjust the minimum pulse width of LOCK that will be considered as a valid indication of loss-of-lock.

For example, if the goal is to use the LOCK signal as an indication of catastrophic failure, the LOCK will need to go low and stay low for a long time, perhaps permanently. In this case, the glitch filter needs to be designed to ignore LOCK unless it's low for a long time. If the goal is to use the LOCK signal as an indication of potential system failure in the near future, then the glitch filter can be set to ignore LOCK unless it's low for a "sufficient" amount of time (such as 100us). Examining the rate that LOCK is going between low and high states can further diagnose unstable system operation. The exact implementation is up to the system designer. Below is a Verilog implementation of a simple glitch filter. Note the counter values in there are just place holders. The exact value will depend on the goal of the glitch filter.

```
module filter (clock, resetx, lock_from_PLL, system_PLL_lock);

 input clock,resetx,lock_from_PLL;

 output system_PLL_lock;

  reg    system_PLL_lock;

 integer count;

 always @(posedge clock)
   begin

        if (resetx)
          begin
            case (lock_from_PLL)
             0: // glitch filter of 512 cycles with the lock_from_PLL being low
                        begin
                          count=count+1;
                          if(count==512)
                            begin
                                    system_PLL_lock=0;
                                    count=0;
                            end
                        end
              1: // lock_from_PLL is high, assert the system_PLL_lock on this cycle, reset filter
                        begin
                          system_PLL_lock=1;
                           count=0;
                        end
            endcase // case(lock_from_PLL)
          end // if (resetx)

        // synchronous reset
        else
          begin
            system_PLL_lock=0;
             count=0;
          end // else: !if(resetx)

    end // always @ (posedge clock)
endmodule // filter
```

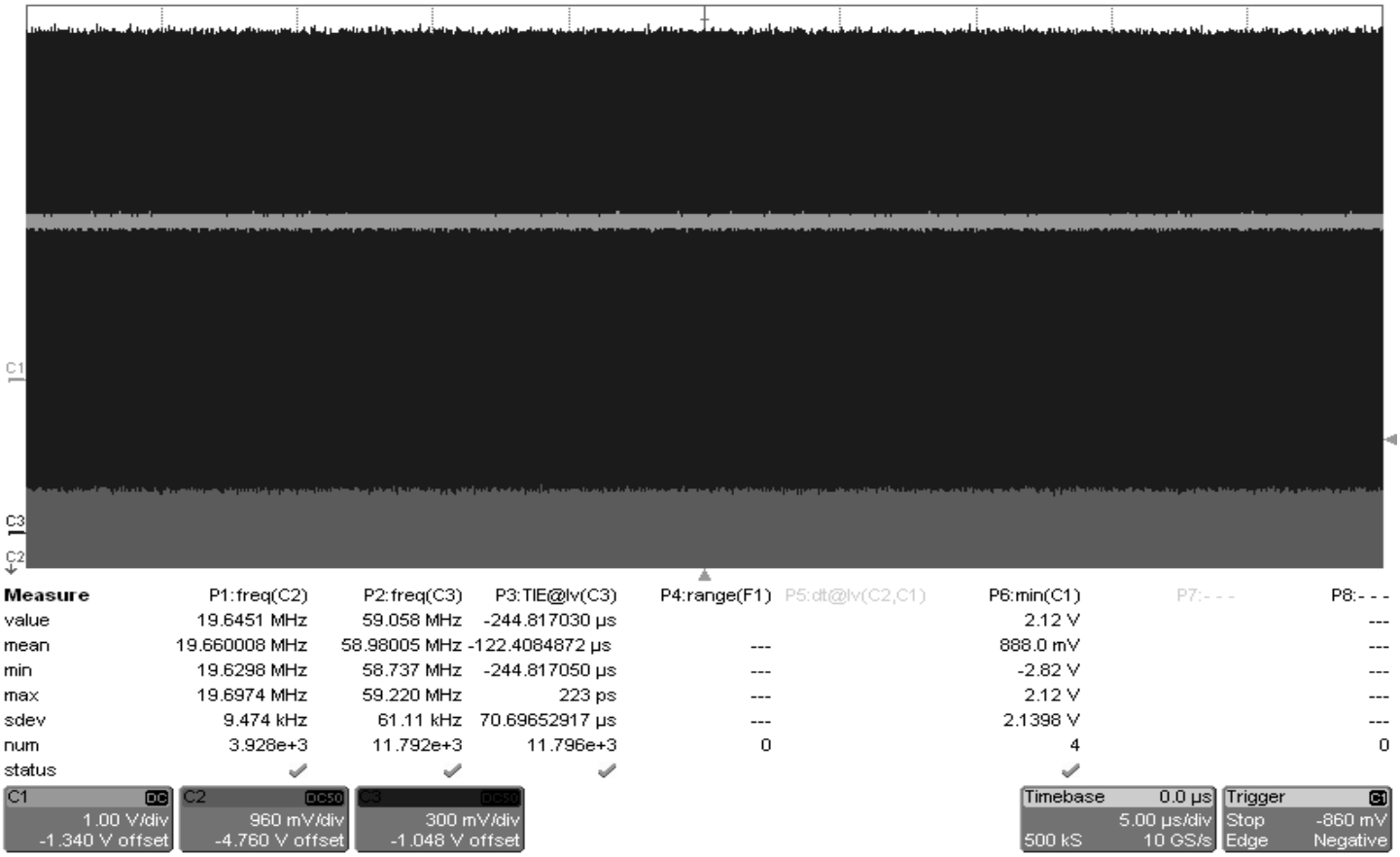

Figure 5: IDT5T2010 Lock detect pin test with 0.2 rad phase modulation

IDT5T2010
Channel 1 = LOCK Signal
Channel 2 = Ref Clk = 19.66MHz (51ns period)
Channel 3 = Output = 58.98MHz
Phase modulation: 0.2 rad or ~ 1.62ns phase shift
Lock detect Pin = Hi
Test time = 3 hours

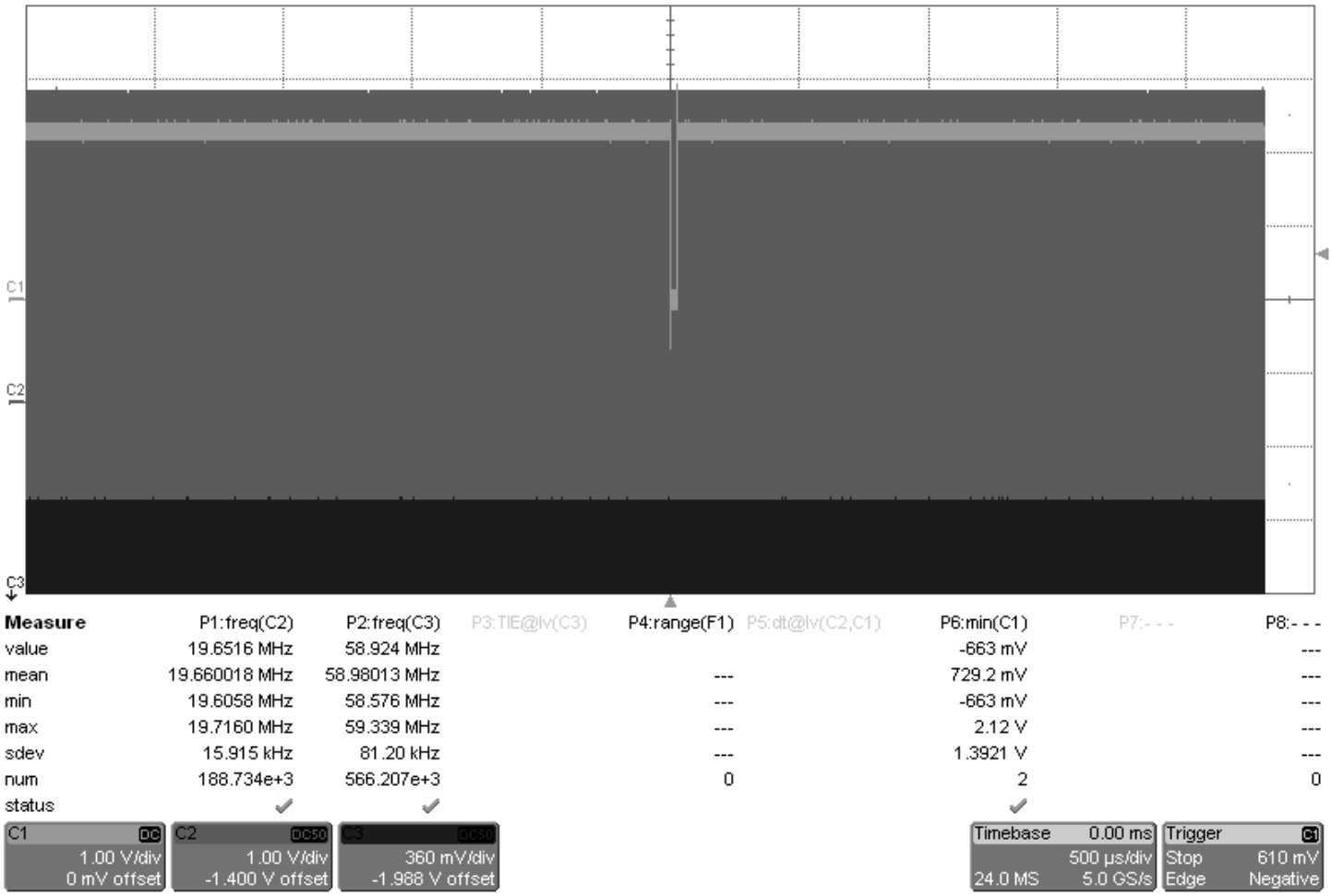

Figure 6: IDT5T2010 Lock detect pin test with 0.5 rad phase modulation

IDT5T2010
Channel 1 = LOCK signal
Channel 2 = Ref Clk = 19.66MHz (51ns period)
Channel 3 = Output = 58.98MHz
Phase modulation: 0.5 rad or ~ 4.06ns phase shift
Lock detect Pin = Hi-to-Low, Low cycle ~ 26 us (approx of 512*51ns).
Test time = 1 hours

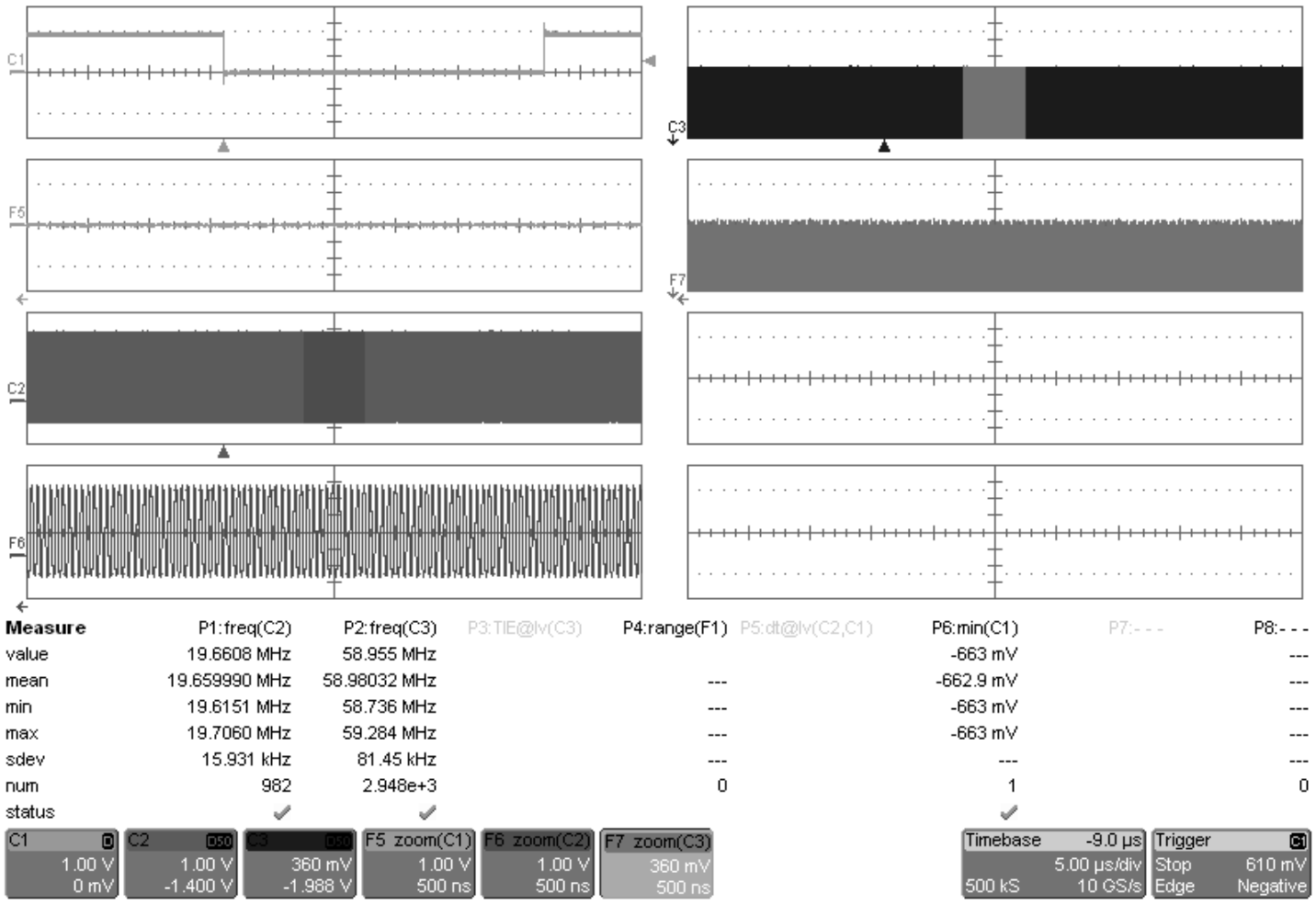

Figure 7: IDT5T2010 Lock detect pin test with 0.5 rad phase modulation

IDT5T2010
Channel 2 = Ref Clk = 19.66MHz (51ns period)
Channel 3 = Output = 58.98MHz
Phase modulation: 0.5 rad or ~ 4.06ns phase shift
Lock detect Pin = Hi-to-Low ,
Channel 1 = Zoom in of Low cycle ~ 26 us (approx of 512*51ns).
Test time = 1 hours

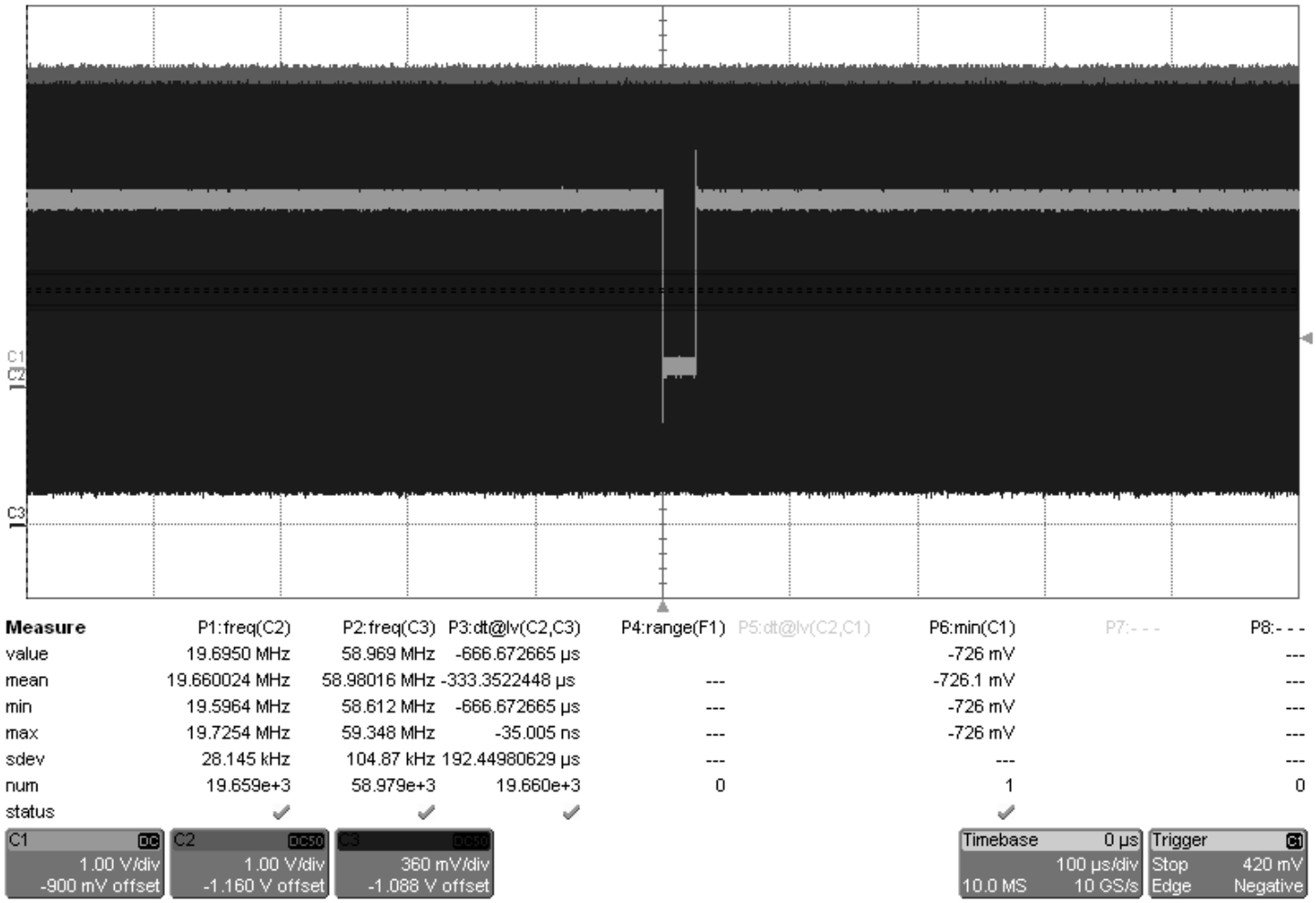

Figure 8: IDT5T2010 Lock detect pin test with 1.0 rad phase modulation

IDT5T2010
Channel 1 = LOCK signal
Channel 2 = Ref Clk = 19.66MHz (51ns period)
Channel 3 = Output = 58.98MHz
Phase modulation: 1.0 rad
Lock detect Pin = Hi-to-Low, Low cycle ~ 26 us (approx of 512*51ns).
Test time = 1 hours

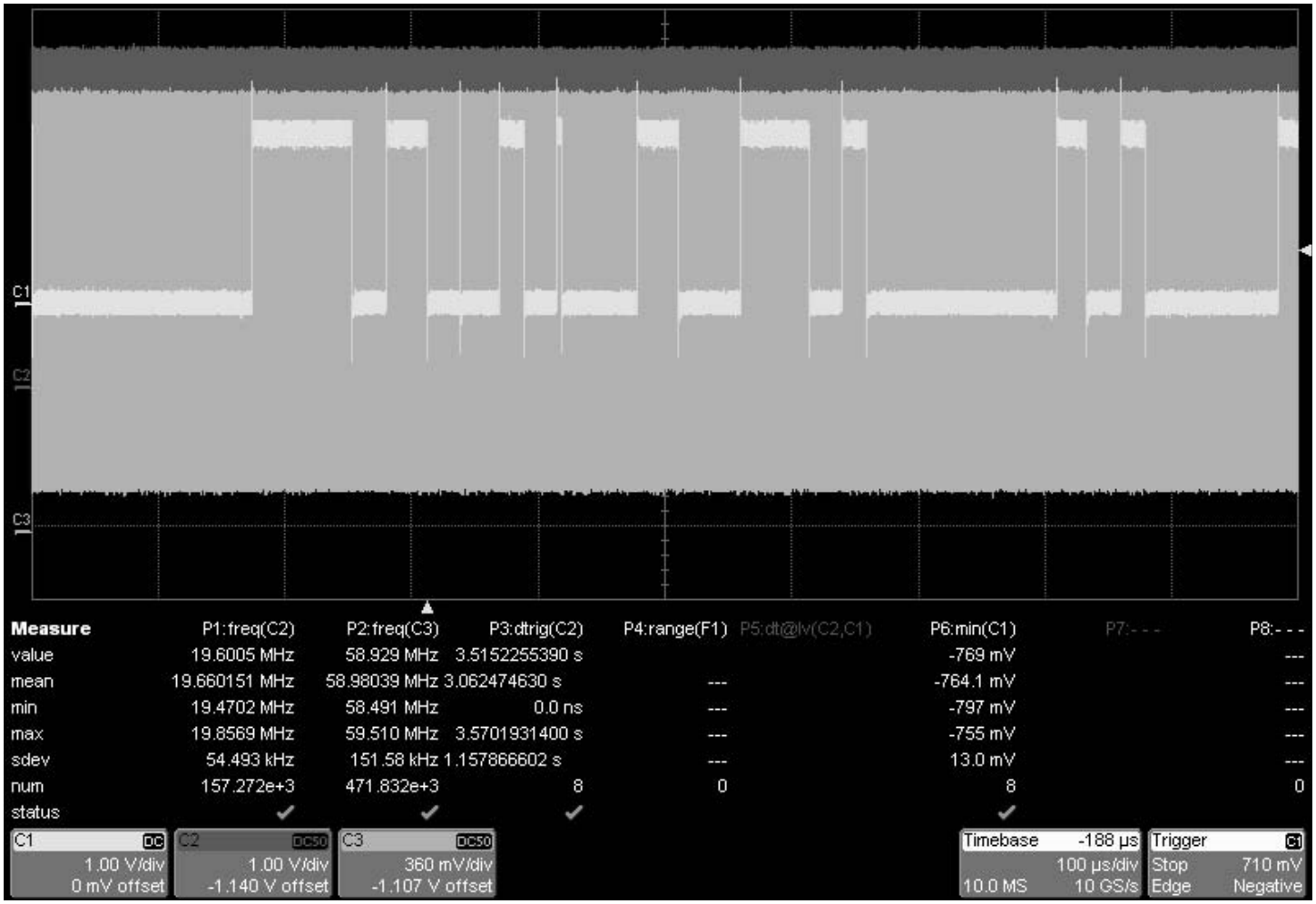

Figure 9: IDT5T2010 Lock detect pin test with 1.6 rad phase modulation

IDT5T2010
Channel 1 = LOCK signal
Channel 2 = Ref Clk = 19.66MHz (51ns period)
Channel 3 = Output = 58.98MHz
Phase modulation: 1.6 rad
Lock detect Pin = Hi-to-Low
Lock Detect pin start failing at cycle > 26us

SUMMARY:

1. The lock detector is sensitive to high jitter. It was implemented as a phase lock detector and not as a frequency lock detector. As figure 8 shows, excessive jitter (more than .2UI) will cause the lock detector to switch rapidly between the HIGH and LOW states. Without external qualification, the LOCK signal should only be used as an indication of jitter in the system, not as an indication of failure.

2. A glitch filter will eliminate this sensitivity to phase and jitter. Increasing the width of the glitch filter will cause the LOCK signal to behave more like a frequency lock rather than phase lock indicator.

3. Figure 8 shows a "glitch low" on the LOCK signal of about 200us. Note that 12ns of jitter on a 19.66MHz clock is highly unusual. For a frequency lock detector, use as wide a glitch filter as feasible.

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