



1 Introduction

The IDT82V2048 and IDT82V2058 offer several operating modes to suit the many possible design and applications for these LIUs. One of these modes, Hardware Mode will be discussed in this paper. Some functions that are available in Host Control Mode may not be available or may function differently in Hardware Control Mode. Where there are operational differences, these will be noted in the text.

Hardware Control Mode offers the advantage of a lower cost solution and saving of board space. These advantages are realized because a

microprocessor is not required for configuration, thus saving cost and board space. Additional space saving is realized because the signal traces between the microprocessor and LIU are not present.

Hardware Control Mode is achieved by the correct setting of certain multi-function control pins. During power-up or reset, the LIU detects the conditions on the pins and self-configures to operate in the desired mode. The pins involved in Hardware Control Mode configuration are indicated in [Table-1](#).

Table-1

| Signal Name | Pin No. | | Description |
|-------------|---------|--------|--|
| | QFP144 | BGA160 | |
| MODE2 | 11 | E2 | L = Select Hardware Control Mode |
| MODE1 | 43 | K2 | Ground for Hardware Control Mode |
| CODE | 88 | H12 | L = B8ZS (T1) / HDB3 (E1); H = AMI for all channels |
| JAS | 87 | J11 | Determines Jitter Attenuator (JA) Configuration, see Table-2 . |
| TS2 | 86 | J12 | T1 transmit template select, see Table-3 (In 2058, this pin is connected to ground in hardware control mode.) |
| TS1 | 85 | J13 | T1 transmit template select, see Table-3 (In 2058, this pin is connected to ground in hardware control mode.) |
| TS0 | 84 | J14 | T1 transmit template select, see Table-3 (In 2058, this pin is connected to ground in hardware control mode.) |
| LP7 | 28 | K1 | Configures Channel 7 to loopback according to Table-4 |
| LP6 | 27 | J1 | Configures Channel 6 to loopback according to Table-4 |
| LP5 | 26 | J2 | Configures Channel 5 to loopback according to Table-4 |
| LP4 | 25 | J3 | Configures Channel 4 to loopback according to Table-4 |
| LP3 | 24 | J4 | Configures Channel 3 to loopback according to Table-4 |
| LP2 | 23 | H2 | Configures Channel 2 to loopback according to Table-4 |
| LP1 | 22 | H3 | Configures Channel 1 to loopback according to Table-4 |
| LP0 | 21 | G2 | Configures Channel 0 to loopback according to Table-4 |
| OE | 114 | E14 | L sets all TTIPn/TRINGn to high impedance state |
| CLKE | 115 | E13 | Selects active edge of RCLKn and SCLK; sets active level of RDPn/RDNn |
| A4 | 12 | F4 | Set to GND for Hardware Control mode |
| MC3 | 13 | F3 | Selects Monitor Configuration (see Table-5) |
| MC2 | 14 | F2 | Selects Monitor Configuration (see Table-5) |
| MC1 | 15 | F1 | Selects Monitor Configuration (see Table-5) |
| MC0 | 16 | G3 | Selects Monitor Configuration (see Table-5) |

Table-2

| JAS | Jitter Attenuator (JA) Configuration |
|---------|--------------------------------------|
| L | JA in transmit path |
| VDDIO/2 | JA not used |
| H | JA in receive path |

Table-3 Built-In Waveform Template Selection (only for 2048)

| TS2 | TS1 | TS0 | Mode | Cable Length | Maximum Cable Loss (dB) |
|-----|-----|-----|----------|---------------------------------|-------------------------|
| 0 | 0 | 0 | E1 | 75 Ω /120 Ω cable | - |
| 0 | 0 | 1 | Reserved | | |
| 0 | 1 | 0 | Reserved | | |
| 0 | 1 | 1 | T1 | 0 – 133ft. ABAM | 0.6 |
| 1 | 0 | 0 | | 133 – 266ft. ABAM | 1.2 |
| 1 | 0 | 1 | | 266 – 399ft. ABAM | 1.8 |
| 1 | 1 | 0 | | 399 – 533ft. ABAM | 2.4 |
| 1 | 1 | 1 | | 533 – 655ft. ABAM | 3.0 |

Table-4

| LPn | Loopback Configuration |
|---------|------------------------|
| L | Remote Loopback |
| VDDIO/2 | No Loopback |
| H | Analog Loopback |

Table-5

| MC[3:0] | Monitor Configuration |
|---------|----------------------------------|
| 0000 | Normal operation – No monitoring |
| 0001 | Monitor Receiver 1 |
| 0010 | Monitor Receiver 2 |
| 0011 | Monitor Receiver 3 |
| 0100 | Monitor Receiver 4 |
| 0101 | Monitor Receiver 5 |
| 0110 | Monitor Receiver 6 |
| 0111 | Monitor Receiver 7 |
| 1000 | Normal operation – No monitoring |
| 1001 | Monitor Transmitter 1 |
| 1010 | Monitor Transmitter 2 |
| 1011 | Monitor Transmitter 3 |
| 1100 | Monitor Transmitter 4 |
| 1101 | Monitor Transmitter 5 |
| 1110 | Monitor Transmitter 6 |
| 1111 | Monitor Transmitter 7 |

2 Operation:

1. Set MODE2 to logic Low to place the IDT82V2048/2058 into Hardware Control Mode.
2. Select either Single Rail or Dual Rail mode for the system side interface (see page 5 of the data sheet for specific instructions).
3. Select the Line Code Rule (AMI/B8ZS/HDB3) by setting the appropriate value on the CODE pin.
4. Set the active edge of RCLK with the CLKE pin.
5. Set the output drivers to high impedance or normal mode with the OE pin.
6. Select the waveform template using TS[2:0] according to [Table-3](#).
7. Set A4 to GND and choose the monitor configuration according to MC[4:0] and [Table-5](#).
8. Choose the Transmit Clock mode according to the pin descriptions on page 5 of the data sheet. This permits the selection between normal mode, TAO, or power down per channel.
9. Optionally select Loopback mode by setting the LPn pins according to [Table-4](#) (Note that Digital Loopback is not available in Hardware Control mode).
10. The JAS pin selects the JA (jitter attenuator) mode according to [Table-2](#).

Note, since Hardware Control Mode does not permit register access, there is no way to access the extended operating modes of the 2048/2058 controlled by the Expanded (indirect) registers.