

Introduction

This application note will discuss some of the key parameters, measurements and concerns regarding the drive level specification, which is typically called high driving the crystal. With the advancement in quartz crystal technology, both the packages and the internal crystal blanks have continued to migrate to smaller sizes. This reduction in crystal blanks has led to the reduction in the drive level capability and datasheet specification of many of the crystal manufactures. In the past, the standard package was HC49 which can handle a relatively large crystal blank with a common maximum drive level specification of 1mW. At the present time, surface mount crystal packages are as small as 1.6mm x 1.2mm which commonly specifies a 100uW maximum and 10uW typical for drive level.

This reduction in drive level has produced contrasting interest between the crystal manufactures and the silicon circuit designers who design phase lock loops (PLL's) devices with integrated crystal oscillators. The circuit designers want to operate the crystal oscillator at relatively high drive levels for best phase noise performance. This is accomplished by maximizing the clock voltage across the crystal relative to the oscillator noise spectral density at the clock frequency. In contrast, the crystal manufactures are reducing the blank size in order to minimize the amount of quartz material used. This inherently reduces the drive level specifications. In addition, crystal manufactures are using the smaller blanks and retrofitting them into larger packages like HC49. This has created issues in finding crystal manufactures with higher drive level specifications especially for Legacy designs which many times are being forced to use lower drive level rated crystals. In many applications, lower drive level crystal can be used, but special attention must be given to some key parameters.

Crystal drive level is the amount of power dissipated in a crystal. It can be calculated by measuring the excitation current flowing through the crystal blank. It can affect, among others, the motional resistance, resonance frequency and phase-noise of the crystal. As the excitation current through the crystal increases, the drive level and the amplitude of crystals vibration also increase, causing changes in both the resistance and frequency.

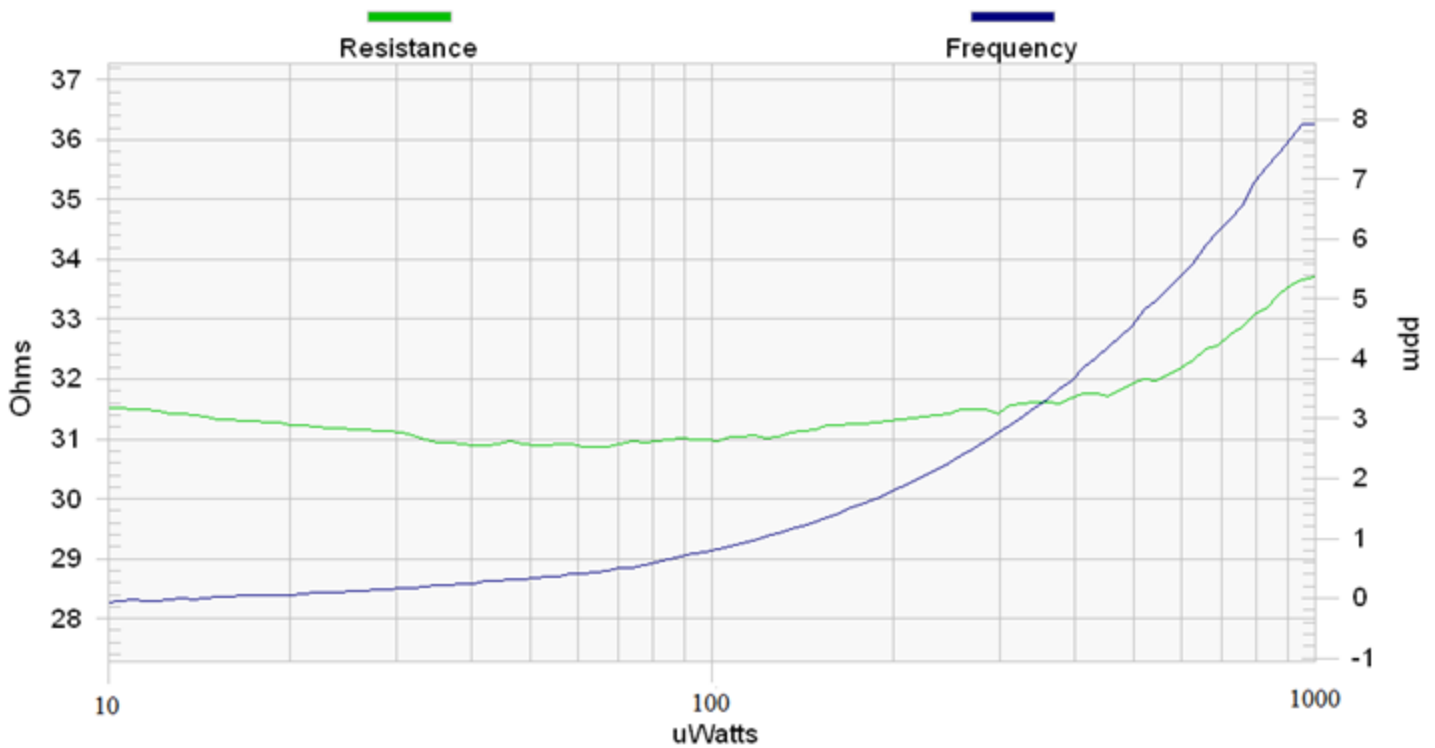
A simple analysis in sweeping the drive level can be performed to verify changes in both resistance and frequency of the crystal. This analysis, typically called Drive Level Dependence (DLD), can be taken using a Saunders & Associates (S&A) 250B/C desktop network analyzer. Refer to figure 1. S&A manufacturers test and production systems for quartz crystals, oscillators, filters, and components. It has become an industry standard and preferred test system by many of the leading crystal manufactures. This desktop system is relatively inexpensive and is essential if designing or using silicon component, which require quartz crystals.

Figure 1. 250B/C Network Analyzer



DLD Sweep

Figure 2. DLD Sweep Result



The DLD sweep in figure 2 shows the effect of both the motional resistance and frequency shift for a drive level between $10\mu\text{W}$ and $1000\mu\text{W}$. The left side Y axis is the motional resistance and the right side the PPM variation with the x axis being the drive level. This DLD sweep was done at room temperature.

Crystal Drive Level and Power Dissipation Example

The internal oscillator of an IDT clock synthesizer is to be used with an external crystal. A particular crystal is to be used and the compatibility of the crystal drive level with the current provided by the IDT oscillator must be checked.

Consider the crystal to have the following specifications:

Table 1. Specification of Quartz Crystal Units

No.	Description	Contents
1	Nominal frequency (Fn)	27.000MHz
2	Holder type	SX-1 T/R
3	Mode of oscillation	Fundamental (AT)
4	Storage temperature range	-40°C to +85°C
5	Frequency calibration	±0.003% (±30ppm)
6	Frequency drift in operating temperature range (0°C to 50°C)	±0.003% (±30ppm)
7	Equivalent resistance (C.I.)	40 ohms max.
8	Load capacitance (C _L)	20pF
9	Drive level (D/L)	100
10	Test impedance meter	SAUNDERS 250A
11	Shunt capacitance (C ₀)	7.0 max. pF
12	Insulation resistance	500 MegaOhm min. / DC 100V
13	Aging rate a year	±0.0003%

From the above specifications it can be seen that the crystal is a 27 MHz Fundamental mode AT cut crystal. The recommended load capacitance is 20pF and the maximum drive level is specified to be 100uW.

When tested on Saunders 250B/C Network Analyzer the measured parameters for the crystal were:

- C_L = 19.02pF
- Target Frequency FL = 27 MHz
- FL ppm error = 0ppm
- Co = 3.8pF
- RR (Rs) = 7.5ohms
- RL (Resistance at FL) = 10.8 ohms (RR * ((1+C₀/C_L)²))
- C1 (Cs) = 14.9fF
- L (Ls) = 2.33mH

The crystal was connected to the internal oscillator X1 and X2 pins of the IDT clock synthesizer IC and the tuning capacitors were adjusted to make the output frequency 0 ppm. No series resistor (Rx) on X2 was added at this time. The oscillations were stable every time on power-up.

The current on X2 was measured using an AC current probe and was found to be 27mA (Peak-Peak). This gives us $27 / (2 \cdot \sqrt{2}) = 9.54$ mA (rms current).

Power Dissipation = $(9.54)^2 \cdot 7.5 = 683$ uW.

At this point we can see that we will be violating the maximum power dissipation specification of the crystal (100uW). In order to address this issue the following steps are taken.

Insert a series resistor of 3.9 Kohms (by trial) on X2 to reduce the drive. The current on X2 with 3.9 Kohms series resistor = 7.2mA (Peak-Peak). This gives us roughly 2.545mA (rms). The power dissipation is $(2.545)^2 \cdot 7.5 =$ nearly 50uW of power dissipation

The power dissipation of the crystal is well under the 100uW maximum power dissipation specification. The output frequency was monitored upon repeated power cycling (with the 3.9 Kohms resistor in place) and found to be within the accuracy specification. The output was verified to be a locked and stable square wave.



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