Introduction

This application note provides examples of high speed LVCMOS driver clock drivers. For high-speed LVCMOS drivers, general rules for high-speed digital board design must be followed. Proper termination is required to ensure signal quality and Electro-Magnetic Interference (EMI) reduction.

There are many different termination schemes for single-ended LVCMOS drivers. This application note discusses parallel termination, AC termination and series termination. The following termination approaches are only general recommendations under ideal conditions. Board designers should consult with their signal integrity engineers or verify through simulations in their system environment.

Parallel (DC) Termination

The standard termination of an LVCMOS driver in a Z_O=50 ohm transmission line environment is shown in Figure 1. The driver is terminated with 50 ohm pull down to VTT=V_{DDO}/2 at the receiver end. The LVCMOS clock buffer characterization set up is terminated in similar manner using split power supplies approach (see test condition in the datasheet of an LVCMOS driver). In actual applications, the equivalent parallel termination shown in Figure 2 can be used. The LVCMOS parallel termination has the same effect as the standard LVCMOS shown in Figure 1. The parallel termination shown in Figure 2 can eliminate the need of VTT=V_{DDO}/2 power supply (or reference voltage). The power dissipation calculation is described further in application note AN-809.

Figure 1. LVCMOS Driver Standard Termination

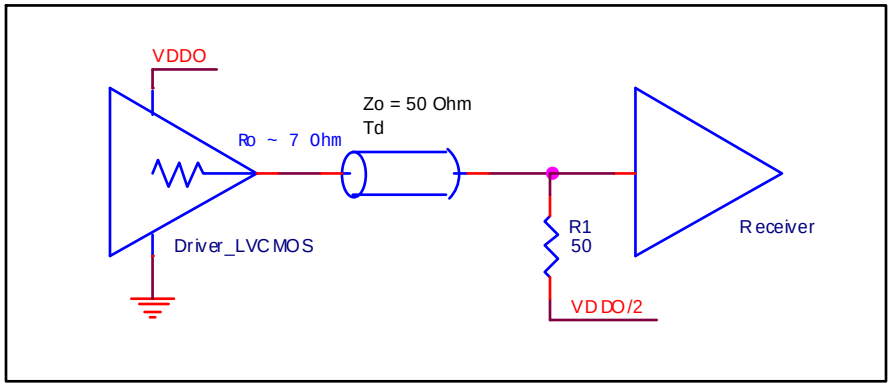
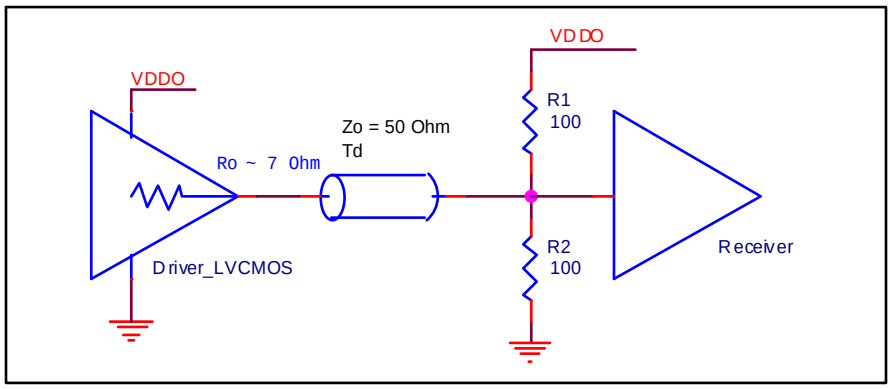


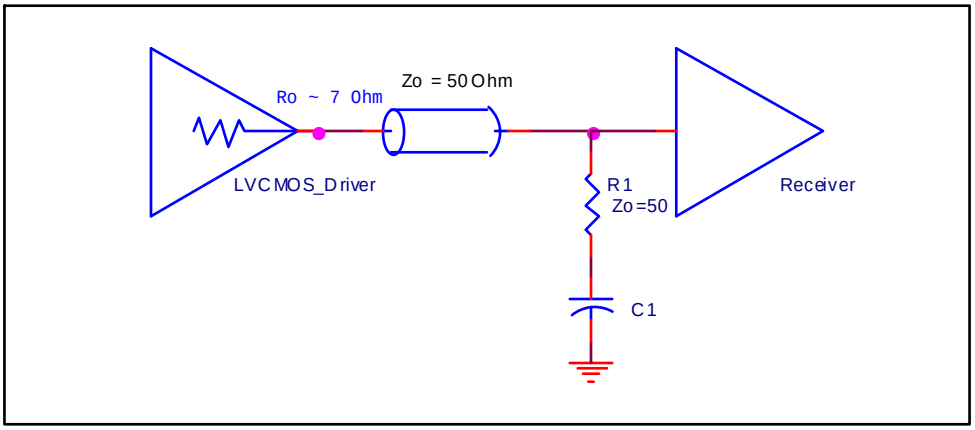
Figure 2. LVCMOS Parallel Termination



AC Termination

The LVCMOS driver AC termination in a 50 ohm transmission line environment is shown in Figure 3. The majority of load current is drawn during transient region (i.e. rising edge and falling edge). This termination consumes less power than the parallel termination. The proper value of capacitor C1 depends on the trace delay and capacitance of the transmission line. Some PC board layout or simulation software tools provide a feature of calculating the transmission line capacitance by entering the trace information (see References, [1]).

Figure 3. AC Termination



Series Termination

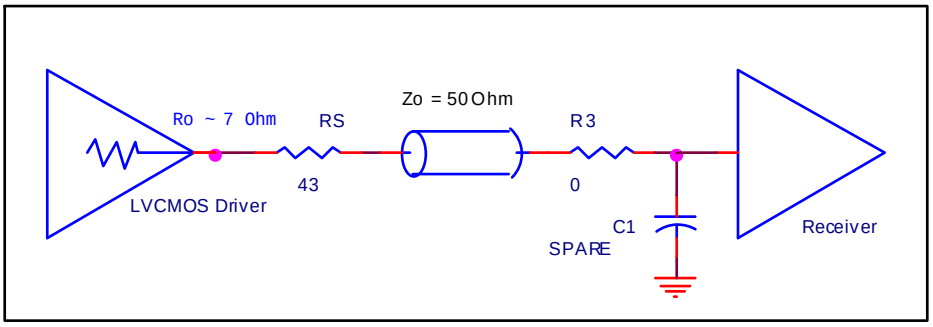
Series termination is a popular termination scheme for LVCMOS drivers. Figure 4 shows a simple series termination for LVCMOS drivers with output impedance of 7 ohm. The Power Dissipation of this termination scheme is described in a separate document.

The typical output impedance R_O of a high speed LVCMOS driver is approximately 7 to 16 ohms (some parts might have different R_O value. Refer to datasheet for the output impedance). For example, R_O=7 ohm, the closest series resistor value, R_S, can be calculated as follows:

$R_S = Z_O - R_O = 43$ ohms

In the Figure 4, the footprint for optional series resistor R3 or optional capacitor C1 at the receiver input is recommend for adjusting edge rate or overshoot if necessary.

Figure 4. One-to-One LVCMOS Series Termination



When the number of drivers is not equal to number of receivers as shown in Figure 6, the series resistor value R_S is calculated as follows:

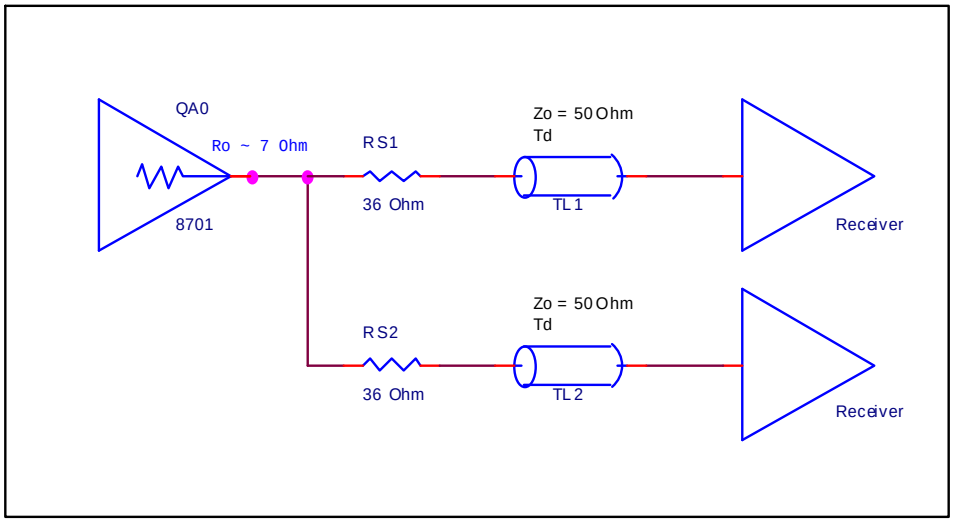
$R_S = Z_O - (R_O \times M)/(N)$

where N = number of driver; M = number of receiver

This configuration assumes that all the trace delays and load conditions are equally matched.

For example, one driver driving 2 receivers as shown in Figure 5, with N=1and M=2, the series resistor is calculated to be Rs = 36 ohms. The trace delays Td on TL1 are equal. The loading conditions on both receivers should also be equal.

Figure 5. Series Termination for One LVCMOS Driver Driving Two Receivers



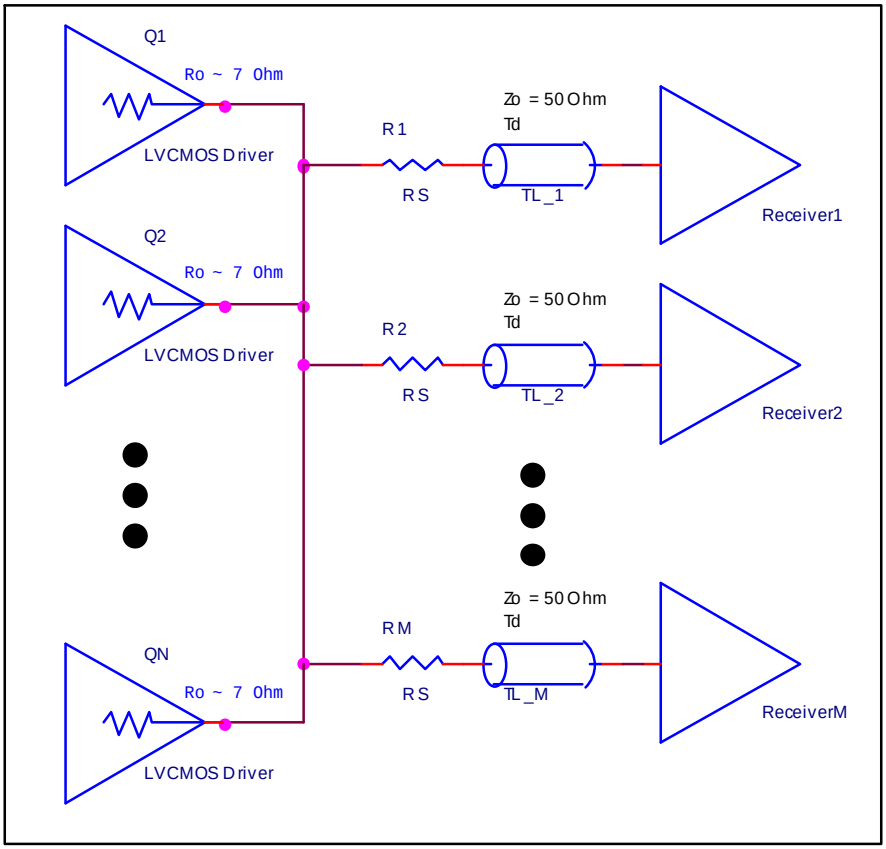
For 5 drivers driving 6 receivers, the closest series resistor can be calculated as follows:

N=5, N=6, Zo=50 Ohms, Ro =7 ohm

Rs = 50 - (7 x 6)/5 = 41.6 ohm

The result above is straight from calculations. The closest available resistor value should be chosen.

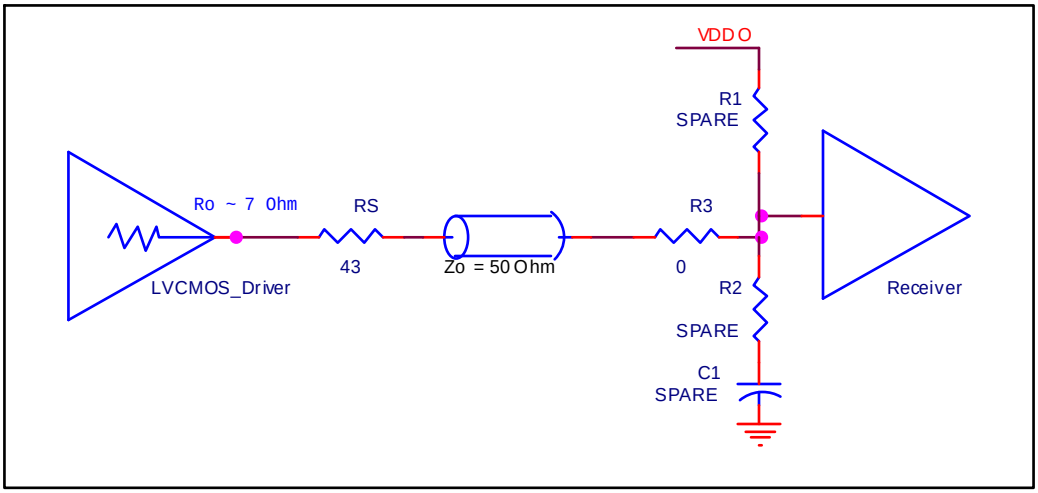
Figure 6. Tie N Outputs Together to Drive M Receivers



PC Board Layout with Option of Multiple Termination Scheme

For signal integrity, take the necessary precaution and follow the high-speed digital design rules as much as possible. In most cases, the board design cannot fully comply the high-speed design rules due to constrains on the board environment, e.g. space available, cost, etc. There is always some unknown parameters or interference in the system environment. The signal quality can only be optimized through the experiment; one termination scheme may work better then the other. While capturing a schematic for PC Board layout, if there is space available, it is recommended to provide options to choose different termination schemes. Figure 7 shows an example schematic for a PC board footprint that provides an option of choosing various types of terminations.

Figure 7. PC Board Layout Provides Footprint to Choose Various Termination Options



References

[1] Kaufer, Steve, Crisafulli, Kellee, Terminating Trace on High-Speed PCBs, Printed Circuit Design, March 1998

[2] Dr. Johnson, Howard, Dr. Graham, Martin, High-Speed Digital Design, A Handbook of Black Magic, Prentice Hall, 1993

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com