Introduction

The UFT3G provides very flexible frequency translation/generation with 0ppm accuracy. However, sometimes an application requires a fine-tuning of the base frequency to accommodate very small frequency offsets between two time domains or to calibrate for a known frequency error in the reference. This application note provides details on the methods available for fine-tuning the UFT3G devices. The scope of this document is to provide details on how to update an existing configuration generated with either Timing Commander or manually calculated using the 8T49N28X_Frequency_Programming_Guide_v1.0.pdf Application note (AN-860).

Overview

Table 1 below summarizes the four methods for fine-tuning the UFT3G output frequency. Each mechanism manipulates different parts of the device and has different responses.

Table 1: UFT3G Frequency Tuning Mechanisms

Tuning Mechanism	Dynamic Response	Granularity	Mode	Adjusts	Output Frequency Range
Fractional Output Divider	Smooth transient between frequencies (switches frequencies on first clock cycle after the divider update)	<1ppb	Jitter Attenuator and Synthesizer Mode	Single output and it's buffered copies (400MHz max)	8kHz-400MHz
WDCO	Smooth transient between Frequencies (~10mS frequency transient for a 50ppm change)	13ppb	Jitter Attenuator and Synthesizer Mode	All outputs derived from the PLL	8kHz-1GHz
Fine Feedback Divider	Momentary high pulse on the outputs	<1 part-per-trillion	Synthesizer Mode	All outputs derived from the PLL	8kHz-1GHz
Pre-Divider Offset	Band-width Shaped Clock Switch Response (~180mS for 22.5Hz BW)	<1ppm	Jitter Attenuator Mode	All outputs derived from the PLLs driven by the Reference clock	8kHz-1GHz

WDCO mode, Fractional Output Divider (FOD) adjustment, and Pre-Divider Offsets are recommended for dynamic frequency adjustment. Compared to the WDCO mode, the FOD adjustment has the advantage of finer frequency granularity and a faster response time. However, it is limited to output frequencies of 400MHz and below. The Input Pre-Divider mechanism can be used to create very slow, smooth frequency transients that are governed by the digital bandwidth settings.

For more information on the implementation details, please consult the following sections of this document: Fractional Output Divider Frequency Adjustment, WDCO Frequency Adjustment, Fine Feedback Divider Frequency Adjustment, and Input Pre-Divider Frequency Adjustment.

Fractional Output Divider Frequency Adjustment

The 8T49N28X UFT devices have two-stage fractional output dividers. For the Fractional N (FracN) output dividers, the output divide ratio is given by:

Output Divide Ratio = (N.F)x2

where:

N = Integer Part: 4, 5, ...(2_{18}-1)

F = Fractional Part: [0, 1, 2, ...(2_{28}-1)]/(2_{28})

The output frequency is given by:

$f_{output}=f_{vco}/((N.F)x2)$

For integer operation of these outputs dividers, N = 3 is also supported.

The relevant register settings are given by the following two formulas:

N_Qx= Integer portion of the Output Divide Ratio

NFRAC_Qx = round(F*2^28)

In the following example, a 156.25MHz output and 10ppm offset will be used.

1) Setup 8T49N28X to generate a 156.26MHz output on a fractional output divider, derived from a VCO running at 3750MHz. The output divider is 24.

   24=(N.F)*2 ⟶ N=12, F=0

2) Use the target ppm offset to calculate the required Noffset value using the following formula.

   PPM_offset= (N_{0ppm}-N_{offset})/N_{0ppm} *1e6

   N_{offset}= N_{0ppm} -(PPM_Offset/1e6* N_{0ppm})

where:

N_{offset} = New N divider for ppm offset

N_{0ppm} = 0ppm offset divider

For the example:

N_{0ppm}=24

N_{offset}= 24 -(10/1e6* 24)= 23.99976

Next, decompose the effective output divider into the corresponding register settings:

N_{offset} =(N.F)x2= 23.99976

N_Qx= 11, F= 0.99988

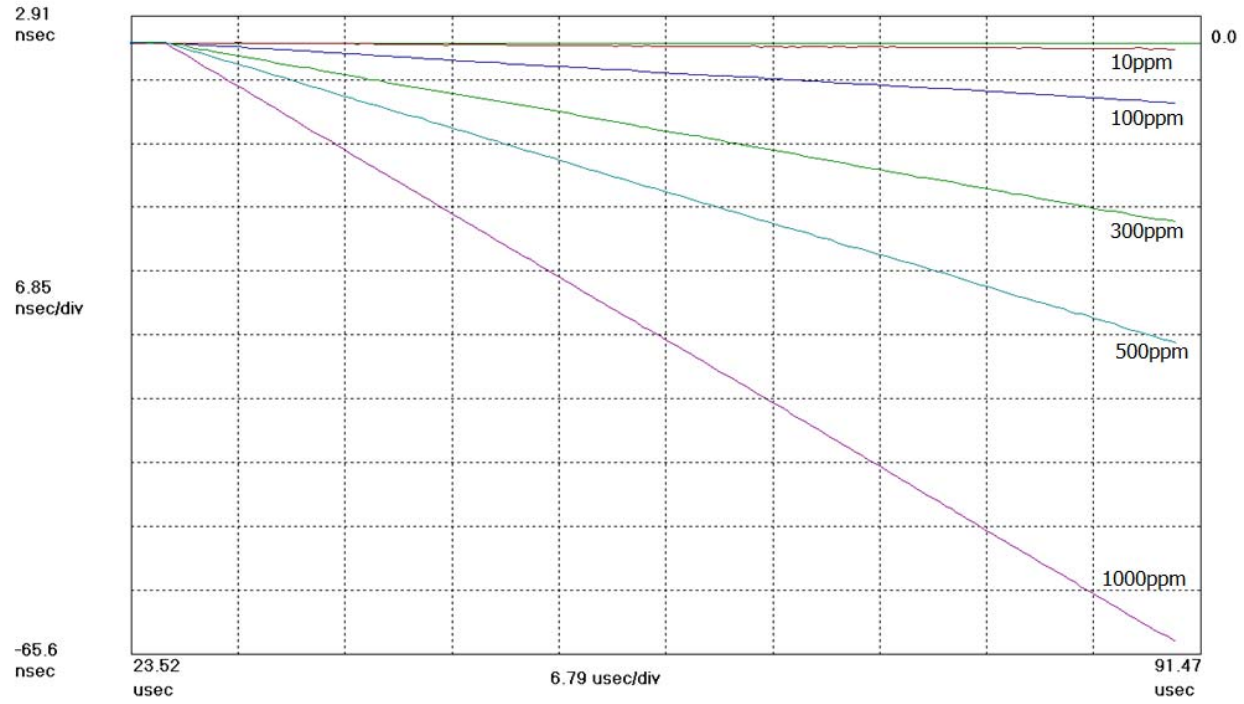
NFRAC_Qx = round(F*2^28)= 268403244

Update the complete N_Qx and NFRAC_Qx register range using an I^2C block write.

When measuring the frequency update, trigger the measurement equipment off the rising edge of the I^2C write “STOP” bit.

The plots below show phase transient responses, relative to a 0ppm signal, for different ppm offsets. There are no glitches and the frequency change is very fast and smooth. The slope of the deviation of the phase is approximately the ppm offset of the output.

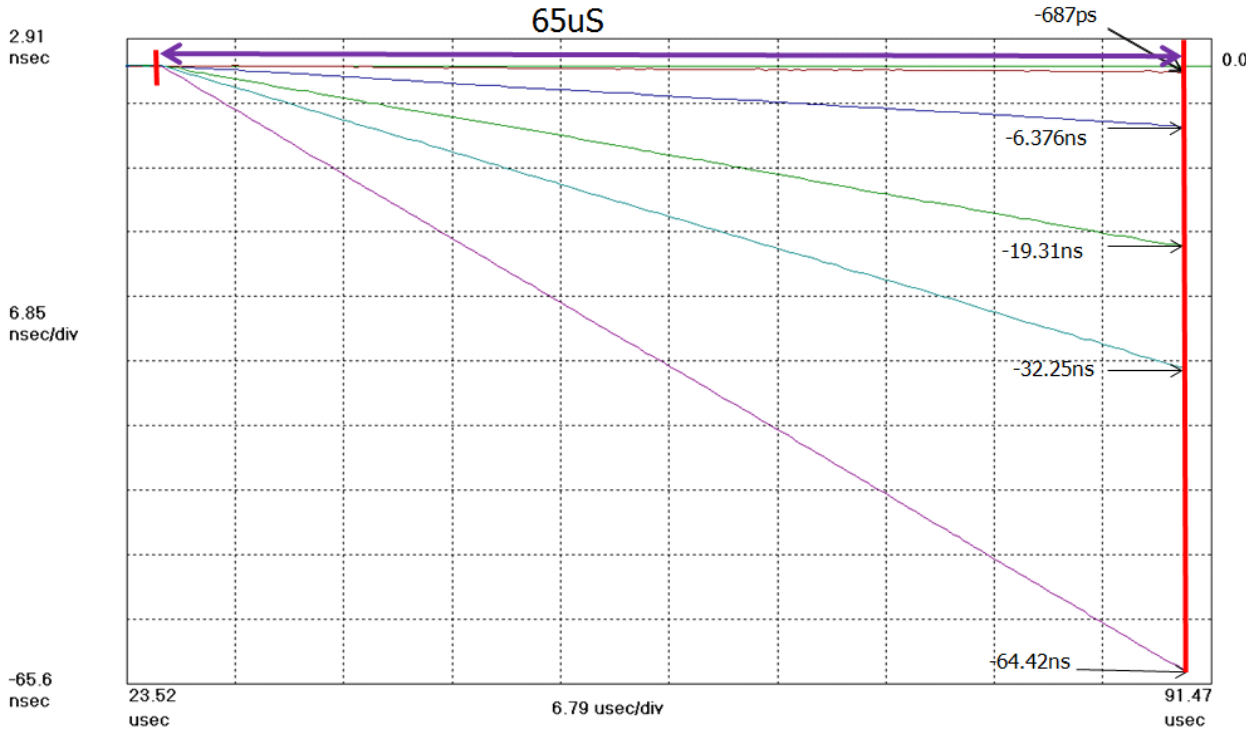
Figure 1. Phase Transient Response after FOD Update



For example, in Figure 2 below, the 1000ppm signal has deviated 64.42ns in 65µs so the ppm offset can be estimated as follows:

Slope=~ppm offset= 65µS/64.42ns= 991ppm

Figure 2. Zoom of Phase Transient Response after FOD Update



WDCO Frequency Adjustment

The 8T49N28X devices contain a Write DCO mode that allows the user to offset the VCO frequency from its normal operating frequency using digital register settings. The following procedure shows how to program the WDCO mode.

Calculate the WDCO Value

The WDCO granularity for the IDT8T49N281/IDT8T49N282/IDT8T49N2813 devices is calculated as follows:

1) Calculate the WDCO least-significant-bit (lsb) value:

$WDCO_{lsb}$ ppm offset = 1/(f_{vco}/f_{xtal} *2^21)*1e6

where:

f_{vco}= VCO frequency

f_{xtal}= Crystal frequency taking into account the doubler

Example: VCO= 3000MHz, XTAL=40MHz, Crystal doubler enabled

$WDCO_{lsb}$(ppm) = 1/ (3000/(40*2)*2^21)*1e6= 0.0127ppm

Note: A higher VCO frequency will yield more granularity but a smaller WDCO range.

2) Divide the target ppm by the WDCO lsb value and then round to the nearest integer in order to obtain the WDCO setting:

WDOC setting= round (ppm target / $WDCO_{lsb}$)

Example: 25ppm target offset

25ppm /.0127ppm = 1966.08 ⟶ 1966

WDCO Registers

The 8T49N28x device has two 17 bit WDCO registers for APLL0 and two for APLL1 (if applicable). The register field is signed two's complement. This means that the max ppm range is:

-[(2^16)-1]*$WDCO_{lsb}$ to +[(2^16)-1]*$WDCO_{lsb}$

Example:

If $WDCO_{lsb}$ = 0.0127ppm, then the WDCO range is:

=-(65535)*0.0127 to (65535)*0.0127

= -832ppm to 832ppm

WDCO: Normal Mode vs Holdover Mode

WDCO “Normal Offset” registers offset the VCO in Normal, Freerun, and Holdover modes. The registers are “live” and take immediate effect upon update.

WDCO “Holdover Offset” registers offset the VCO only in Holdover mode and only take effect when the “WDCO” bit is enabled. The “Holdover Offset” is opposite polarity of the “Normal Offset”. ***For systems that support only single-byte I^2C commands, the “Holdover Offset” can be used to mask intermediate writes.***

The following sections describe the registers and step-by-step procedures to implement each of the modes. For simplification, only one of the two modes at a time will be used.

Table 2: WDCO Registers, PLL0

PLL0 Normal Offset WDCO Registers R0025, R0026, R0027 17 bits

WDCO Holdover Offset R0028, R0029, R002A

Digital PLL0 Feedback Control Register Block Field Locations							
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0017	M1_0_0[23:16]							
0018	M1_0_0[15:8]							
0019	M1_0_0[7:0]							
001A	M1_0_1[23:16]							
001B	M1_0_1[15:8]							
001C	M1_0_1[7:0]							
001D	M1_0_2[23:16]							
001E	M1_0_2[15:8]							
001F	M1_0_2[7:0]							
0020	M1_0_3[23:16]							
0021	M1_0_3[15:8]							
0022	M1_0_3[7:0]							
0023	LCKBW0[3:0]				ACQBW0[3:0]			
0024	LCKDAMP0[2:0]			ACQDAMP0[2:0]			PLLGAIN0[1:0]	
0025	TGLCKDMP0[2:0]			TGLCKHYS0	TGLCKBW0[2:0]			Rsvd NRMOFF0[16]
0026	Rsvd NRMOFF0[15:8]							
0027	Rsvd NRMOFF0[7:0]							
0028	TGLCKTHR0[6:0]							Rsvd HLDOFF0[16]
0029	Rsvd HLDOFF0[15:8]							
002A	Rsvd HLDOFF0[7:0]							

Table 3: WDCO Register, PLL1

PLL01Normal Offset WDCO Registers R0058, R0059, R005A 17 bits

WDCO Holdover Offset R00B, R005C, R005D

Digital PLL1 Feedback Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
004F	M1_1_1[7:0]							
0050	M1_1_2[23:16]							
0051	M1_1_2[15:8]							
0052	M1_1_2[7:0]							
0053	M1_1_3[23:16]							
0054	M1_1_3[15:8]							
0055	M1_1_3[7:0]							
0056	LCKBW1[3:0]				ACQBW1[3:0]			
0057	LCKDAMP1[2:0]			ACQDAMP1[2:0]			PLLGAIN1[1:0]	
0058	TGLCKDMP1[2:0]			TGLCKHYS1	TGLCKBW1[2:0]			Rsvd NRMOFF1[16]
0059	Rsvd NRMOFF1[15:8]							
005A	Rsvd NRMOFF1[7:0]							
005B	TGLCKTHR1[6:0]							Rsvd HLDOFF1[16]
005C	Rsvd HLDOFF1[15:8]							
005D	Rsvd HLDOFF1[7:0]							

Table 4: WDCO Enable Bit and PLL State Control

Digital PLL0 Input Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
0008	REFSEL0[2:0]			FBSEL0[2:0]			RVRT0	SWMODE0
0009	PRI0_3[1:0]		PRI0_2[1:0]		PRI0_1[1:0]		PRI0_0[1:0]	
000A	REFDIS0_3	REFDIS0_2	REFDIS0_1	REFDIS0_0	Rsvd	Rsvd WDCO0	STATE0[1:0]	

PLL0 WDCO Enable Bit	WDCO0	R/W	0b	Enables WDCO mode for Digital PLL0. This mode allows a fixed offset to be programmed into the VCO.
State Control	STATE0[1:0]	R/W	00b	Digital PLL0 State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode for PLL0. 10 = Force NORMAL state 11 = Force HOLDOVER state

Digital PLL1 Input Control Register Block Field Locations								
Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
003B	REFSEL1[2:0]			FBSEL1[2:0]			RVRT1	SWMODE1
003C	PRI1_3[1:0]		PRI1_2[1:0]		PRI1_1[1:0]		PRI1_0[1:0]	
003D	REFDIS1_3	REFDIS1_2	REFDIS1_1	REFDIS1_0	Rsvd	Rsvd WDCO1	STATE1[1:0]	

PLL1 WDCO Enable Bit	WDCO1	R/W	0b	Enables WDCO mode for Digital PLL1. This mode allows a fixed offset to be programmed into the VCO.
State Control	STATE1[1:0]	R/W	00b	Digital PLL1 State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode for PLL1 10 = Force NORMAL state 11 = Force HOLDOVER state

WDCO Normal Offset Programming Steps

Use the following steps to program the WDCO offset. Instructions for PLL0 and PLL1 are included. Program only the applicable PLL.

1) Lock the device to the XTAL input.
2) Make sure that the DPLL settings are set as follows:

   DPLL0 Powered up: Register 0xB8 bit2=1

   DPLL1 Powered up: Register 0xB8 bit3=1 (if applicable).

   DSM_ORD0=3 (Register 0x3A, bits 6 and 7, for PLL0)

   DSM_ORD1=3(Register 0x6D, bits 6 and 7, for PLL1, if applicable).

   STATEx can be in any of the four states.
3) Program the “WDCOx NRMOFF” registers.

The WDCO offset will now be observed as a ppm offset on the output.

WDCO Holdover Offset Programming Steps

Use the following steps to program the WDCO Holdover offset. Instructions for PLL0 and PLL1 are included. Program only the applicable PLL.

1) Lock the device to the XTAL input.
2) Make sure that the DPLL settings are set as follows:

   DPLL0 Powered up: Register 0xB8 bit2=1

   DPLL1 Powered up: Register 0xB8 bit3=1

DSM_ORD0=3 (Register 0x3A, bits 6 and 7, for PLL0)

DSM_ORD1=3(Register 0x6D, bits 6 and 7, for PLL1, if applicable).

STATEx=11 (Holdover)

3) Program the “WDCO HLDOFF” registers. The ppm offset on the output will remain at 0.
4) Set WDCOx=1. The WDCO offset will now be observed as the opposite ppm offset on the output.

Updating WDCO with Single-byte Writes

When using only single-byte I^2C writes, changing from 0x00FF to 0x0100 can cause unintended or unnecessary frequency steps. Using the WDCO HLDOFF setting, the output can be manipulated such that only the target ppm offsets are present.

In this example the WDCO is offset from 0x00FF to 0x0100 with a temporary return to a 0ppm offset. The sequence starts with WDCOx_HLDOFF=0x00FF and WDCOx=0.

Table 5: Program WDCO Using Single-Byte Writes

Command	WDCO HLDOFF Value	ppm offset
Write WDCOx HLDOFF	0x00FF	0
Write WDCOx=1	0x00FF	-0xFF* $WDCO_{lsb}$
Run tests	--	--
Write WDCOx=0	0x00FF	0
Write WDCOx HLDOFF lower byte	0x0000	0
Write WDCOx HLDOFF upper byte	0x0100	0
Write WDCOx=1	0x00FF	-0x100* $WDCO_{lsb}$

The WDCO update to the VCO will take ~500µS to settle on the output. The two images below show example of the frequency versus time transients when the FOD is updated.

Figure 3. WDCO Frequency Change: 0ppm to +50ppm

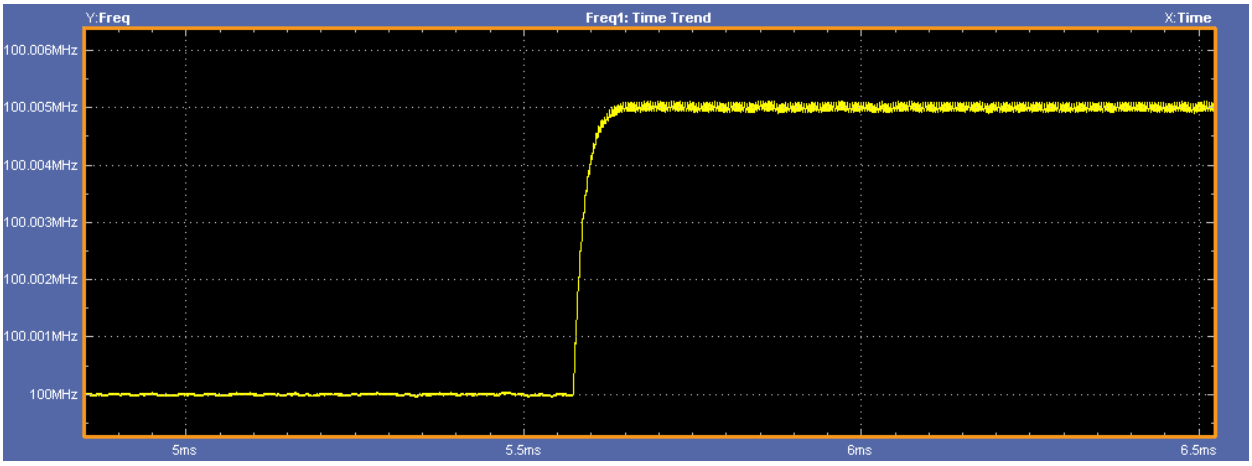
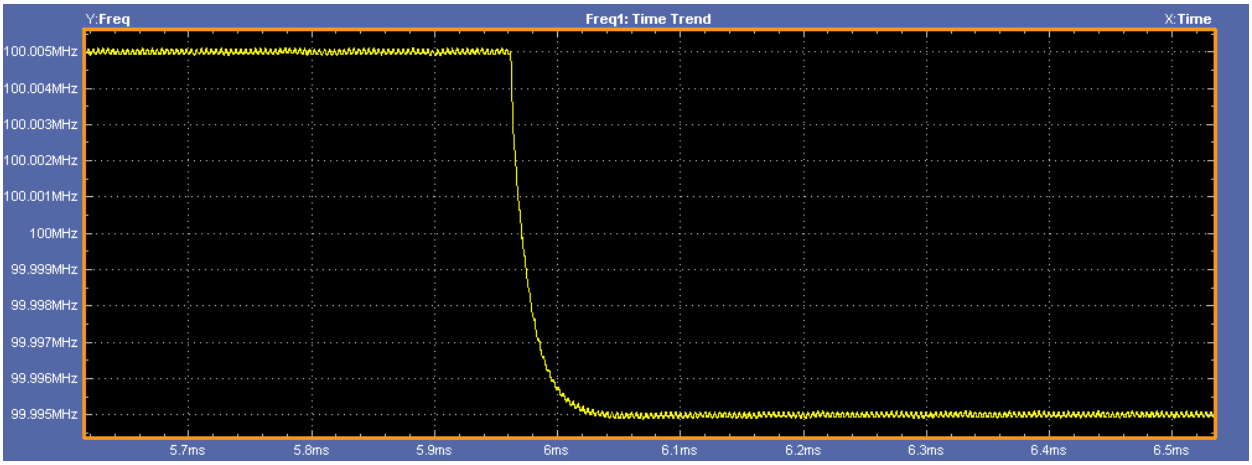


Figure 4. WDCO Frequency Change: +50ppm to -50ppm



Fine Feedback Divider Frequency Adjustment

The feedback divider for the 8T49N28X devices can be adjusted with <1ppt (part-per-trillion) granularity. This mode provides the ability to generate very accurate frequency outputs. However, updates to the feedback divider will trigger a re-sync sequence which momentarily stops the outputs from switching for an interval of 320ns. Therefore, this mode is not recommended for dynamic adjustment of the VCO if glitch-less outputs are required.

The VCO feedback divider value can be calculated as follows:

DSM_INTx+ (DSMFRACx + DSM_NUMx/DSM_DENx)/2^21.

Refer to the datasheet for information on DSM_INTx and DSMFRACx. Information for DSM_NUMx and DSM_DENx is shown below.

Table 6: Fine Feedback Registers

APLL0

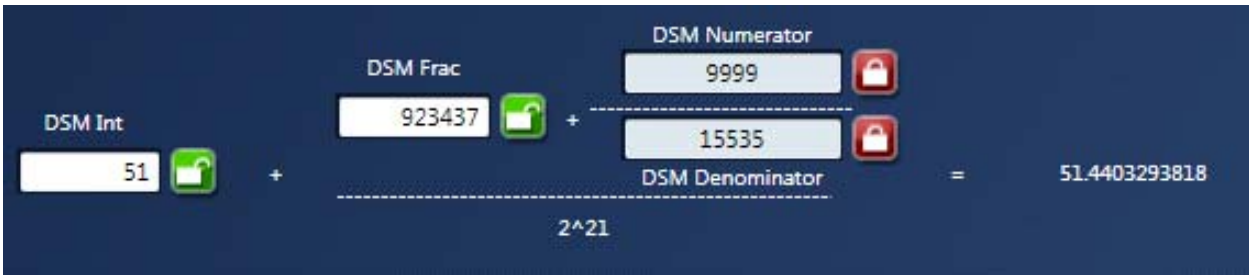
Digital PLL0 Feedback Configuration Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value (Binary)**	**Description**
DSM_DEN0[15:0]	R/W	0x0001	Denominator of fraction to be used by Delta-Sigma Modulator.
DSM_NUM0[15:0]	R/W	0x0000	Numerator of fraction to be used by Delta-Sigma Modulator.

APLL1

0069	Rsvd DSM_DEN1[15:8]		
006A	Rsvd DSM_DEN1[7:0]		
006B	Rsvd DSM_NUM1[15:8]		
006C	Rsvd DSM_NUM1[7:0]		
DSM_DEN1[15:0]	R/W	0x0001	Denominator of fraction to be used by Delta-Sigma Modulator
DSM_NUM1[15:0]	R/W	0x0000	Numerator of fraction to be used by Delta-Sigma Modulator.

An example calculation is shown below:

Figure 5. Fine Feedback Example Calculation



VCO Manual Override

The Fractional feedback adjustments always trigger a digital re-lock sequence. To prevent this, the VCO must be set into Manual override mode. In order to do this, the following steps need to take place:

1) Read the VCO digital setting.
2) Override the VCO
    a) Write the Digital setting to the VCO override field.
    b) Enable the Manual PLL mode.
3) Change the feedback divider.

1. Read the VCO Digital Bit Setting

"x" in the following figures is "0" for PLL0 and "1" for PLL1 settings.

Read the VCO digital setting.

Register 0x021C[5:0]= Calibration Digital Bits for APLL0

Register 0x021D[5:0]= Calibration Digital Bits for APLL1

Figure 6. Calibration Bits Registers

Bit 5 indicates which VCO range is selected.

CALI_DBITx[5]=0: VCO2 range is selected

CALI_DBITx[5]=1: VCO1 range is selected

The rest of the bits, CALI_DBITx[4:0] are the Digital Band

In the example above:

APLL0, Digital Bit settings= 0x0F ⟶ VCO2 range is selected, digital band is 0b01111

APLL0, Digital Bit settings= 0x32 ⟶ VCO1 range is selected, digital band is 0b10010

2. Override the VCO

A) Select the VCO Range:

Set VCOMAN_x= CALI_DBITx[5] from the read data (previous figure)

0 ⟶ VCO2

1 ⟶ VCO1

B) Set the Digital Bits for the corresponding VCO Range:

If CALI_DBITx[5]=1, then set DBIT1_x = CALI_DBITx[4:0]

If CALI_DBITx[5]=0, then set DBIT2_x = CALI_DBITx[4:0]

C) Enable Manual VCO Override:

Set DBITM_x=1

Override the VCO Registers

Table 7: Manual VCO Override Enable Bits

Analog PLL0 Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00AC	CPSET_0[2:0]			RS_0[1:0]		CP_0[1:0]		WPOST_0
00AD	Rsvd				SYN_MODE0	Rsvd	DLCNT_0	DBITM_0
00AE	Rsvd		VCOMAN_0	DBIT1_0[4:0]				
00AF	Rsvd			DBIT2_0[4:0]				

DBITM_0	R/W	0	Digital Lock Manual Override Setting for Analog PLL0: 0 = Automatic Mode 1 = Manual Mode
VCOMAN_0	R/W	1	Manual Lock Mode VCO Selection Setting for Analog PLL0: 0 = VCO2 1 = VCO1
DBIT1_0[4:0]	R/W	01011	Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL0.
DBIT2_0[4:0]	R/W	00000	Manual Mode Digital Lock Control Setting for VCO2 in Analog PLL0.

APLL0

Analog PLL1 Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00B0	CPSET_1[2:0]			RS_1[1:0]		CP_1[1:0]		WPOST_1
00B1	Rsvd				SYN_MODE1	Rsvd	DLCNT_1	DBITM_1
00B2	Rsvd		VCOMAN_1	DBIT1_1[4:0]				
00B3	Rsvd			DBIT2_1[4:0]				

DBITM_1	R/W	0	Digital Lock Manual Override Setting for Analog PLL1: 0 = Automatic Mode 1 = Manual Mode
VCOMAN_1	R/W	1	Manual Lock Mode VCO Selection Setting for Analog PLL1: 0 = VCO2 1 = VCO1
DBIT1_1[4:0]	R/W	01011	Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL1:

APLL1

3. Change the Feedback Divider

A. Write all the registers to the device. This will be the initial condition.

B. Use an I2C Block Write to write the registers for DSMFRACx, DSM_NUMx, and DSM_DENx

a. For PLL0, this range is 0x33 to 0x39

b. For PLL1, this range is 0x66 to 0x6C

C. To write only the Fine Fractional DSM_DENx:

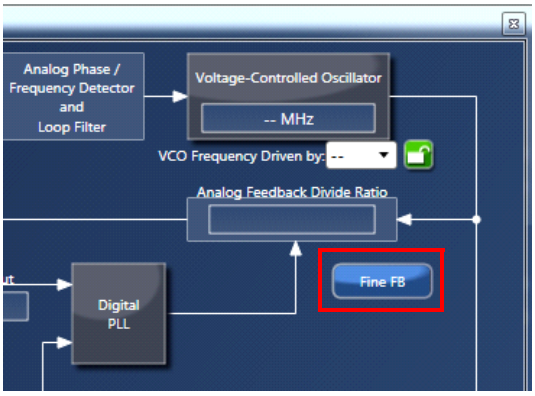
a. For PLL0, this range is 0x38 to 0x39

b. For PLL1, this range is 0x6b to 0x6C

Fine Feedback Adjustment with Timing Commander

The 8T49N28x v2.6 and newer personalities support automatic toggling between two Fine Frequency adjustments using a loop. The tool, if enabled by an IDT representative, can be found by pressing the “Fine FB” in the PLL pop-up window:

Figure 7. Fine Feedback Popup Button



The bottom of the new pop-up window has the following options:

Figure 8. Feedback Fine Tuning Configuration

Below is a description of the labels:

Register: the I^2C block write start address

Pause Between Writes: the pause time (in ms) between writes

Write Loops: How many times to repeat the loop.

Data0: 1st set of byte values. For example, “00 01”

Data1: 2nd set of bytes value. For example, “00 00”. Consider this the reset data.

Write Button: Pressing this will loop through the data writes.

The following setup will update the DSM_NUM1 with an I^2C block write. First, setup the device default values as follows:

a) Connect to the device.

b) Press “WriteAll” button.

c) Disable Auto-Polling, Disable Connection Monitor, and Disable Write Immediate.

d) Set DSM_NUM=0xff (decimal 15535)

Adjust the Fine Feedback:

e) Bring up the “Fine FB” window

f) Set the offset register to 0x6B

g) Set the Pause time to 5000

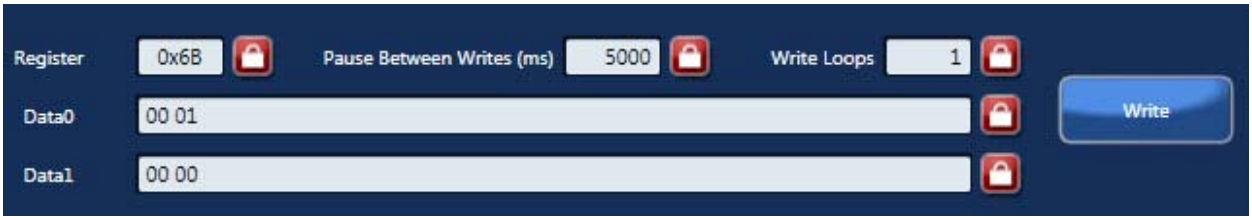
h) Set the Write Loops=1

i) Set Data0=00 01. This sets the DSM_NUM lsb

j) Set Data1=00 00

k) Press “Write”

Figure 9. Fine Feedback Auto Writes



Pre-Divider Offset Frequency Offset

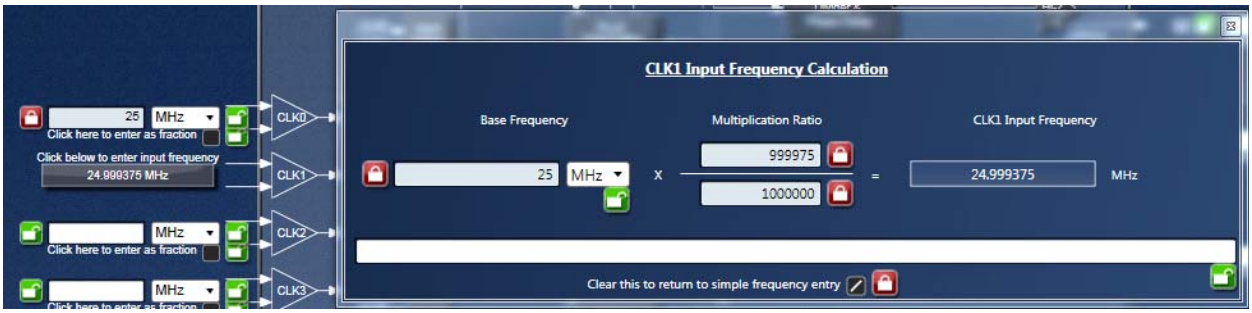
When the 8T49N28X device is configured in jitter attenuator mode, the configuration is calculated for 0ppm offset. This provides a 1:1 ppm tracking between the input and the output frequencies. However, there is flexibility within the device to calculate an alternate input pre-divider ration that causes a ppm offset of the output frequency relative to the input clock. The input pre-divider calculation algorithm is beyond the scope of this document. Timing Commander will be used in the example below. However, if there is a need to support the calculations within a system, please refer to 8T49N28X_Frequency_Programming_Guide_v1.0.pdf Application note (AN-860)

The following example shows how to generate a +25ppm offset for CLK1.

A. On the evaluation board or system, connect the same 25MHz input to CLK0 and CLK1.

B. Configure CLK1 to be -25ppm (so that when the PLL locks to this input, it will create a +25ppm offset).

Figure 10. CLK1 PPM Offset

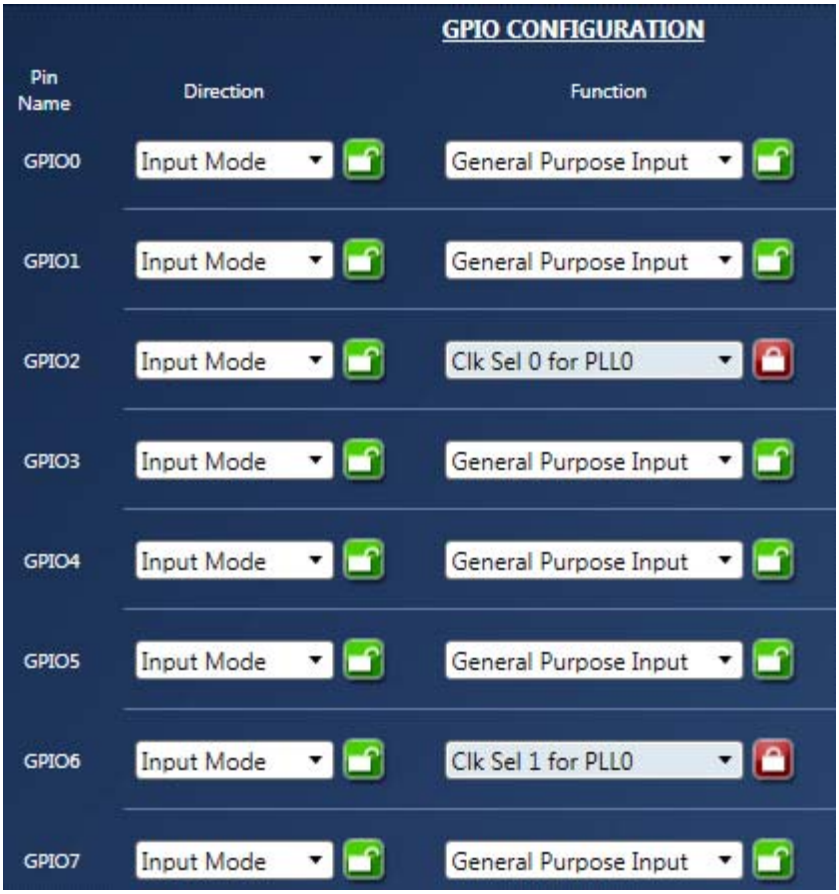


C. Select a PFD frequency that is as close as possible. Use the sliders if necessary. See Figure 11. For this test, set the switch mode to be selected by the GPIO by setting “Switching Mode” to “Manual-via-Pin”. In the system, this will be selected using a register. But for this test, it is easier to trigger off a DC control signal than an I^2C sequence:

Figure 11. Common PFD Frequency for Offset Clock

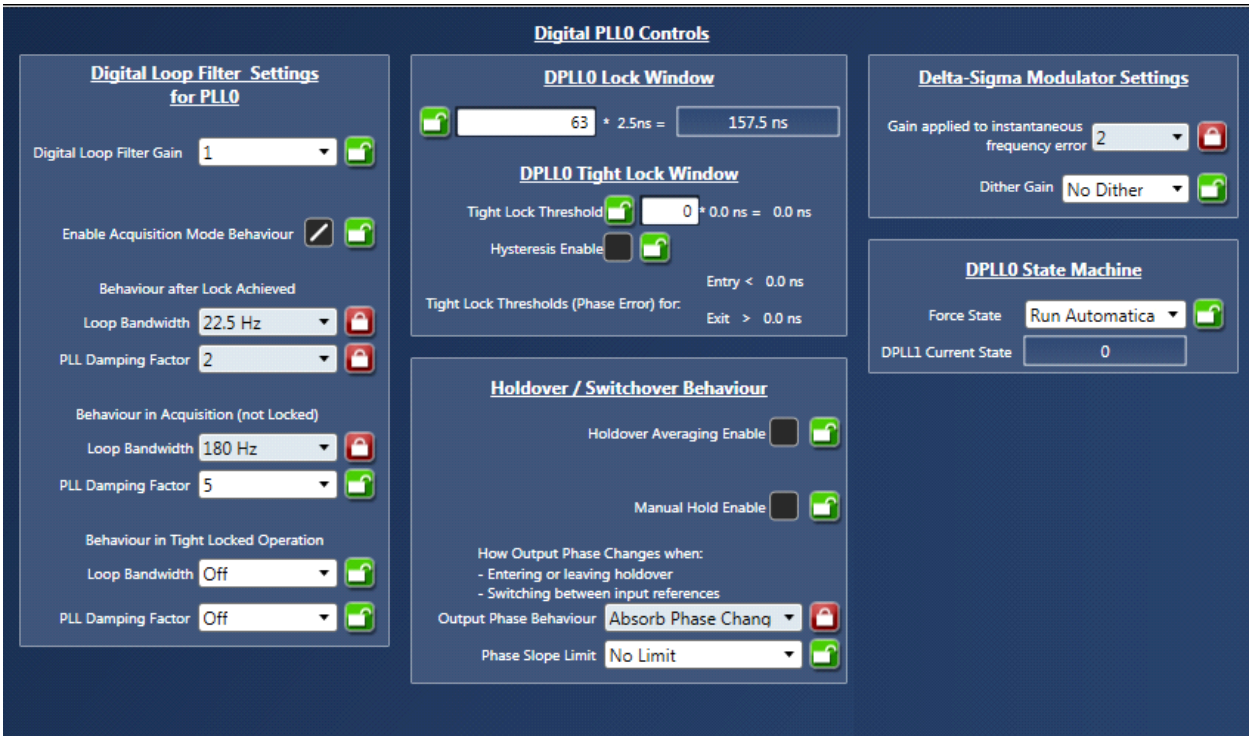
Setup the GPIO to select the clock source for PLL0.

Figure 12. GPIO Setup for PLL0 Clock Selection



Set the Digital PLL BW settings to adjust the clock switching profile. Below are some friendly settings for a '286 device. Please contact IDT for more information regarding bandwidth setting recommendations.

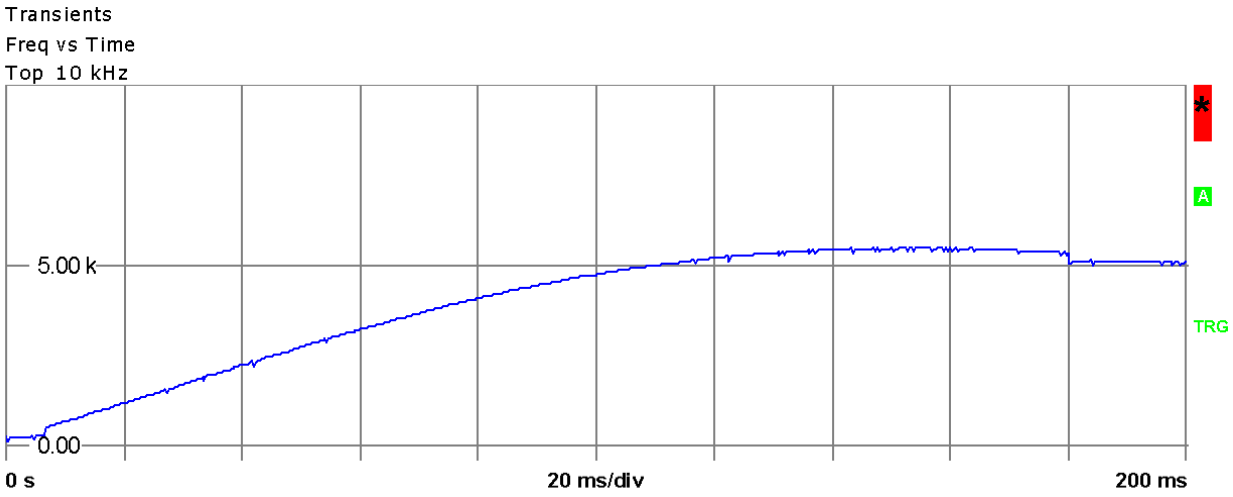
Figure 13. DPLL Clock Switch Bandwidth Settings



Connect the GPIO6 go ground. Connect GPIO2 to a banana wire and also the trigger input of the equipment. Touch GPIO2 to GND to trigger the clock switch.

Figure 14 shows that the frequency transient for a 156.25MHz signal switching from CLK0 (0ppm) to CLK1 (25ppm). The transient is very smooth and settles after 180ms.

Figure 14. Clock Switch PPM Offset



This mechanism can be used in a couple of ways. One option is to configure the different input CLKs for varying ppm offsets and then use the manual clock select to the target margin frequency. For example, the clocks can be configured as follows:

CLK0 = 0ppm

CLK1 = -100ppm

CLK2 = 100ppm

CLK3 = not used

Another methodology is to alternately configure two clocks and use the manual selection to smoothly switch between them. Here's an example:

a) Configure CLK0 to have a ppm offset
b) Manually Select CLK0
c) Configure CLK1 to have a ppm offset
d) Manually Select CLK1
e) Repeat a-d using new ppm offsets

Revision History

Rev.	Date	Originator	Description of Change
A	10/14/14	P. J.	Initial release.
B	11/05/14	S. G.	Corrected typo in *UFT3G Frequency Tuning Mechanisms* table for WDCO Granularity from 9ppm to 13ppb (pg. 1).

www.IDT.com

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com