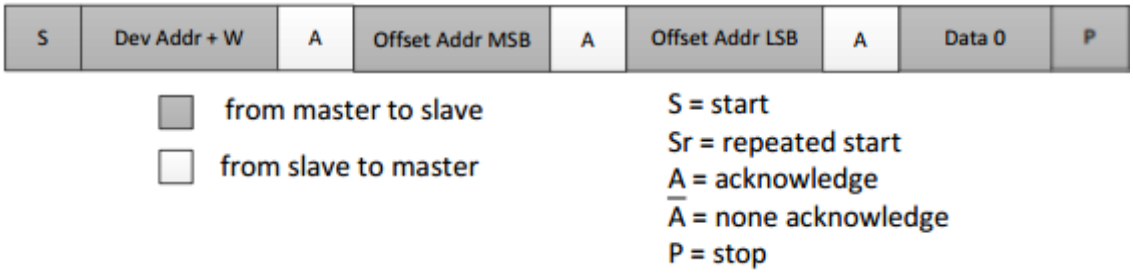
Introduction

This application note addresses important timing considerations that must be taken into account when writing to the UFT3G devices (8T49N28x, 8T49N24x, 8T49N1012) using I2C or SPI. The UFT3G devices are very flexible and support in-system programming. Whether configuring the device for on-the-fly frequency changes, or programming the part at boot up, it's important to provide the necessary idle time between writes in order to ensure that ensuing I2C writes are successful. Though many of these devices support the SPI protocol, the scope of this application note will be limited to the I2C protocol. However, the same principles and idle times apply for the SPI protocol. In addition, this document does not cover the setup and hold timings associated with each protocol since they are covered in the datasheets.

I2C Write Sequences

One important consideration is the type of I2C writes that the system is using. It's very common for systems to use **single-byte writes**, as described in Figure 1. The system's I2C master will write individual registers with each command starting with a Start command and terminating with a Stop command.

Figure 1. Single-Byte Write



Systems may also support I2C **block writes**, also referred to as "Sequential Write" in the datasheets and shown in Figure 2 below.

Figure 2. Block Write

Timing Considerations

The first consideration is that changes to the PLL feedback dividers will affect the I2C timings, which are derived from the PLL (PLL0 for devices with more than one PLL). Under normal operation, whenever changes are made to the feedback dividers of this PLL it triggers a re-calibration which will momentarily disrupt the I2C timings for about 250mS. In addition, if the DPLL calibration is disabled, though changes to the feedback divider won't cause any re-calibration, they will still cause a momentary change in frequency that also disrupts the I2C timings for about 350µS. Any I2C transactions issued during these "disruptions" run the risk of corruption, so it's recommended to provide the idle times mentioned.

Timing Recommendations

With the Write Sequence and Timing Considerations in mind, the following recommendations ensure deterministic I2C sequences.

Back-to-back single-byte writes that don't modify the primary PLL feedback dividers

Recommended idle time =160nS. (See "Appendix" for the calculations).

Back-to-back single-byte writes that modify the primary PLL feedback dividers

1. If the PLL is running under normal operation (DPLL calibration is enabled), allow 250mS for calibration each time a feedback divider setting is modified. This may be impractical in a system since this may add seconds of idle time for a single configuration. Taking that into account, the calibration circuit may be disabled. See next point for the idle time recommendation.
2. If the DPLL's calibration circuit is disabled allow 350µS of idle time.

System Implementation

The recommendations below describe how this is implemented in a system.

Step A: After reset, allow 125mS for the I2C bus to be available.

Step B: Use the sequence for the Case below that matches the system's implementation.

Case 1: Single-byte-writes, DPLL calibration disabled

1. Disable DPLL0 and wait 350µS

   8T49N28x: write 0x05 to register 0x0B8

   8T49N24x: write 0x05 to register 0x70

   8T49N1012: write 0x03 to register 0xA2

2. Write back-to-back byte writes with 160nS idle time between writes.

   If writing to the primary PLL feedback dividers, wait 350µS between writes.

3. Enable DPLL0

   8T49N28x: write 0x00 to register 0x0B8

   8T49N24x: write 0x00 to register 0x70

   8T49N1012: write 0x00 to register 0xA2

4. Calibration takes place at the end of the write, so wait 250mS before the next I2C command.

Case 2: Single-byte-writes, DPLL calibration enabled

1. Write back-to-back byte writes with 160nS idle time between writes.
2. If modifying the primary PLL feedback dividers, wait 250ms between writes.

Case 3: Block write

1. Write from add the registers in a single command.

   8T49N28x: write from register 0x00 to 0xCB

   8T49N24x: write from register 0x00 to 0x7B

   8T49N1012: write from register 0x00 to 0xA2

   Calibration takes place at the end of the write, so wait 250mS before the next I2C command.

Appendix

Idle Time Calculations:

One T cycle = VCO period × 64.

For a device with a VCO minimum frequency of 3GHz, that's 6 × (64 × 1/3GHz) = 2 × 64 × 1nS = 128nS.

For a device with a VCO minimum frequency of 2.4GHz, that's 6 × (64 × 1/3GHz) = 2 × 64 × 1nS =1 60nS.

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