ICS307-03 DEMO BOARD INSTRUCTIONS ICS307-03

The ICS307-03 demo board provides a way to quickly evaluate the performance of this serially programmable clock generator. The demo board can be connected to the parallel port of a PC for programming the ICS307-03 using the VersaClock™ II Programmer software (http://search.icst.com/software).

Jumpers

The jumper for PD provides a direct connection to GND when closed. Leave the jumper open for normal operation. There is an internal pull-up on the PD pin. A small wire or 0 ohm chip resistor can also be used as a jumper.

Output Termination

Resistors R1, R2, and R3 are 33 ohm series termination resistors on the clock outputs. A discrete capacitor can be placed on the bottom side of the board at the CLKx test points (a GND is near the test point of each output) to simulate the capacitive loading of the driver on a system board.

External Clock and Crystal Tuning

There are two ways to provide a source clock to the ICS307-03, one is from an external reference clock and the second is from a crystal. The SMA connector is for the use of an external reference clock i.e. pulse generator. Jumper the SMA trace pad to the trace pad side of C9 going to X1 of ICS307-03 (bottom side of the board). Leave X2 unconnected with no capacitors on C8. A 49.9 ohm chip resistor can be placed at C9 for termination.

If using a parallel resonant crystal, leave the SMA trace pad open. C8 and C9 are for the crystal load capacitors, if needed. Crystals with a load capacitance of 12 pF does not require any external load capacitors on C8 and C9. For crystals with a specified load capacitance greater than 12 pF, external load capacitors will be required for an accurate frequency output on C8 and C9. The values of the external load capacitors are based on the formula:

C8, C9 = (CL - 12) * 2

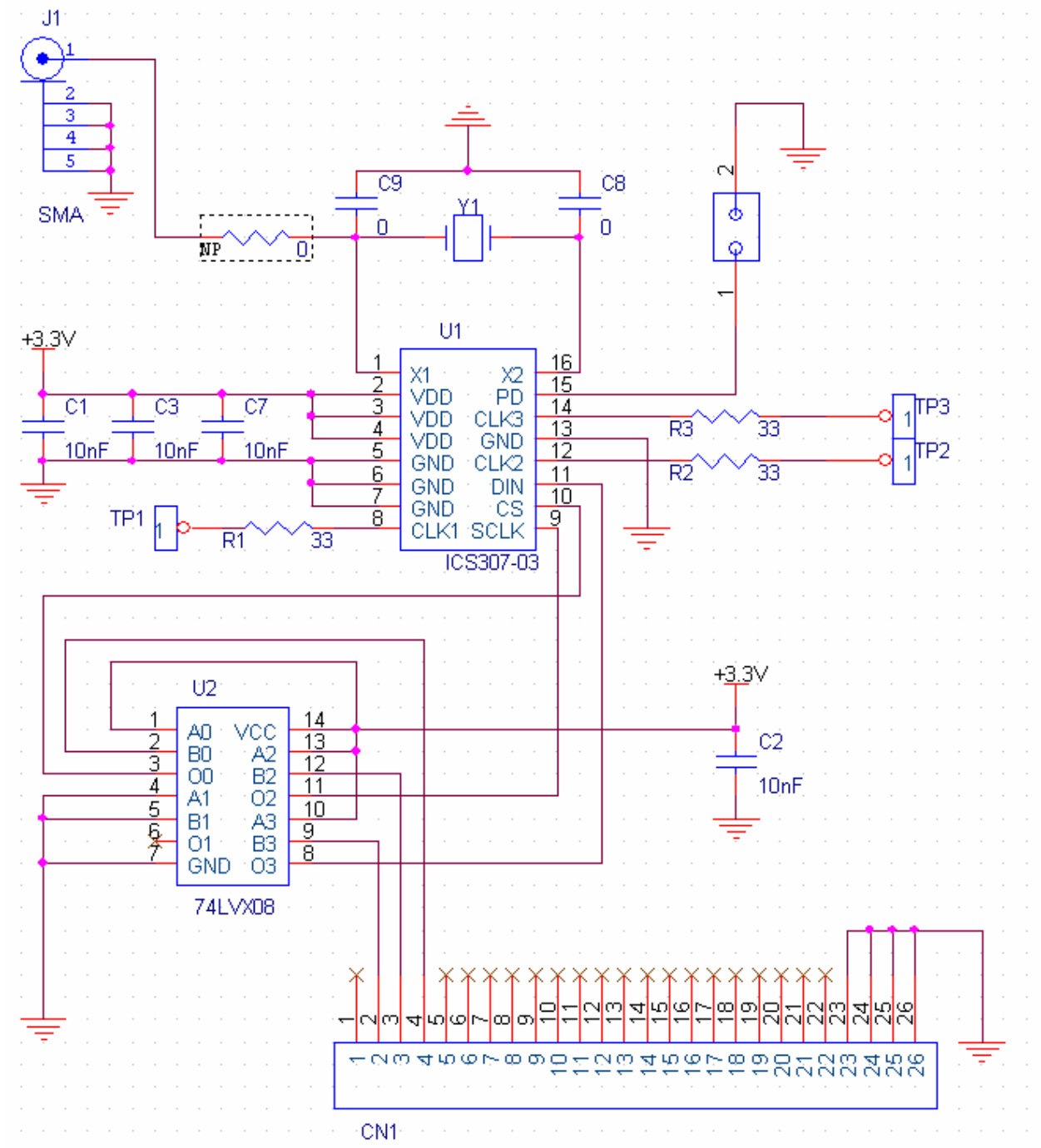
where CL is the specified crystal load capacitance in pF.

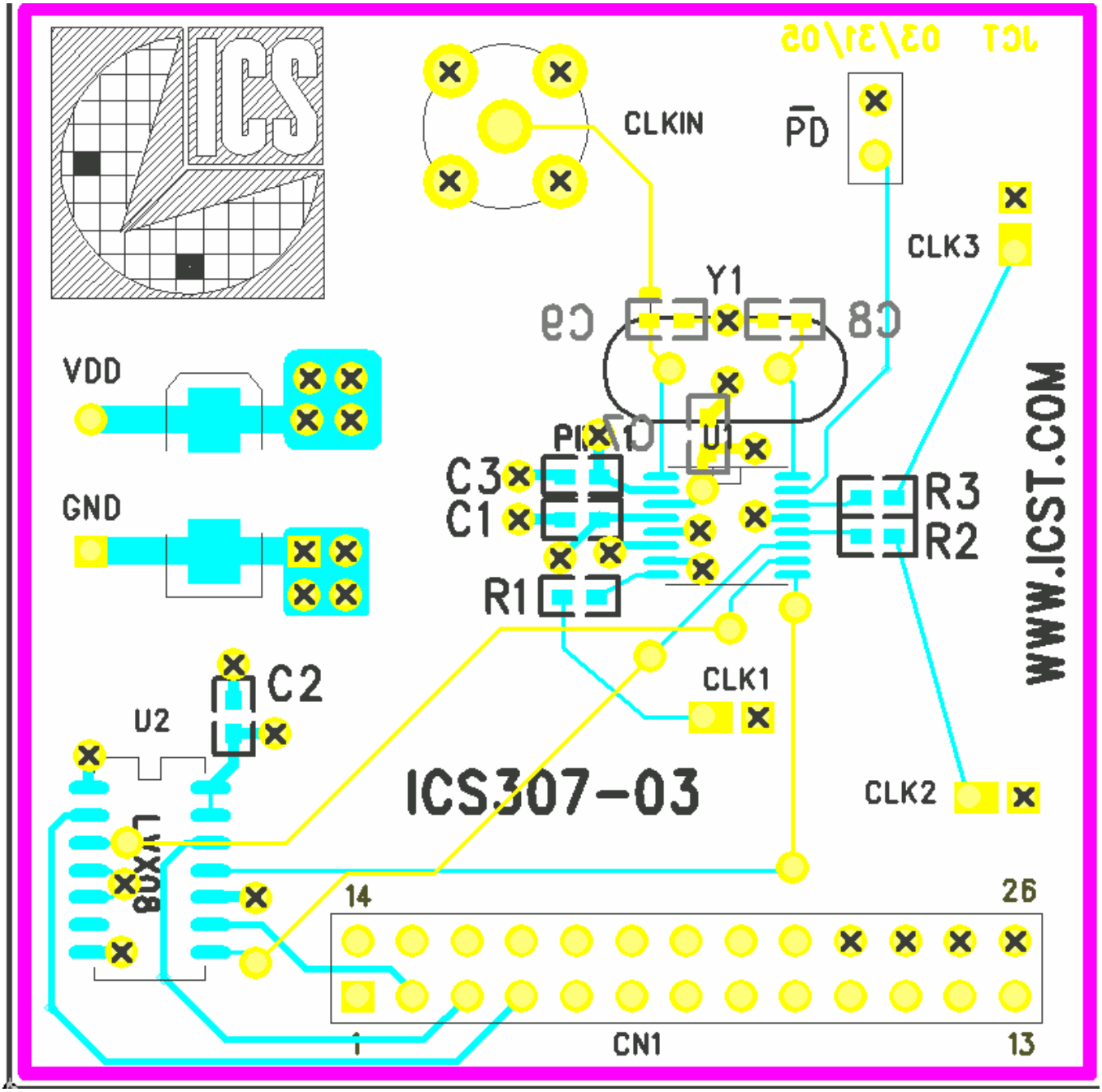
Decoupling

Each VDD has a 0.01 µF decoupling capacitor to GND.

Programming

The ICS307-03 demo board has a 26-pin header that can be connected to the parallel port of a PC when using the VersaClock™ II software for programming. Pins 2, 3, and 4 on the header are used as DIN, SCLK, and CS, respectively. The three signals are buffered through an LVX08 to the ICS307-03.


J1
SMA
NP
0
C9
C8
Y1
U1
X1
X2
VDD
PD
CLK3
GND
CLK2
DIN
CS
SCLK
ICS307-03
+3.3V
C1
C3
C7
10nF
R3
R2
33
TP3
TP2
TP1
R1
U2
A0
B0
O0
A1
B1
O1
GND
VCC
A2
B2
O2
A3
B3
O3
74LVX08
C2
CN1


CLKIN
PD
CLK3
Y1
VDD
GND
C3
C1
R1
R3
R2
U1
C2
U2
CLK1
CLK2
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