IDT Application Note MAN05

IDT has developed a patented technique to integrate a Voltage Controlled Crystal Oscillator (VCXO) function into clock synthesizer products. The VCXO oscillator circuit, in conjunction with an external crystal, allows the output clocks to be pulled (varied up or down in frequency) more than 100 parts per million (±100ppm or 0.01%), under control of an analog input voltage. The MK27XX and MK37XX series of products integrate a VCXO oscillator and a PLL, creating a cost effective VCXO clock solution. Our communication synchronization products (MK2049, MK2058, MK2059, MK2069, ICS726A) use the integrated VCXO as a circuit block, and this information applies to these products also.

Crystal Selection

The crystal is the frequency reference of the VCXO and the overall performance of the circuit depends on the characteristics of it. It is important that the crystal meets all required specifications if the VCXO is expected to work reliably. IDT works with crystal vendors to define, build, and certify crystals that meet these requirements, and the crystal vendors maintain an inventory of these devices in stock. Please see our web site for recommended part numbers.

Using a packaged clock oscillator to drive these VCXO products will not work correctly. The clock will be generated, but the frequency cannot be pulled because the VCXO circuit has no control over the oscillator frequency.

Crystal Specifications

The crystals defined for use with VCXO products have specifications common to all crystals, and additional requirements to insure VCXO performance. All crystals have specifications for:

1. Frequency tolerance (often called Calibration Accuracy). This is the allowable frequency error from a specified center frequency of the crystal at 25 c. This parameter is specified with a maximum and minimum frequency deviation, expressed in percent (%) or parts per million (ppm). It is typically +/-20ppm for IC VCXO crystal designs. The source of this error term is principally variation in the manufacturing process.

2. Temperature stability. This is the change in frequency allowed as temperature is varied from 25 c to the temperature extremes, hot and cold. This variation is characteristic of a quartz crystal, and the slope and magnitude is controlled by the type of crystal cut and the crystal lattice angle at which the crystal is cut. This parameter is specified with a maximum and minimum frequency deviation, expressed in percent (%) or parts per million (ppm). It is typically +/-30ppm for IC VCXO designs.

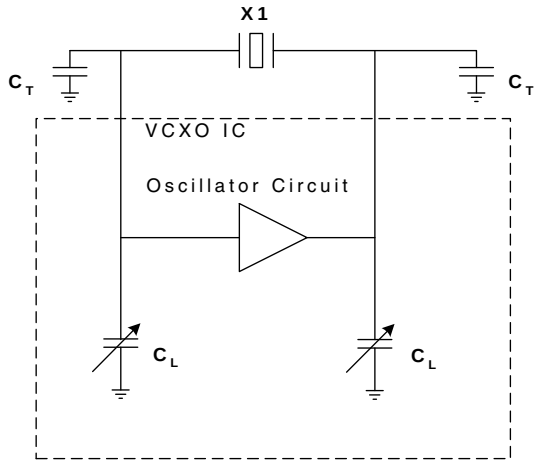

Figure 1 - VCXO Circuit

3. Load capacitance. This is the capacitance, specified in picofarads (pF), which the oscillator circuit presents to the crystal for the crystal to resonate on frequency. Load Capacitance is comprised of a combination of the circuits' discrete load capacitance, stray board capacitance, and capacitance internal to the device. Because this includes the stray capacitance of the circuit board, we recommend that pads for small capacitors (CT in figure 1) be provided in your layout to make small adjustments to the total capacitance. Details are given in the Layout Considerations section.

4. Equivalent Series Resistance. This is a term that represents (in ohms) all the losses within the crystal. If this value is too high, the oscillator may have startup problems.

5. Aging. This specifies the amount that the frequency is allowed to drift, long term, and is typically 5ppm in the first year, and logarithmically declines each year

Additional requirements for VCXO crystals

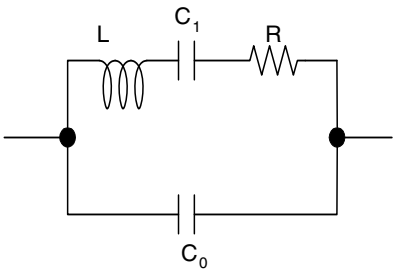

Figure 2 - Equivalent Circuit of a Crystal

The ratio C0/C1 is inversely proportional to pullability; lower ratios indicate a more pullable crystal. Crystals intended for use with IDT VCXOs must have C0/C1 ratio no higher than 250 if they are to meet minimum pull requirements.

Crystals can be made to resonate either at the fundamental frequency, or on the third, fifth, or even higher overtone. VCXO crystals are always fundamental mode, because overtone modes are much less pullable and require additional oscillator circuitry for proper operation.

The third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental, and in a VCXO circuit, the third overtone is not typically exactly three times the fundamental, or the oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the transfer curve such as the one in Figure 3. This potential problem is why VCXO crystals are required to be tested for absence of any activity inside a +/-100 ppm window at three times the fundamental frequency.

Crystals for VCXO applications are always parallel resonant because series resonant oscillators cannot be pulled. The designation for the lattice angle of these

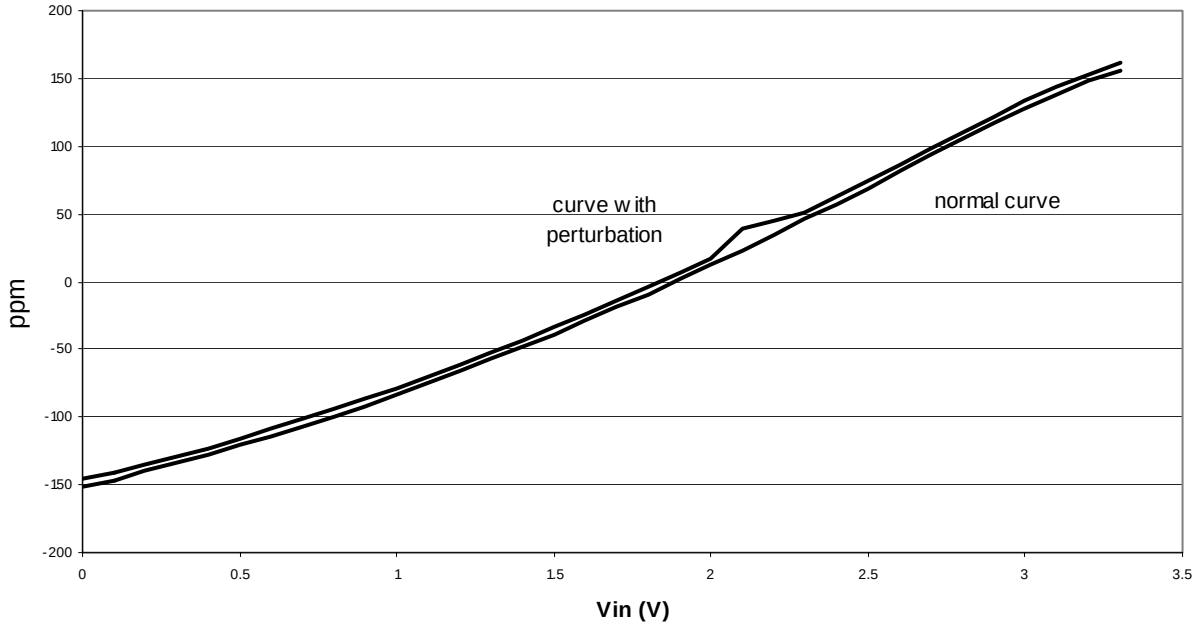

Figure 3 - Perturbation due to third overtone

crystals is AT-cut. Do not use BT cut crystals for IDT VCXO products.

Absolute Pull Range

VCXOs are usually used as a narrowband local frequency source that is locked to some external frequency reference. The VCXO must have sufficient accuracy and pullability to be able to lock to that reference, and Absolute Pull Range is the measure of that ability. All the frequency errors of the VCXO are subtracted from the nominal pull range, and the remaining range can be guaranteed over all conditions. Here is an example using the standard specifications for the recommended crystals:

115 ppm	guaranteed pull range for the IDT VCXO circuit with a minimum pull (C0/C1=250) crystal
-20 ppm	subtract initial accuracy
-30 ppm	subtract temperature stability
-20 ppm	subtract aging
-10 ppm	subtract for circuit variation
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35 ppm	Absolute Pull Range

The VCXO will be able to output a frequency +/- 35ppm under all conditions, which is sufficient for applications such as MPEG transport (32 ppm), SONET (20 ppm), PDH communication links (32 ppm), and others. If your application requires more APR, the best approach is to respecify the crystal to reduce the error terms. Contact IDT for advice.

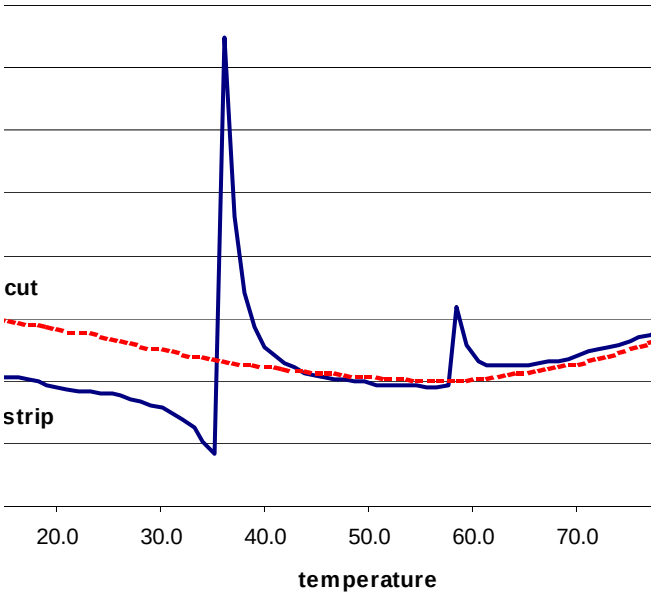
Packaging and Assembly Considerations

The special requirements of a VCXO crystal are best met with a full size AT-cut round quartz crystal blank. Unfortunately, this blank will only fit into the traditional full size HC/49U metal can or the smaller UM1. These packages are available with wire leads for through hole mounting, or a third lead may be added to the top of the crystal can and the three leads may then be formed into a surface mount gull wing device. Smaller surface mount packages, including HC49/US (the "short" can), require a smaller piece of quartz (often called AT strip resonators). The resulting mechanical limitations of strip resonators restrict the performance of the crystal. The smaller electrodes mean that C0/C1 is higher and the pullability spec is harder to meet. Greater mechanical losses in the quartz mean that the ESR specification is harder to meet. And the most subtle and potentially most

Figure 4- The HC/49U or UM1 crystal can be ordered with gull-wing leads for surface mounting.

devastating effect is that, in the smaller crystal, undesired vibrational modes can be active over narrow temperature ranges and cause serious frequency perturbations (also known as activity dips) such as those in figure 6. In this example, severe discontinuities exist at 38 C and 59 C. This could cause unlocking in a feedback control system at these temperatures, yet there is no hint of this problem at room temperature. IDT maintains a list of crystals that have been tested and approved for use with our VCXO chips. Please refer to the "Approved VCXO Crystals" document for a list of IDT approved crystal vendors.

Figure 5 AT-strip temperature perturbation



Printed Circuit Board Layout

Any external parasitic capacitance will reduce the pull range of the VCXO. In order to maximize the range, it is important to minimize parasitic capacitance related to X1 and X2 on the PCB. The ground and power planes should be cut out under the X1 and X2 pins and the crystal. For example, on the MK277X, this cutout should extend under the chip to the right hand side pins 16-20, and down to pin 6. In addition, all signal lines should be routed away from this area to reduce noise pickup.

The crystal must be mounted as close to the device as possible. For maximum flexibility, and since no two board designs are the same, two pads should be included for the connection of optional centering capacitors (CT) from each of the X1 and X2 pins and ground. The value of these capacitors is usually 0-4 pF and needs to be determined only once for each board layout.

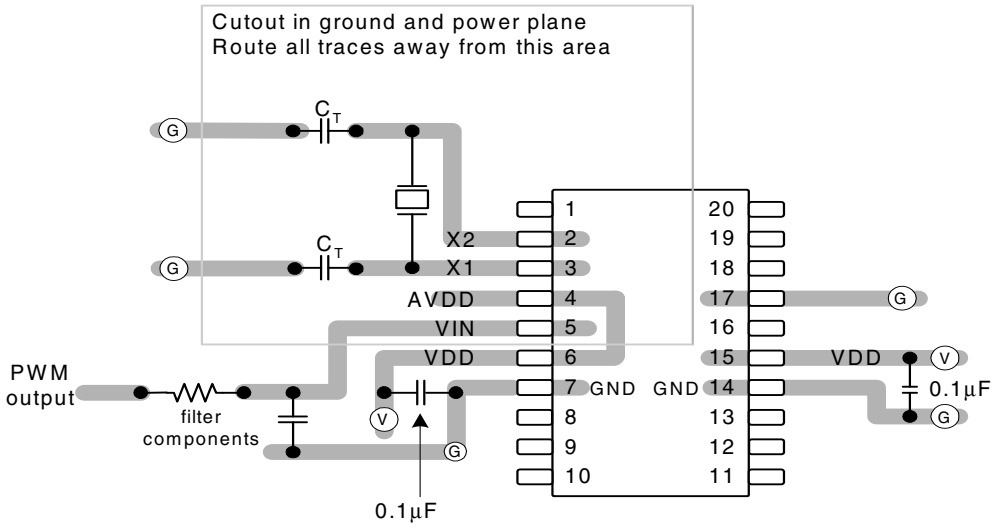
The filter components shown in Figure 6 convert a PWM output into the 0 to 3V analog voltage necessary to drive pin 5. Do not run any other traces underneath the device (other than traces from the device).

Decoupling and Output Termination

The layout of Figure 6 shows two 0.1µF decoupling capacitors connected between pins 6 and 7 and 14 and 15 for the MK277X. These capacitors must be placed as close to the chip as possible. This is the minimum recommended configuration, and will give good results in most applications. For noisy power supplies, an additional 0.1µF can be placed on pin 4, and a 10µF capacitor can be added in parallel.

A series termination resistor of 33Ω may be used for each clock output to match a 50Ω transmission line. This also should be placed close to the device.

Figure 6 - An example of recommended layout - MK2770



Determining Value of Fixed Centering Capacitors

VCXO parts from IDT require that locations be provided to tune the load capacitance of the pullable crystal. This tuning serves to center the crystal's operating frequency relative to the VCXO, thereby increasing the range of frequencies that can be locked-to by the VCXO over that of an untuned board.

The IDT applications department can perform this procedure. Send us two PC boards (stuffed or unstuffed) and we will calculate the value of the capacitors needed.

Many boards will not need any tuning capacitors, but for consistent long-term performance of a system, two load capacitor pads should be put into every design. What follows is the general procedure for tuning these load capacitors to match the specific board layout. Typically, the required capacitors will range from 0 to 4 pF.

Procedure

To determine the need for and value of these capacitors, you will need a PC board of your final layout, a frequency counter capable of less than 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, C_L. In practice, this measurement can be performed at the crystal manufacturer by obtaining datalogged crystals, or by using a crystal tester.

To determine the value of the crystal capacitors:

1. Connect VDD of the part to either 5.0V or 3.3V (depending on part and system requirements). Connect the loop filter voltage to the second power supply. Adjust the voltage for the loop filter to 0V. Measure and record the frequency of the clock output.

2. Adjust the voltage on the loop filter to 3.0V (for a 5 V part) or 3.3V (for a 3.3V part). Measure and record the frequency of the same output (this is f_{high}).

To calculate the centering error:

Centering error

$$= 10^6 \cdot \frac{(f_{high} - f_{target}) + (f_{0v} - f_{target})}{2 \times f_{target}} - error_{xtal}$$

Where:

f_{target} = nominal crystal frequency

$error_{xtal}$ = actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than +/- 15 ppm, no adjustment is needed. If the centering error is more than 15 ppm negative, the PC board has too much stray capacitance and will need to be redone with a new layout to reduce stray capacitance. (The crystal may be re-specified to a higher load capacitance instead. Contact IDT for details.) If the centering rror is more than 15 ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor

= 2 x (centering error)/(trim sensitivity)

Trim sensitivity is a parameter which can be supplied by your crystal vendor or calculated using the following formula:

$$\text{trim sensitivity} = \frac{10^6 \times C_1}{2 \times (C_0 + C_L)^2}$$

If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the measurement to verify that the remaining error is acceptably low (less than ±15ppm).

CL Tuning for 0ppm at VIN=VDD/2

For applications that require VCXO pull curve to be centered at VDD/2, follow external C_L tuning procedure below:

1. Set V_{IN}=1.65 V, measure reference output frequency. Record the measured frequency.

Calculate centering ppm error,

$$\text{ppm error} = (f_{VDD/2} - f_{target}) / f_{target}) * 10^6$$

2. If the error is ±15ppm, no adjustment is needed. If the frequency is -15 ppm or lower, there is no solution except to redo the board layout to reduce stray capacitance.

3. If the centering error is more than 15 ppm positive, add tuning capacitors from each crystal pin (X1/X2) to ground. The value for each of these caps (in pF) is given by:

External Capacitor = 2 x (ppm error)/(trim sensitivity)

Where

$$\text{trim sensitivity} = \frac{10^6 \text{ x } C_1}{2 \text{ x } (C_0 + C_L)^2}$$

4. After calculating the external load caps using the procedure above, and installing them on the board, you can measure the frequency at VIN= 0.0V and VIN= 3.3V. To determine the min and max of the pull range, calculate the ppm error at the measured frequencies ($f_{0.0V}$ and $f_{3.3V}$) and target frequency.

Example calculation

Using a 19.44 MHz pullable crystal, specified at 14 pF load capacitance. With its rated 14 pF load, this crystal is measured to have an output of 19.4405 MHz (26 ppm initial error, positive).

For a MK2058-01, the frequency, using a 0 and 3.3V input on pin 5, for mode SEL[2:0] = 111, the output is measured to be 19.4420 and 19.4410, respectively (in this example, the input frequency and output frequency happen to be the same), yielding a centering error of:

Centering error

$$= 10^6 \cdot \frac{(19.442 - 19.44) + (19.441 - 19.44)}{2 \times 19.44} - 26\text{ppm}$$

= 51 ppm

Assuming a trim sensitivity of 30 ppm/pF, The external capacitors to ground should be:

External capacitor = 2 x 51 / 30 = 3.4 pF.

Rounding to the nearest standard value, two 3.3 pF capacitors should be used.