Introduction

Some of the growing application areas of the VersaClock®LP device are in Smartbooks, Netbooks and E-Book Readers. There are several discrete crystals and oscillators used in these systems that can potentially be replaced with a single clock synthesizer and buffer IC. This can lead to savings in power, board space and cost. This application note provides schematic and layout guidelines that should be considered while designing in the VersaClock®LP device in the above mentioned applications. It also provides an insight into the external clocking requirements of popular processors used in these systems.

External Clocking Needs of Popular Processors

The external clocking needs of 4 popular Netbook, Smartbook and E-book Reader processors are illustrated below.

Samsung 6410

- 32.768 KHz
- 12 MHz

12.288 MHz

125 Clock

48 MHz

27 MHz

Optional

System Peripheral

RTC
PLL x 3
Timer w/ PWM
Watch-Dog Timer
DMA(2 ch)
Keypad (8 x 5)

ARM Core

ARM1176JZF-S
ID-Cache 16KB
ID-TCM 19KB
533/667MHz

Multimedia Acceleration
Camera I/F
Multi Format CODEC
H.264/MPEG4/VC1
NTSC, PAL TV out
(with Image Enhancement)
JPEG
Video Graphics
3D Graphics

Memory Subsystem

SRAM/ROM/ND/OneNAND
Mobile SDRAM
Mobile DDR SDRAM
NAND Flash

Power Management
Normal, Idle
Stop, Sleep

TFT LCD Controller
Resolution typically
800x480
Color: TFT LCD

X84/32 Multi-Layer AHB/AXI Bus

Connectivity
AC97 / PCM Audio I/F
I2S / I2S 5-ch
I2C x 2
UART x 4
GPIO
I/OA v1.1
USB OTG 2.0
USB Host 1.1

Communication
HS-MMC/SD
SPI (Full Duplex)
HIS (Modem I/F)
Samsung 2416

32.768 KHz
12 MHz

ARM Core
ARM926EJ
I/D Cache 16KB/16KB
400MHz @ 1.2V

Multimedia Accelerator
CSC & Scaler
2D Graphics

Connectivity
GPIO
24bit I²S 1x
PCM & AC97
I²C x1
UART x4
IrDA v1.0
1x HS-SPI

Memory Subsystem
SRAM/ROM/NOR/OneNAND
SDRAM x32
Mobile SDRAM x32
mDDR/DDR2 x16
NAND flash
1/4/8bit HW ECC
4KB page read

Power Management
Normal, Idle Stop, Deep Sleep

32bit Multi-layer AHB Bus

TFT LCD Controller
24/18bit or 8bit for Dual i80
1024x1024
output: 2-layer PIP
16bit a-blending

System Peripheral
RTC
PLL x2
Timer w/ PWM
Watch Dog Timer
DMA (8ch)

Multimedia Accelerator

Nvidia T20

32.768 KHz
12 MHz

ARM Core
Cortex-A9
MP4Core Processor

Multimedia Acceleration
Camera I/F
2D Graphics
3D Graphics
JPEG
Multi Format CODEC (H.264/MPEG4)

Memory Subsystem
DDR2 SDRAM
NAND FLASH

Connectivity
PCM Audio I/F
I2S
I2C
UART
USB 2.0
HS-MMC/SD
SPI (Full Duplex)
ULPI
SDIO

Power Management
Normal, Idle
Stop, Sleep

LCD Display Controller
Other than the frequency requirements of the processor, Smartbook, Netbook and E-book Readers may require additional frequencies for the applications listed below.

- LAN (25 MHz typical)
- Bluetooth/Wi-Fi (19.2 MHz / 26 MHz typical)
- GPS (16.368 MHz / 16.369 MHz/ 26 MHz typical)
- Low Power 32.768 kHz clock for PMIC, Bluetooth/Wi-Fi, Keyboard and Embedded Controller

The table in the following page lists the typical input and output frequency requirements in systems using the processors listed above. It also lists the optimal PLL divider and loop filter settings that would need to be set on the VersaClock LP device in order to synthesize the required output frequencies.
## Typical VersaClock LP Configurations

| Application | Processor | PLL Parameters | Output Frequency | Output VDDO (Typical) | Reference Feedback Output (Typical) | Reference Input (Typical) | CRef (nF) | Cc (nF) | Cc'(nF) |  \( \Delta f/

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |

| TI OMAP2430 | 2.4G | 3.3V | 26 | 26 | 12 | 2277 | 2277 | 27 | 0.88 | 300 |
Input Crystal/Clock Selection

The following items need to be considered while selecting the reference crystal/clock source for the VersaClock LP device.

Frequency Accuracy

Different standards impose different requirements for the overall frequency accuracy of the reference clock. Some popular standards with their reference clock frequency accuracy requirements are summarized in the table below.

<table>
<thead>
<tr>
<th>Standard</th>
<th>Frequency Accuracy Across Operating Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth</td>
<td>+/- 20 ppm</td>
</tr>
<tr>
<td>802.11a</td>
<td>+/- 20 ppm</td>
</tr>
<tr>
<td>802.11b/g</td>
<td>+/- 25 ppm</td>
</tr>
<tr>
<td>GPS</td>
<td>+/- 0.5 ppm</td>
</tr>
<tr>
<td>10/100 Ethernet</td>
<td>+/- 100 ppm</td>
</tr>
<tr>
<td>USB</td>
<td>+/- 500 ppm</td>
</tr>
</tbody>
</table>

In general, the frequency tolerance of the VersaClock LP device input clock/crystal should be selected such that the output clocks meet the overall frequency accuracy requirement for all target devices in the system.

Output Clock Phase Noise

The phase noise of the synthesized output clock from the VersaClock LP device depends on the operating bandwidth of the internal PLLs. It is often crucial for the bandwidth of these PLLs to be set optimally in order to keep the phase noise of the synthesized outputs low. The bandwidth of a PLL is often limited by the phase detector rate. Bluetooth, Wi-Fi and GPS ICs are particularly sensitive to the phase noise of the reference clock to their chipset. An ideal scenario would be to generate buffered copies of the VersaClock LP device reference clock and route them directly to these ICs, assuming they require similar reference clock frequencies. More often that not, these ICs are designed to work with multiple reference clock frequencies and finding a common operating frequency is often possible.

Select versions of the VersaClock LP device have a unity gain buffer that preserves the waveshape of the input reference clock and contributes negligible additive phase noise. Other frequencies could then be synthesized from this reference clock. USB and Ethernet Phy standards specify a maximum tolerable RMS filtered phase jitter specification for their reference clocks. Audio Codecs are sensitive to reference clock carrier to noise ratio in addition to phase noise. LCD controllers are sensitive to long term jitter on the reference clock while application processors are sensitive to short term cycle-cycle jitter. In general, for PLL synthesized output clocks, the higher the PLL phase detector rate, the higher is the permissible closed loop bandwidth of the PLL and lower is the overall phase noise and accumulated jitter. If possible, for phase noise critical applications, select an input frequency that will yield the highest phase detector frequency for the PLL.
Crystal Specifications

The following are typical specifications when selecting a crystal to be used as input source to the VersaClock LP device:

### MHz Crystal

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>8 MHz – 30 MHz</td>
</tr>
<tr>
<td>Tolerance over Temperature</td>
<td>±5 PPM – ±50 PPM</td>
</tr>
<tr>
<td>Operating Mode</td>
<td>Fundamental (AT Cut)</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>20pF</td>
</tr>
<tr>
<td>ESR</td>
<td>50 ohms (max)</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0 to 70°C</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>1 mWatt (max)</td>
</tr>
<tr>
<td>Package</td>
<td>SMD Low Profile</td>
</tr>
</tbody>
</table>

### Recommended Crystal Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Web URL</th>
</tr>
</thead>
</table>

### kHz Crystal

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>32.758 kHz</td>
</tr>
<tr>
<td>Tolerance over Temperature</td>
<td>20 PPM (+/- .002%)</td>
</tr>
<tr>
<td>Operating Mode</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>6.0-8.0pF</td>
</tr>
<tr>
<td>ESR</td>
<td>65K ohms (max)</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0 to 70°C</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>0.1 µWatt (max)</td>
</tr>
<tr>
<td>Package</td>
<td>SMT (7 x 1.5 x 1.4 mm)</td>
</tr>
</tbody>
</table>

### Recommended Crystal Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Web URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epson Toyocom</td>
<td><a href="http://www.epsontoyocom.co.jp/english/">http://www.epsontoyocom.co.jp/english/</a></td>
</tr>
<tr>
<td>Citizen</td>
<td><a href="http://www.citizencrystal.com/khz.htm">http://www.citizencrystal.com/khz.htm</a></td>
</tr>
</tbody>
</table>
Recommended Schematic for IDT5P49EE502

Crystal frequency is
application dependent.

USE RESISTOR TO REDUCE XTAL
DRIVE POWER TO 50 uW IF NECESSARY.
OTHERWISE USE 0 OHM RESISTOR.

NOTE: FERRITE BEADS =

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Package Size</th>
<th>DC Res.</th>
<th>Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>muRata</td>
<td>BLM21A601R</td>
<td>600</td>
<td>0.30</td>
<td>500</td>
</tr>
<tr>
<td>TDK</td>
<td>MMZ2012S01A</td>
<td>600</td>
<td>0.30</td>
<td>600</td>
</tr>
<tr>
<td>STEWARD</td>
<td>H208058-601</td>
<td>600</td>
<td>0.30</td>
<td>600</td>
</tr>
<tr>
<td>AssocCmpTch</td>
<td>CBG0805-600-50</td>
<td>600</td>
<td>0.30</td>
<td>600</td>
</tr>
</tbody>
</table>

Manufacture Part Number  2010MHz PkgSz DC res. Current (Ma)
muRata BLM21A601R 600 0.30 500
muRata BLM21A601SN 600 0.50 200
muRata BLM21D601SN1 600 0.65 200
Ceratech HB-171608-601 600 0.50 200
TDK MMZ1608-601P 600 0.20 500

Series resistor for CLKOUTRx
with VDDO = 3.3 Volts.

R1 1 33
Recommended Schematic for IDT5P49EE602

NOTE: FERRITE BEADS =

Manufacture Part Number 28100MHz PkgSz DC res. Current (mA)
muRata BLM21A60UR 600 0805 0.30 500
STEWARD HZ0805E601K 600 0805 0.30 600
Ceratech HB-1T1608-601 600 0805 0.30 200

Manufacture Part Number 28100MHz PkgSz DC res. Current (mA)
muRata BLM8AG601SN1 600 0603 0.50 200
muRata BLM8BD601SN1 600 0603 0.65 200
Ceratech HB-1T1608-601 600 0603 0.50 200

Crystal frequency is application dependent.

USE RESISTOR TO REDUCE XTAL
DRIVE POWER TO 50 uW IF NECESSARY.
OTHER WISE USE 0 OHM RESISTOR.

NOTE: APPLICATION NOTE FOR SMARTBOOKS, NETBOOKS, & E-BOOK READERS

Integrated Device Technology
San Jose, CA

Application Note
Recommended Schematic for IDT5P49EE802
PCB Layout Guidelines

Clocking ICs with regular output transitions can be demanding on voltage and current distribution components such as power supplies, power buses and power planes. The power bus inductance often prevents the rapid energy transfer needed to keep up with the quick output transitions and fast rise/fall times. 0.1µF bypass capacitors placed right next to the VDD pins of the device (as recommended on the schematic) can greatly improve this situation by delivering the required energy in time. Care should be taken while selecting these capacitors.

Bypass Capacitor Selection and Placement

1) Choose a surface mount bypass capacitor (preferably ceramic X5R type) that has a low ESR, low ESL and low impedance at the frequency of interest.

2) Package sizes have an impact on the ESL of the capacitor as well. Choose a small package size '0402' for the bypass capacitor in order to keep the parasitic inductance as low as possible.

3) The length of the trace (if any) from the device power pin to the bypass capacitors should be kept as short as possible to keep the impedance of the bypass path low. The other end of the bypass capacitor is connected to a via going directly to the ground plane. The length of the trace (if any) from the capacitor to the via should be kept as short as possible.

The clock chip may also inject noise into the system power supply and vice versa. A low pass filter formed by a combination of a ferrite bead and capacitor (as recommended on the schematic) is often used to block power supply noise.

Low Pass Filter Component Selection and Placement

1) The Ferrite bead selected should have a maximum DC resistance between 0.4-0.8 ohms with a current rating of at least 200mA.

2) The Ferrite bead should have an impedance of 300 ohms or more at 100 MHz. Try to use a ferrite bead in '0603' package to reduce parasitics.

3) The Ferrite bead should not have a long inductive tail extending to low frequencies. Use the ferrite beads suggested on the schematic for reference.

4) The capacitor to ground should be placed right next to the ferrite bead in order to be effective. This capacitor delivers the power required for low frequency load surges.

5) Choose a 10µF MLCC capacitor for this purpose with low ESR and ESL.

Additionally, the Analog and Digital VDDs need to be isolated for optimal performance. Use an inexpensive resistor and capacitor as recommended on the schematic for this isolation. It is recommended to connect the VersaClock LP device VDDOs (Output Voltages) to the I/O power supply of the chipset that is receiving the clock synthesized from the output that the VDDO voltage controls. In order to minimize signal reflections, connect a 33 ohm series resistor on the outputs.
PCB Stack-up

PCB stack-up can impact the EMC performance of a product greatly. An ideal stack-up can be very effective in reducing the radiation from the loops on the PCB (differential mode emissions) as well as cables connected to the board (common-mode emissions). The five most critical objectives when selecting an ideal PCB stack-up are:

1) Signal layers should always run adjacent to a power plane.
2) Signal layers should be tightly coupled to their reference planes.
3) Power and Ground planes should be closely coupled.
4) Critical signals should be routed on buried layers located between planes. The planes will then act as a shield and constrain the radiation.
5) Having multiple ground planes will lower the ground impedance of the board and reduce common mode radiation.

An 8-layer board can be used to satisfy all the above objectives. The preferred stack-up for an 8-layer board is shown below:

```
| SIGNAL (H) | GND |
| SIGNAL (V) |
| GND        |
| VDD        |
| SIGNAL (H) | GND |
| SIGNAL (V) |
```

The above stack-up has a tightly coupled center power-ground plane for controlling common mode emissions. Critical signals can be routed on signal layers 3 or 6 and be effectively shielded by the planes. 'H' indicates horizontal routing for signals on Layers 1 and 6 while 'V' indicates vertical routing for signals on Layers 3 and 8. Orthogonal routing will help to minimize capacitive coupling between the signals on different layers. This configuration has the added advantage that orthogonal signals always reference the same plane. Typical layer spacing for a 0.060” thick board is 0.006”/0.006”/0.015”/0.006”/0.015”/0.006”/0.006.”
For 6-layer boards, the most common stack-up is shown below:

```
SIGNAL
GND
SIGNAL

SIGNAL
POWER
SIGNAL
```

This stack-up is also fairly good in controlling emissions. The interplane capacitance between power and ground is not significant and external decoupling schemes explained earlier must be followed.

For 4-layer boards, stripling routing of critical signals is often not possible.

### Signal Routing Guidelines

1) Maintain minimum separation of 3 times the clock trace width when routing signal traces adjacent to the clock trace.

2) Maintain minimum separation of 3 times the clock trace width from PCB edges and split planes when routing clock traces.

3) Do not route clock traces across plane splits.

4) If VersaClock LP device is mounted on the top side of the board, the best practice for routing clock traces stripline (for the 8-layer and 6-layer stack-up shown earlier) would be to connect the output series termination resistor (if used) directly to the VersaClock LP device output pins with a very short trace and no vias between the resistor and the device. On the other end of the resistor place a via to the signal layer on Layer 3. For unity gain buffer outputs an AC coupling capacitor can be connected directly to the output of the device at one end and a via to the signal layer on Layer 3 at the other end. When switching signal layers, always route to another signal layer that shares the same reference plane. For the 8-layer and 6-layer board stack-up shown earlier with the VersaClock LP device mounted on the top side, this would imply switching from signal layer on Layer 1 to signal layer on Layer 3 as both these layers have the reference plane (Gnd plane on Layer 2). Avoid routing to signal layers that are adjacent to a different plane.
Errata

The following is the errata list for the VersaClock LP device (at the time this document was created):

- The rms crystal drive current for the MHz oscillator on the VersaClock LP device is around 3.7mA. This results in a power dissipation of around 343µW for a crystal with a typical series resistance of 25ohms. We recommend using a SMD low profile crystal with a power dissipation specification of 500µW or higher with this device.

- The internal load capacitance on XIN and XOUT is fixed to 32pF. This leads to an effective internal load capacitance of 16pF. Factoring in the input pad capacitance, the effective internal capacitance increases to around 18pF. We recommend using a MHz crystal with load capacitance rating of 20pF (accounting for PCB stray capacitance) with this device.

- We recommend using a 32.768 kHz crystal (if required) with 8pF load capacitance rating. The internal load capacitors on X132K and X232K need to be unbalanced to achieve 50% Duty Cycle on the output.

- The output impedance for outputs powered by VDDO = 1.8V is around 80 ohms. Running traces > 1 inch on a system board for outputs power by VDDO = 1.8V is not recommended from a signal integrity standpoint.

- The 32.768 kHz oscillator has a typical operating current of 35µA and the power down current of the VersaClock LP device is around 10µA.

- GPS and wireless module performance cannot be guaranteed with the synthesized clocks from VersaClock LP device.

- Please consult IDT if your jitter requirements are not met on any one of the VersaClock LP device output clocks when programmed with the software generated configuration file.