**Supplemental Information**

This notice describes the differences between the updated version (Version 11, dated August 20, 2009) and its previous version (Version 10, dated October 29, 2008) of the IDT82P2281 Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

**Revision History**

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**Changed Items**

**Aug 20, 2009**

- **Item 35**: Added clock recovery bullet point in APPLICATIONS portion. (Page 12)
- **Item 34**: Added clock recovery paragraph in section ‘3.12 BIT-ORIENTED MESSAGE RECEIVER’. (Page 58)

**Oct 29, 2008**

- **Item 33**: Added SSM bullet point in FEATURES portion. (Page 12)
- **Item 32**: Added SSM paragraph in section ‘3.12 BIT-ORIENTED MESSAGE RECEIVER’. (Page 58)

**Aug 15, 2008**

- **Item 31**: Changed section 7.2 to 7.2.1 and added Tj. (Page 354)
- **Item 30**: Added section 7.2.2 Operating Current Requirements. (Page 354)
- **Item 29**: Added Pmax in section 7.3. (Page 355)

**Feb 26, 2008**

- **Item 28**: Updated Figure 21–24 and Figure 28–31 to clarify the F-bit in T1/J1 mode. (Page 67, 68, 74, 75)

**May 31, 2007**

- **Item 27**: Added E1 Reference Clock Output Control (03EH) register. (Page 257)

**April 6, 2007**
Item 26: Removed the functional descriptions of the SS7 protocol support. (Pages 55, 83, 188, 192, 195, 196, 302, 309, 310)
Item 25: Added the section ‘3.2.1 Line Monitor’. (Pages 24, 25, 26)
Item 24: Changed the E1 mode ‘CRCM, SIGEN, GENCRC’ bite control table. (Page 285)
Item 23: Changed the figure ‘Read Operation In SPI Mode’ and figure ‘Write Operation In SPI Mode’. (Page 105)
Item 22: Added line driver set to ‘3.27.2.6 Analog Loopback’. (Page 102)
Item 21: Changed the paragraph about transmit clock slave mode and transmit clock master mode. (Page 71)
Item 20: Changed the paragraph about non-multiplexed mode. (Pages 69, 71)
Item 19: Changed the paragraph about receive clock slave mode and receive clock master mode. (Page 64)
Item 18: Added bit ‘REFH_LOS’ row to table 5. (Page 26)
Item 17: Changed REFA_OUT pin description. (Page 17)

August 1, 2006
Item 16: Changed package characteristics from PF to PN. (Page 373)

April 12, 2006
Item 15: Changed REFA_OUT pin description. (Page 17)
Item 14: Changed description of internal counters update methods. (Pages 47, 49)
Item 13: Added T1/J1 Reference Clock Output Control Register (03EH) (Page 145)
Item 12: Added green package information (Page 374)

September 1, 2004
Item 11: The description of the DDSINV bit (b3, T1/J1-06FH) is changed. A transition from '0' to '1' on this bit will invert one 6-bit DDS pattern and this bit is cleared when the inversion is completed. (Page 68, 161)
Item 10: The description of the CRCINV bit (b2, T1/J1-06FH) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC pattern and this bit is cleared when the inversion is completed. (Page 68, 161)
Item 9: The description of the FsINV bit (b1, T1/J1-06FH) is changed. A transition from '0' to '1' on this bit will invert one Fs bit in SF and T1 DM formats, invert one Frame Alignment bit in ESF format or invert one Synchronization Fs bit in SLC-96 format and this bit is cleared when the inversion is completed. (Page 161)
Item 8: The description of the FtINV bit (b0, T1/J1-06FH) is changed. A transition from '0' to '1' on this bit will invert one Ft bit in SF, T1 DM and SLC-96 formats and this bit is cleared when the inversion is completed. (Page 161)
Item 7: The description of the CRCINV bit (b5, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert all 4 calculated CRC bits in one Sub-Multi-Frame and this bit is cleared when the inversion is completed. (Page 70, 283)
Item 6: The description of the CRCPINV bit (b4, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert one 6-bit CRC Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 70, 283)
Item 5: The description of the CASPINV bit (b3, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert one 4-bit Signaling Multi-Frame alignment pattern and this bit is cleared when the inversion is completed. (Page 70, 283)
Item 4: The description of the NFASINV bit (b2, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert one NFAS bit and this bit is cleared when the inversion is completed. (Page 70, 283)
Item 3: The description of the FASALLINV bit (b1, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert one 7-bit FAS pattern and this bit is cleared when the inversion is completed. (Page 70, 283)
Item 2: The description of the FAS1INV bit (b0, E1-06FH) is changed. A transition from '0' to '1' on this bit will invert one FAS bit and this bit is cleared when the inversion is completed. (Page 283)
Item 1: In ‘Ordering Information’, the package is changed to ‘PF’. (Page 362)