Using VersaClock™ Products with an Input Clock Source

In order to insure proper startup when using VersaClock™ (ICS34X series) products with an input clock rather than a crystal, the supply voltage must be within the operating range (3.3 V ±10%) and the input signal must be stable and free from glitching. The input clock must provide pulses of at least 20 ns, and no more than 500 ns, for at least 160 clock cycles without any interruptions to the clock or power during this period. It may take up to 4 ms for output frequencies to reach their target frequency values.

An alternative method is to have the $\overline{\text{PDTS}}$ pin asserted low while power supplies and clock sources stabilize. Once the power supply and input clock source are constant and within the acceptable frequency range, bring $\overline{\text{PDTS}}$ high. This approach is preferred if the clock source is derived from another PLL, or the source oscillator produces unpredictable output pulses prior to stabilization.

No considerations need to be taken when using a crystal input source with VersaClock products.

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