Description

The 5P49EE802 is a programmable clock generator intended for low power, battery operated consumer applications. There are four internal PLLs, each individually programmable, allowing for up to eight different output frequencies. The frequencies are generated from a single reference clock. The reference clock can come from either a TCXO or fundamental mode crystal. An additional 32kHz crystal oscillator is available to provide a real time clock or non-critical performance MHz processor clock.

The 5P49EE802 can be programmed through the use of the I^2C interfaces. The programming interface enables the device to be programmed when it is in normal operation or what is commonly known as in system programmable. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up.

Each of the four PLLs has an 8-bit reference divider and a 11-bit feedback divider. This allows the user to generate four unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation. Spread spectrum generation is supported on one of the PLLs.

Spread spectrum generation is supported on one of the PLLs. The device is specifically designed to work with display applications to ensure that the spread profile remains consistent for each HSYNC in order to reduce ROW noise. It also may operate in standard spread spectrum mode.

There are total seven 8-bit output dividers. Outputs are LVCMOS. The outputs are connected to the PLLs via the switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function can be programmed.

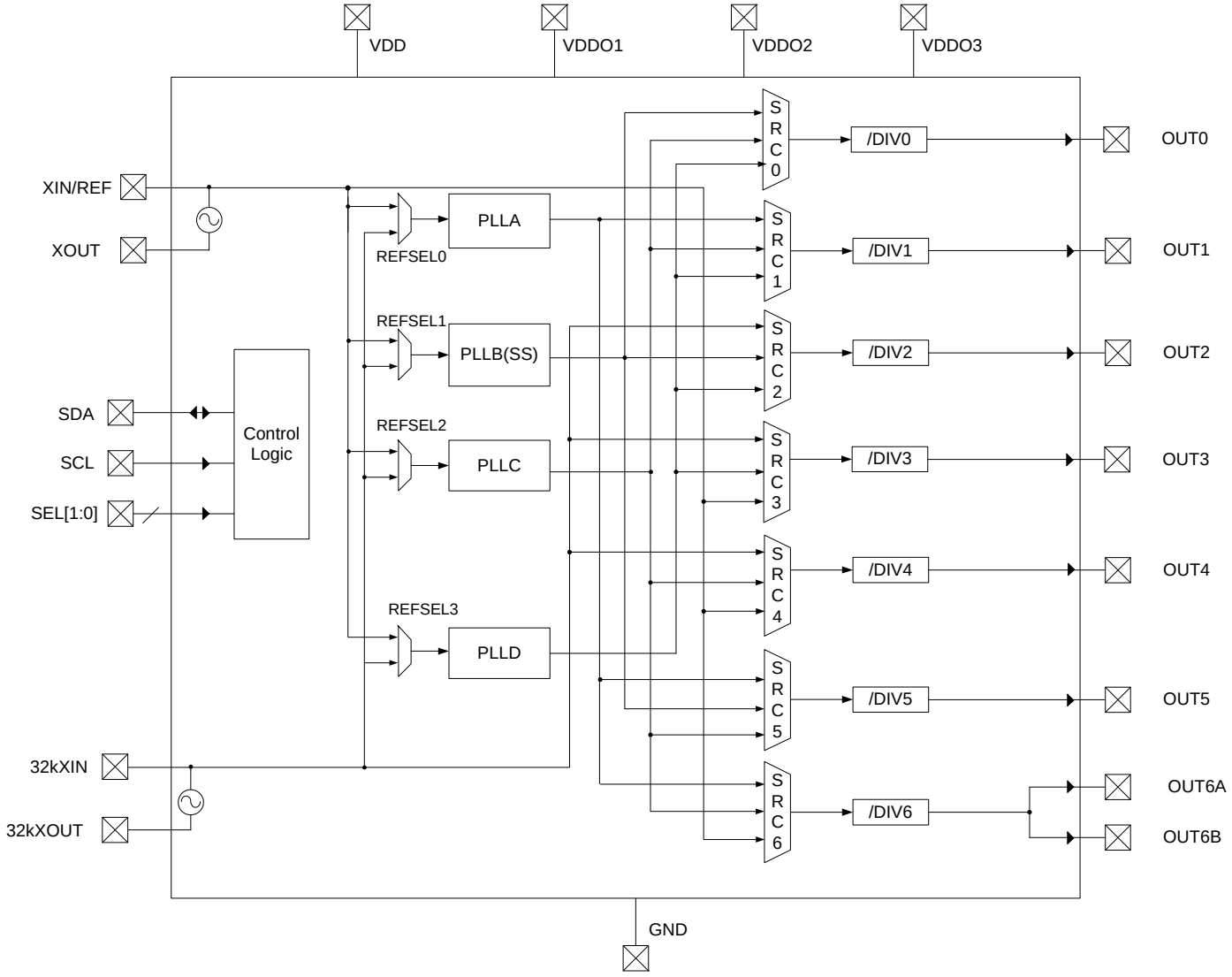
Target Applications

- Smart Mobile Handset
- Personal Navigation Device (PND)
- Camcorder
- DSC
- Portable Game Console
- Personal Media Player

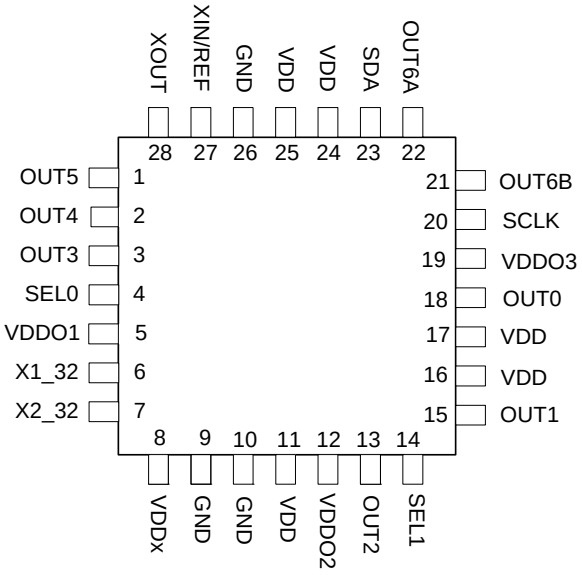
Features

- Four internal PLLs
- Internal non-volatile EEPROM
- Internal I^2C EEPROM master interface
- FAST (400kHz) mode I^2C serial interfaces
- Input Frequencies
  - TCXO: 10 MHz to 40 MHz
  - Crystal: 8 MHz to 30 MHz
  - RTC Crystal: 32.768 kHz
- Output Frequency Ranges: kHz to 120 MHz
- Each PLL has an 8-bit reference divider and a 11-bit feedback-divider
- 8-bit output-divider blocks
- One of the PLLs support Spread Spectrum generation capable of configuration to pixel rate, with adjustable modulation rate and amplitude to support video clock with no visible artifacts
- I/O Standards:
  - Outputs - 1.8V/2.5V/3.3 V LVTTL/ LVCMOS
  - 3 independent adjustable VDDO groups
- Programmable Slew Rate Control
- Programmable Loop Bandwidth Settings
- Programmable output inversion to reduce bimodal jitter
- Individual output enable/disable
- Power-down/Sleep mode
  - 10µA max in power down mode
  - 32kHz clock output active sleep mode
  - 100µA max in sleep mode
- 1.8V VDD Core Voltage
- Available in 28 pin 4x4mm QFN packages
- -40 to +85°C Industrial Temp operation

Functional Block Diagram



Pin Assignment



28 pin VFQFPN
(Top View)

Pin Descriptions

Pin Name	Pin #	I/O	Pin Type	Pin Description
OUT5	1	O	Adjustable	Configurable clock output 5. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
OUT4	2	O	Adjustable	Configurable clock output 4. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
OUT3	3	O	Adjustable	Configurable clock output 3. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
SEL0*	4	I	LVTTL	Configuration select pin. Weak internal pull down resistor.
VDDO1	5		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT6. VDDO1 must be greater than or equal to both VDDO2 and VDDO3.
X132k	6	I	LVTTL	32kHz CRYSTAL_IN -- Reference crystal input
X232k	7	I	LVTTL	32kHz CRYSTAL_OUT -- Reference crystal feedback.
VDDx	8		Power	Crystal oscillator power supply. Connect to 1.8V. Use filtered analog power supply if available.
GND	9		Power	Connect to Ground.
GND	10		Power	Connect to Ground.
VDD	11		Power	Device power supply. Connect to 1.8V.
VDDO2	12		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT5.
OUT2	13	O	Adjustable	Configurable clock output 2. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
SEL1*	14	I	LVTTL	Configuration select pin. Weak internal pull down resistor.
OUT1	15	O	Adjustable	Configurable clock output 1. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.

Pin Name	Pin #	I/O	Pin Type	Pin Description
VDD	16		Power	Device power supply. Connect to 1.8V.
VDD	17		Power	Device power supply. Connect to 1.8V.
OUT0	18	O	Adjustable	Configurable clock output 0. Single-ended output voltage levels are register controlled by either VDDO1, VDDO2 or VDDO3.
VDDO3	19		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT5.
SCLK	20	I	LVTTL	I^2C clock. Logic levels set by VDDO1. 5V tolerant.
OUT6B	21	O	Adjustable	Configurable clock output 6B. Output voltage levels are controlled by VDDO1.
OUT6A	22	O	Adjustable	Configurable clock output 6A. Output voltage levels are controlled by VDDO1.
SDA	23	I/O	LVTTL	Bidirectional I^2C data. Logic levels set by VDDO1. 5V tolerant.
VDD	24		Power	Device power supply. Connect to 1.8V.
VDD	25		Power	Device power supply. Connect to 1.8V.
GND	26		Power	Connect to Ground.
XIN/ REF	27	I	LVTTL	MHz CRYSTAL_IN -- Reference crystal input or external reference clock input. Maximum clock input voltage is 1.8V.
XOUT	28	O	LVTTL	MHz CRYSTAL_OUT -- Reference crystal feedback. Float pin if using reference input clock.

Note *: SEL pins should be controlled by 1.8V LVTTL logic; 3.3V tolerant.

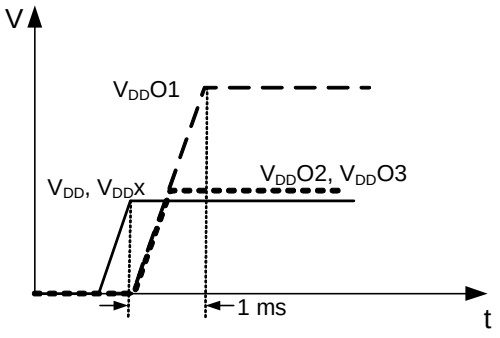
Note 1: Outputs are user programmable to drive single-ended 1.8V/2.5V/3.3V LVTTL as indicated above. Always completely power up VDD and VDDx prior to applying VDDO power.

Note 2: Default factory configuration OUT4=buffered reference output & OUT2=32.768KHz. All other outputs are off.

Note 3: Do not power up with SEL[1:0] = 00 (in Power down/Sleep mode).

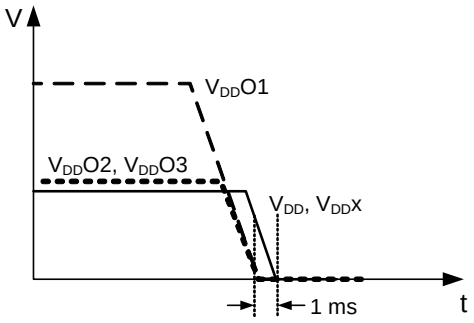
Ideal Power Up Sequence

1) V_{DD} and $V_{DD}x$ must come up first, followed by $V_{DD}O$
2) $V_{DD}O1$ must come up within 1ms after VDD and VDDX come up
3) $V_{DD}O2/3$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2/3$ have approx. same ramp rate

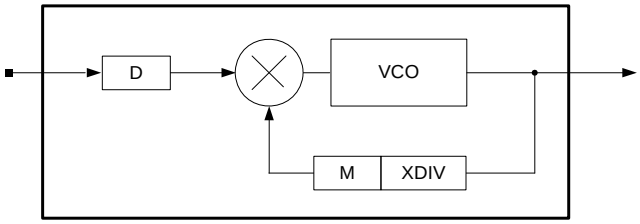


Ideal Power Down Sequence

1) $V_{DD}O$ must drop first, followed by V_{DD} and $V_{DD}x$
2) V_{DD} and $V_{DD}x$ must come down within 1ms after $V_{DD}O1$ comes down
3) $V_{DD}O2/3$ must be equal to, or lower than, $V_{DD}O1$
4) V_{DD} and $V_{DD}x$ have approx. the same ramp rate
5) $V_{DD}O1$ and $V_{DD}O2/3$ have approx. same ramp rate



PLL Features and Descriptions



PLL Block Diagram

	Ref-Divider (D) Values	Feedback Pre-Divider (XDIV) Values	Feedback (M) Values	Programmable Loop Bandwidth	Spread Spectrum Generation Capability
PLLA	1 - 255	1 or 4	6 - 2047	Yes	No
PLLB	1 - 255	4	6 - 2047	Yes	Yes
PLLC	1 - 255	1 or 8 bit divide	6 - 2047	Yes	No
PLLD	1 - 255	1 or 4	6 - 2047	Yes	No

Crystal Input (XIN/REF)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. 0

ONXTALB=0 bit needs to be set for XIN/REF.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The crystal capacitors are internal to the device and have an effective value of 4pF.

Reference Pre-Divider, Reference Divider, Feedback-Divider and Post-Divider

Each PLL incorporates an 8-bit reference-scaler and a 11-bit feedback divider which allows the user to generate four unique non-integer-related frequencies. PLLA and PLLD each have a feedback pre-divider that provides additional multiplication for kHz reference clock applications. Each output divider supports 8-bit post-divider. The following equation governs how the output frequency is calculated.

$$F_{OUT} = \frac{F_{IN} * \left(\frac{XDIV*M}{D}\right)}{ODIV} \quad \text{(Eq. 2)}$$

Where F_{IN} is the reference frequency, XDIV is the feedback pre-divider value, M is the feedback-divider value, D is the reference divider value, ODIV is the total post-divider value, and F_{OUT} is the resulting output frequency. Programming any of the dividers may cause glitches on the outputs.

Spread Spectrum Generation (PLLB)

PLLB has spread spectrum generation capability, which users have the option of turning on and off. Spread spectrum profile, frequency, and spread are fully programmable (within limits). The programmable spread spectrum generation parameters are NC[10:0], MOD[12:0], and NSS[10:0] bits. To enable spread spectrum, set SSENB_B=0.

The spread spectrum circuitry was specifically developed to accommodate video display applications. The spread modulation frequency can be defined to exactly equal the horizontal line frequency (HSYNC)

NC[10:0]

These bits are used to determine the number of pulses per spread spectrum cycle. For video applications, NC is the number of pixels on the horizontal display row (or integer multiple of displayed pixels in a row). By matching the spread period to the screen, no tearing or “shimmer” will be apparent.

NC must be an even number to insure that the upward spread transition has the same number of steps as the downward spread transition.

For non-video applications, this can also be seen as the number of clock cycles for a complete spread spectrum period.

MOD[12:0]

These bits relate the VCO frequency to the target average spread output frequency (F_{MID}).

$F_{MID} = (F_{VCO}) / 8$

$F_{MAX} = F_{MID} + (SS\% * F_{MID})$

$F_{MIN} = F_{MID} - (SS\% * F_{MID})$

$MOD = (F_{REF} * NC) / (2 * F_{MID})$

NSS[10:0]

These bits control the amplitude of the spread modulation.

$NSS = (NC / 2) + (NC / 8) * (F_{MAX} - F_{MIN}) / F_{MID}$

Modulation frequency:

$F_{MOD} = F_{MID} / NC$ (Eq. 11)

Video Example

F_{REF} = 27 MHz, F_{OUT} = 27 MHz, 640 pixels per line, center spread of ±1%. Using F_{VCO}=432MHz, find the necessary spread spectrum register settings.

$F_{MID} = F_{VCO}/8$

NC = 640 (integer number of spread periods/screen)

MOD = (25MHz * 640)/(2 * 54MHz) = 160

NSS = (640/2)+(640/8)*(27.27MHz-26.73MHz)/27MHz = 321.

F_{MOD} = 27MHz/640 = 11.8kHz.

Non-Video Example

F_{REF} = 25MHz, F_{OUT} = 27 MHz, 31.25kHz modulation rate, center spread of ±1%. Find the necessary spread spectrum register settings.

$F_{MID} = F_{VCO}/ 8$

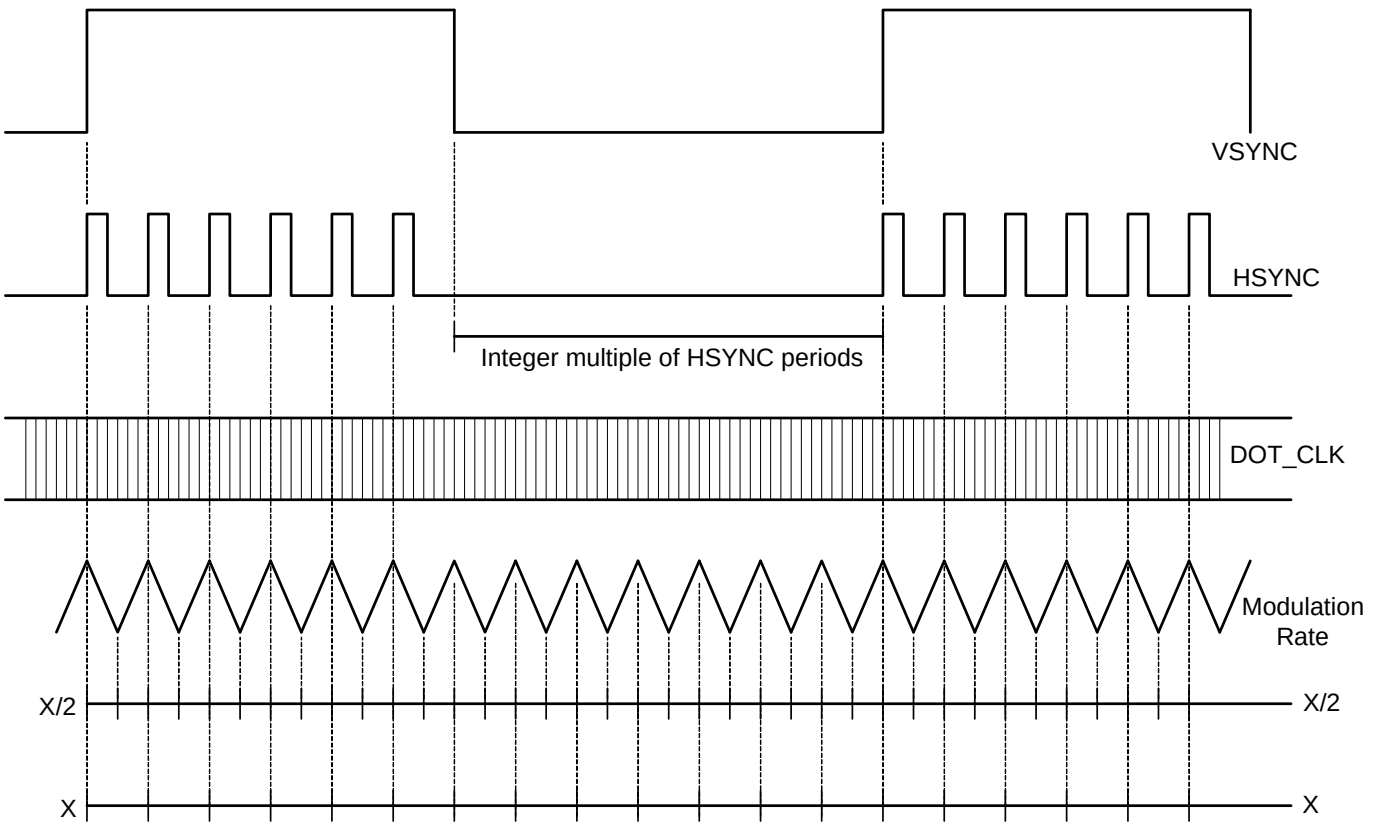
F_{MOD} = 31.25kHz = 50.625MHz/NC.

NC = 1620

MOD = (25MHz * 1620)/(2 * 50.625MHz) = 400

NSS = (1620/2)+(1620/8)*(27.27MHz-26.73MHz)/27MHz = 814.

VSYNC, HSYNC, DOT_CLK – Modulation Rate Relationship

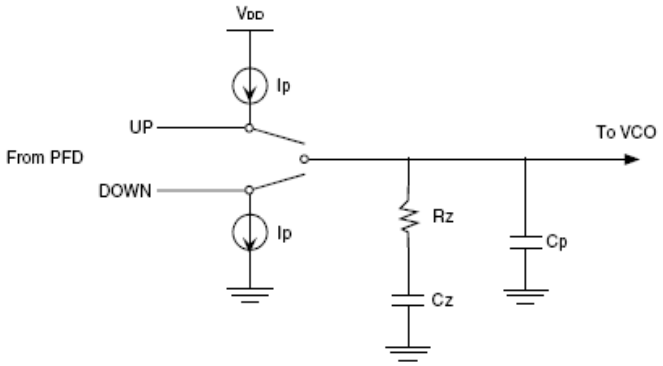


X = Number of cycles of DOT_CLK per HSYNC period.

X/2 = Number of cycles of DOT_CLK that the modulation edge rises/falls.

Loop Filter

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low jitter generation. The specific loop filter components that can be programmed are the resistor via the RZ[4:0] bits, zero capacitor via the CZ[2:0] bits, pole capacitor via the CP[1:0] bits, and the charge pump current via the IP#[2:0] bits.



The following equations govern how the loop filter is set:

Zero capacitor (Cz) = 280pF

Pole capacitor (Cp) = 30pF

Charge pump (Ip) = IP#[2:0] uA

VCO gain (K_{VCO}) = 350MHz/V * 2π

PLL Loop Bandwidth:

Charge pump gain ($K\phi$) = Ip / 2π

VCO gain (K_{VCO}) = 350MHz/V * 2π

M = Total multiplier value (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail)

$\omega c = (Rz * K\phi * K_{VCO} * Cz)/(M * (Cz + Cp))$

$Fc = \omega c / 2\pi$

Note, the phase/frequency detector frequency (F_{PFD}) is typically seven times the PLL closed-loop bandwidth (Fc) but too high of a ratio will reduce your phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin (ϕm) would need to be calculated as follows.

Phase Margin:

$\omega z = 1 / (Rz * Cz)$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp)$

$\phi m = (360 / 2\pi) * [\tan^{-1}(\omega c/ \omega z) - \tan^{-1}(\omega c/ \omega p)]$

To ensure stability in the loop, the phase margin is recommended to be > 60° but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

Damping Factor:

$\zeta = Rz/2 *(K_{VCO} * Ip * Cz)^{1/2}/M$

Example

Fc = 150KHz is the desired loop bandwidth. The total A*M value is 160. The ζ (damping factor) target should be 0.7, meaning the loop is critically damped. Given Fc and A*M, an optimal loop filter setting needs to be solved for that will meet both the PLL loop bandwidth and maintain loop stability.

Choose a mid-range charge pump from register table

Icp= 11.9uA.

$K\phi * K_{VCO}$ = 350MHz/V * 40uA = 12000A/Vs

$\omega c = 2\pi * Fc = 9.42x10^5\ s^{-1}$

$\omega p = (Cz + Cp)/(Rz * Cz * Cp) = \omega z\ (1 + Cz / Cp)$

Solving for Rz, the best possible value Rz=30kOhms (RZ[1:0]=10) gives

ζ= 1.4 (Ideal range for ζ is 0.7 to 1.4)

Solving back for the PLL loop bandwidth, Fc=149kHz.

The phase margin must be checked for loop stability.

$\phi m = (360 / 2\pi) * [\tan^{-1}(9.42x10^5\ s^{-1} / 1.19x10^5 s^{-1})$
$- \tan^{-1}(9.42x10^5\ s^{-1} / 1.23x10^6\ s^{-1})] = 45°$

The phase margin would be acceptable with a fairly stable loop.

SEL[1:0] Function

The 5P49EE802 can support up to three unique configurations. Users may pre-program all configurations, selected using SEL[1:0] pins. Alternatively, users may use I2C interface to configure these registers on- the-fly.

Always power with SEL1=1 and/or SEL0=1.

Power Down/Sleep Mode is selected by the No_PD bit. No_PD=0 enables Power Down mode with no outputs. No_PD=1 enables sleep mode with 32kHz output on OUT2.

.

SEL1	SEL0	Configuration Selections
0	0	Power Down/Sleep Mode
0	1	Select CONFIG0
1	0	Select CONFIG1
1	1	Select CONFIG2

Configuration OUTx IO Standard

Users can configure the individual output IO standard from a single 3.3V power supply. Each output can support 1.8V/ 2.5V or 3.3V LVCMOS. VDDO1 must have the highest voltage of any pin on the device. VDDO2 and VDDO3 may have any value between 1.8V and VDDO1.

Programming the Device

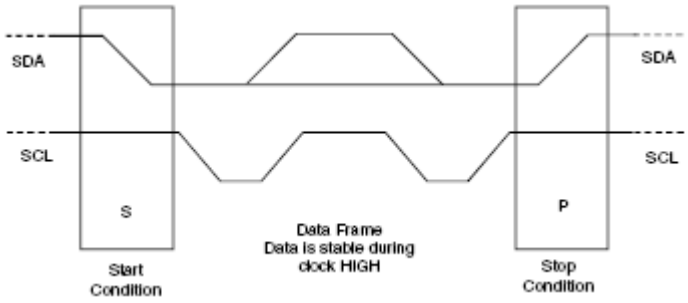
I^2C may be used to program the 5P49EE802.

– Device (slave) address = 7'b1101010

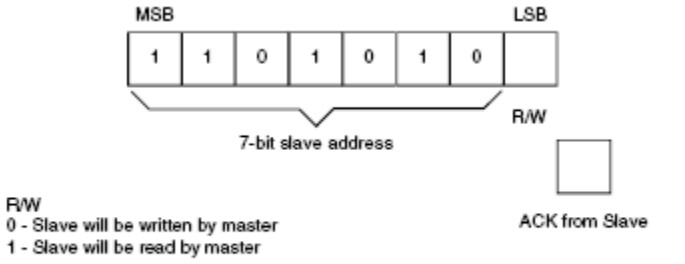
I^2C Programming

The 5P49EE802 is programmed through an I^2C-Bus serial interface, and is an I^2C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing



The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a "1" bit.

First Byte Transmitted on I^2C Bus

External I²C Interface Condition

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence
Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDA LOW)
NACK - Not Acknowledge (SDA HIGH)
Sr - Repeated Start Condition
S - START Condition
P - STOP Condition

EEPROM Interface

The 5P49EE802 can store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I²C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the 5P49EE802 will not generate Acknowledge bits. The 5P49EE802 will acknowledge the instructions after it has completed execution of them. During that time, the I²C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5P49EE802, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The 5P49EE802 will be ready to accept a programming instruction once it acknowledges its 7-bit I²C address.

Progwrite

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	8-bits	1-bit	

Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

Progread

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	

Prior to Progread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Progread command):

S	Address	R/$\overline{W}$	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

Progread Command Frame

Progsave

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx01	1-bit	

Note:
PROGWRITE is for writing to the 5P49EE802 registers.
PROGREAD is for reading the 5P49EE802 registers.
PROGSAVE is for saving all the contents of the 5P49EE802 registers to the EEPROM.
PROGRESTORE is for loading the entire EEPROM contents to the 5P49EE802 registers.

Progrestore

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx10	1-bit	

During PROGRESTORE, outputs will be turned off to ensure that no improper voltage levels are experienced before initialization.

I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level		0.7xVDDO1		5.5	V
V_{IL}	Input LOW Level				0.3xVDDO1	V
V_{HYS}	Hysteresis of Inputs		0.05xVDDO1			V
I_{IN}	Input Leakage Current	V_{DD} = 0V			±1.0	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

I²C Bus AC Characteristics for Standard Mode

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		100	kHz
t_{BUF}	Bus free time between STOP and START	4.7			µs
$t_{SU:START}$	Setup Time, START	4.7			µs
$t_{HD:START}$	Hold Time, START	4			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	250			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			3.45	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCLK)			1000	ns
t_F	Fall Time, data and clock (SDA, SCLK)			300	ns
t_{HIGH}	HIGH Time, clock (SCLK)	4			µs
t_{LOW}	LOW Time, clock (SCLK)	4.7			µs
$t_{SU:STOP}$	Setup Time, STOP	4			µs

1) **No activity is allowed on I2C lines until VDD>1.62V.**

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

I^2C Bus AC Characteristics for Fast Mode

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCL)	0		400	kHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDA)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDA) [1]	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_F	Fall Time, data and clock (SDA, SCL)	$20 + 0.1xC_B$		300	ns
t_{HIGH}	HIGH Time, clock (SCL)	0.6			µs
t_{LOW}	LOW Time, clock (SCL)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

1) **No activity is allowed on I2C lines until VDD>1.62V.**

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P49EE802. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Description	Max	Unit
V_{DD}	Internal Power Supply Voltage	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +4.6	V
V_O	Output Voltage (not to exceed 4.6 V)	-0.5 to V_{DD}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD} , V_{DD}x	Power supply voltage for core VDD	1.71	1.8	1.89	V
V_{DDOX}	Power supply voltage for outputs VDDO1/2/3	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Operating temperature, ambient	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVTTL only)			15	pF
C_{LOAD_OUT}	Maximum load capacitance (1.8V or 2.5V LVTTL only)			8	pF
F_{IN}	External reference crystal	8		30	MHz
	External reference clock CLKIN	1		40	
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

Capacitance (T_A = +25 °C, f = 1 MHz, V_{IN} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance		3		pF
Crystal Specifications					
XTAL_FREQ	Crystal frequency	8		30	MHz
XTAL_MIN	Minimum crystal load capacitance		7		pF
XTAL_MAX	Maximum crystal load capacitance		20		pF

DC Electrical Characteristics for 3.3V LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 33mA	2.4		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 33mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

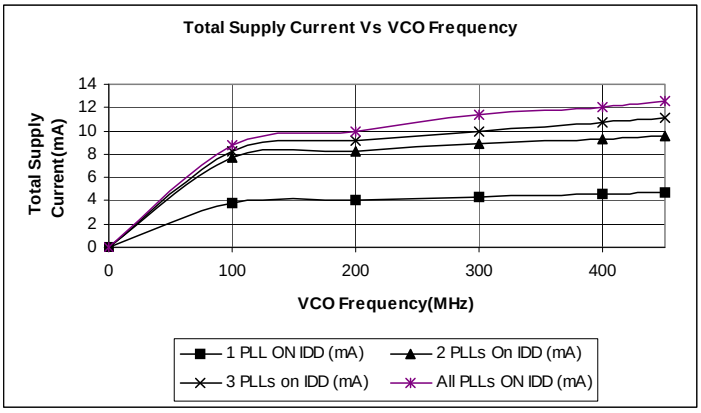
DC Electrical Characteristics for 2.5V LVTTL [1]

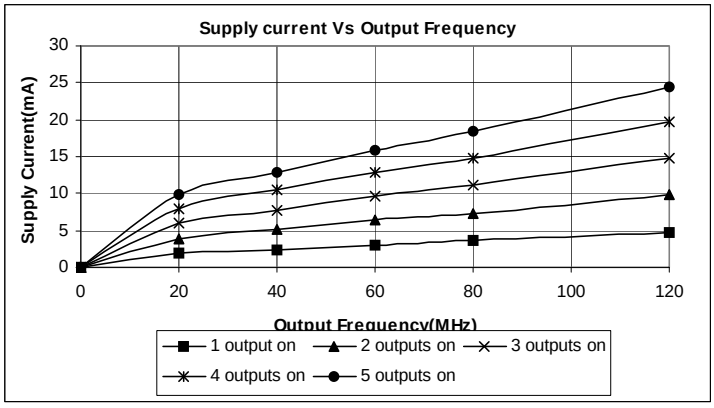
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 25mA	2.1		VDDO	V
V_{OL}	Output LOW Voltage	I_{OH} = 25mA			0.4	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

DC Electrical Characteristics for 1.8V LVTTL [1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	VDDO = 1.71V to 1.89V	1.23		VDDO	V
V_{OL}	Output LOW Voltage				0.6	V
V_{IH}	Input HIGH Voltage	SEL[1:0], 3.3V tolerant	1.35			V
V_{IL}	Input LOW Voltage	SEL[1:0], 3.3V tolerant			0.45	V
I_{OZDD}	Output Leakage Current	3-state outputs			5	µA

Power Supply Characteristics for LVTTL Outputs





Note 1: See “Recommended Operating Conditions” table. Alway completely power up VDD and VDDx prior to applying VDDO power.

AC Timing Electrical Characteristics for 3.3V

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Input Frequency Limit (CLKIN)	1 [1]		40	MHz
1 / t1	Output Frequency	Single Ended Clock output limit (LVTTL) 3.3V	0.001		120	MHz
f_{VCO}	VCO Frequency	VCO operating Frequency Range	100		475	MHz
t2	Input Duty Cycle	Duty Cycle for Input	40		60	%
t3	Output Duty Cycle	Measured at VDD/2	45		55	%
t4	Slew Rate, SLEWx(bits) = 00	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		5.1		V/ns
	Slew Rate, SLEWx(bits) = 01	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		3.8		
	Slew Rate, SLEWx(bits) = 10	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		2.6		
	Slew Rate, SLEWx(bits) = 11	Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD Output Load = 7 pF)		1.8		
t5	Clock Jitter[3]	Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Single output frequency only.			150	ps
		Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Multiple output frequencies switching.			200	ps
t6	Output Skew	Skew between output to output on the same bank			75	ps
		Skew between any output (Same freq and IO type, FOUT >10MHz)			200	ps
t7	Lock Time	PLL Lock Time from Power-up (using MHz reference clock)[1]		5	20	ms
		PLL Lock Time from Power-up using 32.768kHz reference clock)		1	3	s
		PLL Lock time from shutdown mode		5	10	ms

1.Input clock (square wave) may be used at 1 MHz.

2. Time from supply voltage crosses VDD=1.62V to PLLs are locked.

3. Not guaranteed until customer specific configuration is approved by IDT.

AC Timing Electrical Characteristics for 2.5V

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Input Frequency Limit (CLKIN)	1 [1]		40	MHz
1 / t1	Output Frequency	Single Ended Clock output limit (LVTTL) 2.5V	0.001		110	MHz
f_{VCO}	VCO Frequency	VCO operating Frequency Range	100		475	MHz
t2	Input Duty Cycle	Duty Cycle for Input	40		60	%
t3	Output Duty Cycle	Measured at VDD/2	45		55	%
t4	Slew Rate, SLEWx(bits) = 00	Single-Ended 2.5V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		3.6		V/ns
	Slew Rate, SLEWx(bits) = 01	Single-Ended 2.5V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		2.0		
	Slew Rate, SLEWx(bits) = 10	Single-Ended 2.5V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		1.4		
	Slew Rate, SLEWx(bits) = 11	Single-Ended 2.5V LVCMOS Output clock rise and fall time, 20% to 80% of VDD Output Load = 7 pF)		1.0		
t5	Clock Jitter[3]	Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Single output frequency only.			150	ps
		Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Multiple output frequencies switching.			200	ps
t6	Output Skew	Skew between output to output on the same bank			75	ps
		Skew between any output (Same freq and IO type, FOUT >10MHz)			200	ps
t7	Lock Time	PLL Lock Time from Power-up (using MHz reference clock)[1]		5	20	ms
		PLL Lock Time from Power-up using 32.768kHz reference clock)		1	3	s
		PLL Lock time from shutdown mode		5	10	ms

1.Input clock (square wave) may be used at 1 MHz.

2. Time from supply voltage crosses VDD=1.62V to PLLs are locked.

3. Not guaranteed until customer specific configuration is approved by IDT.

AC Timing Electrical Characteristics for 1.8V

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Input Frequency Limit (CLKIN)	1 [1]		40	MHz
1 / t1	Output Frequency	Single Ended Clock output limit (LVTTL) 1.8V	0.001		100	MHz
f_{VCO}	VCO Frequency	VCO operating Frequency Range	100		475	MHz
t2	Input Duty Cycle	Duty Cycle for Input	40		60	%
t3	Output Duty Cycle	Measured at VDD/2	45		55	%
t4	Slew Rate, SLEWx(bits) = 00	Single-Ended 1.8V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		1.3		V/ns
	Slew Rate, SLEWx(bits) = 01	Single-Ended 1.8V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		0.8		
	Slew Rate, SLEWx(bits) = 10	Single-Ended 1.8V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF)		0.6		
	Slew Rate, SLEWx(bits) = 11	Single-Ended 1.8V LVCMOS Output clock rise and fall time, 20% to 80% of VDD Output Load = 7 pF)		0.4		
t5	Clock Jitter[3]	Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Single output frequency only.			300	ps
		Peak-to-peak period jitter, CLK outputs measured at VDD/2; f_{PFD} >= 10 MHz Multiple output frequencies switching.			400	ps
t6	Output Skew	Skew between output to output on the same bank			75	ps
		Skew between any output (Same freq and IO type, FOUT >10MHz)			200	ps
t7	Lock Time	PLL Lock Time from Power-up (using MHz reference clock)[1]		5	20	ms
		PLL Lock Time from Power-up using 32.768kHz reference clock)		1	3	s
		PLL Lock time from shutdown mode		5	10	ms

1.Input clock (square wave) may be used at 1 MHz.

2. Time from supply voltage crosses VDD=1.62V to PLLs are locked.

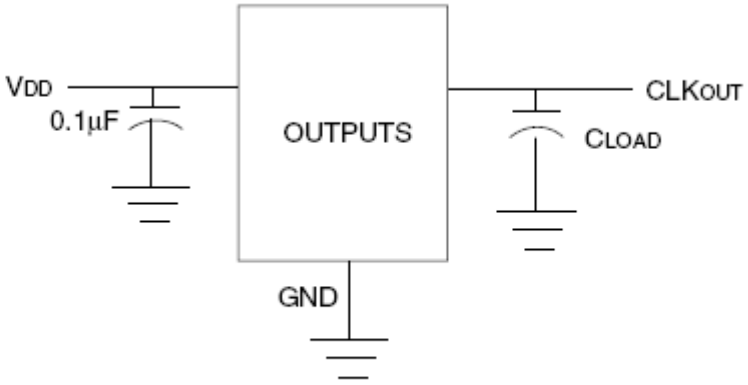
3. Not guaranteed until customer specific configuration is approved by IDT.

Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f_{IN}	Input Frequency	Input Frequency Limit	1 [1]		40	MHz
f_{MOD}	Mod Frequency	Modulation Frequency[3]	32		120	kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (programmable) - Down Spread	Programmable			$\%f_{OUT}$
		Amount of Spread Value (programmable) - Center Spread	Programmable			
		Total Spread Value	0.5		4.0	

1. Practical lower frequency is determined by loop filter settings.
2. Modulation spread percentage is tested on every part and trimming for guaranteed accuracy.
3. Not guaranteed until customer specific configuration is approved by IDT.

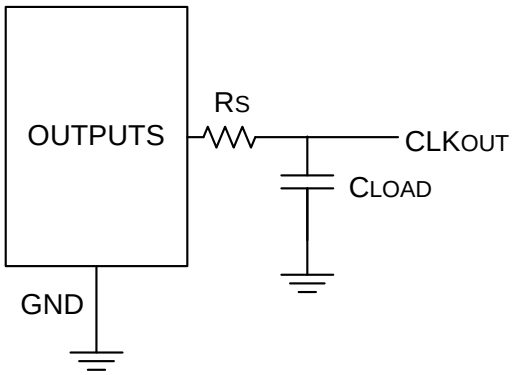
Test Circuits and Conditions [1]



NOTE:
1. All VDD pins must be tied together.

Test Circuits for DC Outputs

Other Termination Scheme (Block Diagram)



Total load capacitance = 7pF

Programming Registers Table

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x00	0	ONXTALB	CSX2[1:0]		CSX1[1:0]		XTAL32ONB	Reserved		ONXTALB - MHz Crystal active low CSX2 [1:0]- internal 32kHz crystal cap2 00 - 18pF; 10 - 30pF 01 - 24pF; 11 - 36pF CSX1 [1:0] - Internal 32kHz crystal cap1 00 - 0pF; 10 - 6pF 01 - 3pF; 11 - 9pF XTAL32ONB - 32k crystal active low
0x01	4	INV[0]	SLEW0[1:0]		No_PD	PS0[2:1]		Reserved		No_PD - Enables/Disables 32kHz clock output on Config 00. No_PD=0 - 32kHz is off. No_PD=1 - 32kHz remains active. INV[#] - Invert output# SLEW#[0:1] - output# slew setting 0 0 - 5.1V/ns 0 1 - 4.4V/ns 1 0 - 2.8V/ns 1 1 - 1.8V/ns PS#[2:1] -Power Select 00 - Reserved 01 - CLK# connects to VDDO1 10 - CLK# connects to VDDO2 11 - CLK# connects to VDDO3
0x02	0	Reserved								
0x03	0	INV[1]	SLEW1[1:0]		Reserved	PS12:1]		Reserved		
0x04	4	INV[2]	SLEW2[1:0]		Reserved	PS2[2:1]		Reserved		
0x05	0	Reserved								
0x06	10	INV[3]	SLEW3[1:0]		Reserved	PS3[2:1]		Reserved		
0x07	4	INV[4]	SLEW4[1:0]		Reserved	PS42:1]		Reserved		
0x08	4	INV[5]	SLEW5[1:0]		Reserved	PS5[2:1]		Reserved		
0x09	0	INV[6B]	INV[6A]	SLEW6[0:1]		Reserved				
0x0A	0	Reserved								
0x0B	0	Reserved								
0x0C	0	Reserved								
0x0D	0	Reserved								
0x0E	0	REFA[7:0]								Configuration0 REFA[7:0] - Reference Divide PLLA
0x0F	4	FBA[10:3]								FBA[10:0] - Feedback Divide PLLA
0x10	0	Reserved					FBA[2:0]			
0x11	1A	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			REFSELA	XDIVA - FB predivide PLLA; 0 - /1; 1 - /4 RZA[1:0] - Zero Resistor PLLA 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPA[2:0] - charge Pump Current PLLA 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELA - Clock input PLLA 0 - MHz input 1 - 32kHz input
0x12	0	REFB[7:0]								REFB[7:0] - Reference Divide PLLB
0x13	1	FBB[10:3]								FBB[10:0] - Feedback Divide PLLB

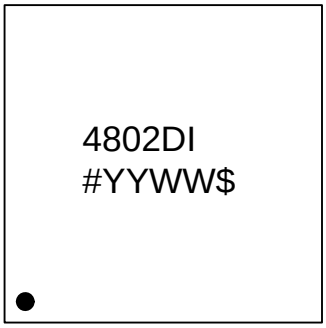
Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x14	8	MOD[4:0]					FBB[2:0]			PLLB Spread Parameters MOD[12:0] NC[10:0] NSS[12:0]
0x15	11	MOD[12:5]								
0x16	7D	NC[10:3]								
0x17	90	NSS[4:0]					NC[2:0]			
0x18	1F	NSS[12:5]								
0x19	55	Reserved			IPB[2:0]			RZB[1:0]		RZB[1:0] - Zero Resistor PLLB 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPB[2:0] - charge Pump Current PLLB 000 - 0.37uA, 100 - 6.3uA 001 - 1.1uA, 101 - 11.9uA 010 - 1.8 uA, 110 - 17.7uA 011 - 3.4uA, 111 - 22.7uA REFSELB - Clock input PLLB 0 - MHz input 1 - 32kHz input
0x1A	1	Reserved						REFSELB	SSENB_B	
0x1B	0	REFC[7:0]								REFC[7:0] - Reference Divide PLLC
0x1C	30	FBC[10:3]								FBC[10:0] - Feedback Divide PLLC
0x1D	0	Reserved					FBC[2:0]			
0x1E	A	FBC2[7:0]								FBC2 - Feedback Predivide PLLC Turn on using XDIVC=1
0x1F	B0	IPC[2:0]			RZC[1:0]		Reserved	XDIVC	REFSELC	RZC[1:0] - Zero Resistor PLLC 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPC[2:0] - charge Pump Current PLLC 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELC 0 - MHz input 1 - 32kHz input
0x20	0	REFD[7:0]								REFD[7:0] - Reference Divide PLLD
0x21	3	FBD[10:3]								FBD[10:0] - Feedback Divide PLLD
0x22	0	Reserved					FBD[2:0]			
0x23	30	XDIVD	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		XDIVD - FB predivide PLLD; 0 - /1; 1 - /4 RZD[1:0] - Zero Resistor PLLD 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPD[2:0] - charge Pump Current PLLD 100 - 6.3uA 101 -11.9 uA 110 - 17.7 uA 111 - 22.7uA REFSELD[1:0] 00 - MHz input 11 - 32kHz input Others - Reserved

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x24	5	OD0[7:0]								OD#[7:0] - Output Divide#
0x25	C	Reserved								
0x26	F	OD1[7:0]								
0x27	1	OD2[7:0]								
0x28	12	Reserved								
0x29	8	OD3[7:0]								
0x2A	1	OD4[7:0]								
0x2B	4	OD5[7:0]								
0x2C	4	OD6[7:0]								
0x2D	A8	SCR6[1:0]		SCR5[1:0]		SCR4[1:0]		SCR3[1:0]		SRC6[1:0] - OD6 source 00 - off; 10 - PLLC 01 - PLLA; 11 - MHz Reference SRC5[1:0] - OD5 source 00 - off; 10 - PLLA 01 - PLLC; 11 - PLLB SRC4[1:0] - OD4 source 00 - off; 10 - MHz Reference 01 - PLLC; 11 - 32kHz Reference SRC3[1:0] - OD3 source 00 - off; 10 - 32kHz Reference 01 - MHz Reference; 11 - PLLD
0x2E	10	Reserved		SCR2[1:0]		SCR1[1:0]		Reserved		SRC2[1:0] - OD2 source 00 - off; 10 - PLLB 01 - 32kHz Reference; 11 - PLLD SRC1[1:0] - OD1 source 00 - off; 10 - PLLC 01 - PLLA; 11 - PLLD
0x2F	1	SCR0[1:0]		Reserved						SRC0[1:0] - OD0 source 00 - off; 10 - PLLC 01 - PLLB; 11 - PLLD
0x30	FF	Reserved								
0x31	B0	PDB[6]	Reserved	OE[6B]	OE[6A]	Reserved				PDB[#] - Powerdown OUT#. PDB[#]=0, OUT# driven low OE[#] - Output enable OUT#. OE[#]=0, OUT# tri-stated. If PDB#=OE#=0, OUT# driven low
0x32	FF	OE[5]	OE[4]	OE[3]	Reserved	OE[2]	OE[1]	Reserved	OE[0]	
0x33	FF	PDB[5]	PDB[4]	PDB[3]	Reserved	PDB[2]	PDB[1]	Reserved	PDB[0]	

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x34	0	REFA[7:0]								Configuration1 (See definitions from Configuration0 above)
0x35	1	FBA[10:3]								
0x36	0	Reserved					FBA[2:0]			
0x37	5A	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			REFSELA	
0x38	0	REFB[7:0]								
0x39	1	FBB[10:3]								
0x3A	8	MOD[4:0]					FBB[2:0]			
0x3B	11	MOD[12:5]								
0x3C	7D	NC[10:3]								
0x3D	90	NSS[4:0]					NC[2:0]			
0x3E	1F	NSS[12:5]								
0x3F	55	Reserved			IPB[2:0]			RZB[1:0]		
0x40	1	Reserved						REFSELB	SSENB_B	
0x41	0	REFC[7:0]								
0x42	30	FBC[10:3]								
0x43	0	Reserved					FBC[2:0]			
0x44	A	FBC2[7:0]								
0x45	B0	IPC[2:0]			RZC[1:0]		Reserved	XDIV	REFSELC	
0x46	0	REFD[7:0]								
0x47	0	FBD[10:3]								
0x48	6	Reserved					FBD[2:0]			
0x49	B0	XDIVD	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		
0x4A	5	OD0[7:0]								
0x4B	C	Reserved								
0x4C	F	OD1[7:0]								
0x4D	5	OD2[7:0]								
0x4E	16	Reserved								
0x4F	8	OD3[7:0]								
0x50	1	OD4[7:0]								
0x51	4	OD5[7:0]								
0x52	1	OD6[7:0]								
0x53	DC	SCR6[1:0]		SCR5[1:0]		SCR4[1:0]		SCR3[1:0]		
0x54	20	Reserved		SCR2[1:0]		SCR1[1:0]		Reserved		
0x55	C1	SCR0[1:0]		Reserved						
0x56	FF	Reserved								
0x57	B0	PDB[6]	Reserved	OE[6B]	OE[6A]	Reserved				
0x58	FF	OE[5]	OE[4]	OE[3]	Reserved	OE[2]	OE[1]	Reserved	OE[0]	
0x59	FE	PDB[5]	PDB[4]	PDB[3]	Reserved	PDB[2]	PDB[1]	Reserved	PDB[0]	

Addr	Default Register Hex Value	Bit # 7	6	5	4	3	2	1	0	Description
0x5A	0	REFA[7:0]								Configuration2 (See definitions from Configuration0 above)
0x5B	4	FBA[10:3]								
0x5C	0	Reserved					FBA[2:0]			
0x5D	1A	Reserved	XDIVA	RZA[1:0]		IPA[2:0]			REFSELA	
0x5E	0	REFB[7:0]								
0x5F	1	FBB[10:3]								
0x60	8	MOD[4:0]					FBB[2:0]			
0x61	11	MOD[12:5]								
0x62	7D	NC[10:3]								
0x63	90	NSS[4:0]					NC[2:0]			
0x64	1F	NSS[12:5]								
0x65	55	Reserved			IPB[2:0]			RZB[1:0]		
0x66	1	Reserved						REFSELB	SSENB_B	
0x67	0	REFC[7:0]								
0x68	30	FBC[10:3]								
0x69	0	Reserved					FBC[2:0]			
0x6A	A	FBC2[7:0]								
0x6B	B0	IPC[2:0]			RZC[1:0]		Reserved	XDIV	REFSELC	
0x6C	0	REFD[7:0]								
0x6D	3	FBD[10:3]								
0x6E	0	Reserved					FBD[2:0]			
0x6F	30	XDIVD	RZD[1:0]		IPD[2:0]			REFSELD[1:0]		
0x70	4	OD0[7:0]								
0x71	C	Reserved								
0x72	F	OD1[7:0]								
0x73	1	OD2[7:0]								
0x74	16	Reserved								
0x75	8	OD3[7:0]								
0x76	1	OD4[7:0]								
0x77	5	OD5[7:0]								
0x78	4	OD6[7:0]								
0x79	78	SCR6[1:0]		SCR5[1:0]		SCR4[1:0]		SCR3[1:0]		
0x7A	10	Reserved		SCR2[1:0]		SCR1[1:0]		Reserved		
0x7B	81	SCR0[1:0]		Reserved						
0x7C	FF	Reserved								
0x7D	B0	PDB[6]	Reserved	OE[6B]	OE[6A]	Reserved				
0x7E	FF	OE[5]	OE[4]	OE[3]	Reserved	OE[2]	OE[1]	Reserved	OE[0]	
0x7F	FF	PDB[5]	PDB[4]	PDB[3]	Reserved	PDB[2]	PDB[1]	Reserved	PDB[0]	

Marking Diagram (NL28)



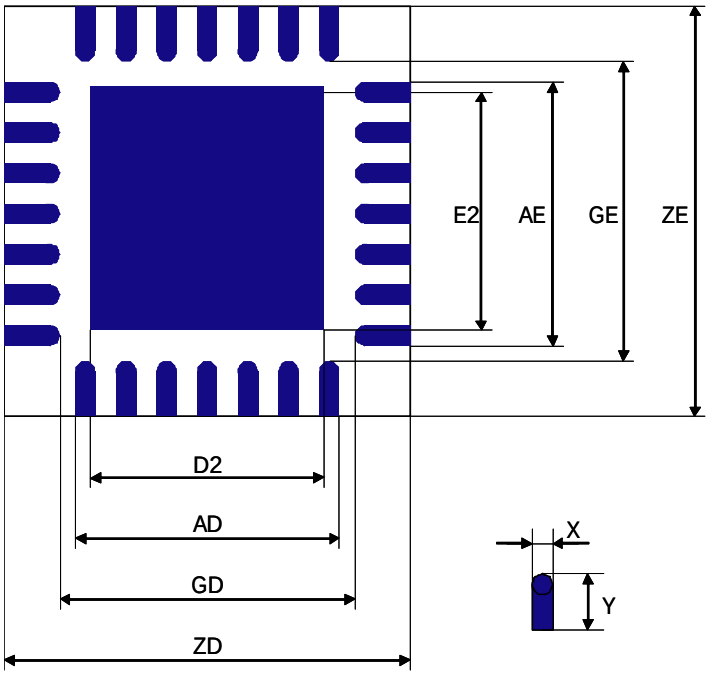
Notes:

1. "#" is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "$" is the assembly mark code.
4. "I" indicates industrial temperature range.

Thermal Characteristics 28-pin VFQFPN

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		48.6		°C/W
	θ_{JA}	1 m/s air flow		41.7		°C/W
	θ_{JA}	2.5 m/s air flow		37.7		°C/W
Thermal Resistance Junction to Case	θ_{JC}			55.1		°C/W

Landing Pattern

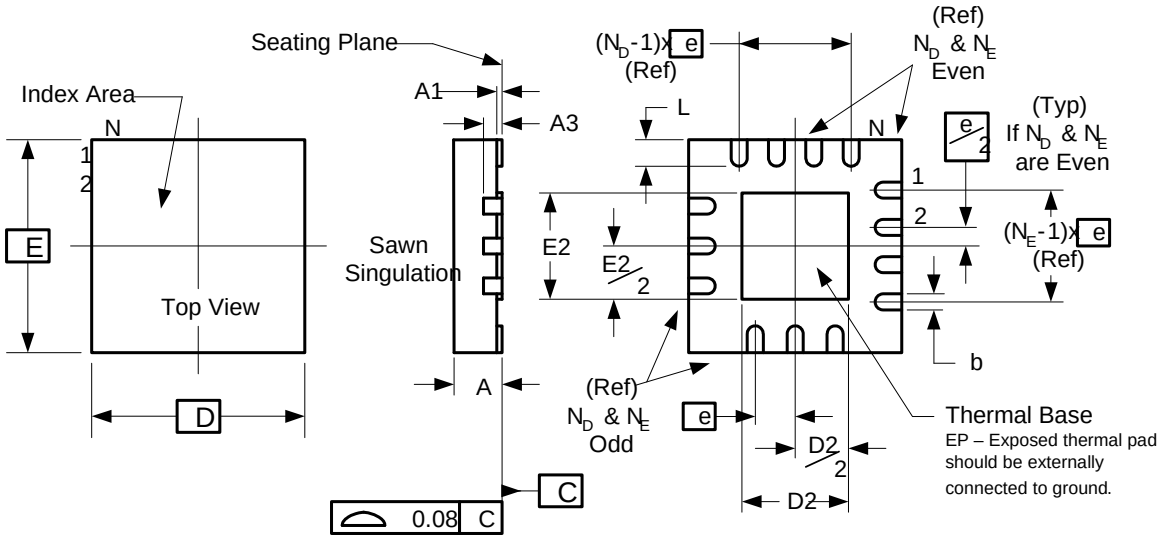


Dimensions	
X(max)	0.25
Yref	0.76
A(max)	2.65
G(min)	2.9
Z(max)	4.41
E2/D2(max)	2.7

Unit : mm

Package Outline and Package Dimensions (28-pin 4mm x 4mm QFN)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.20 Reference	
b	0.15	0.25
e	0.40 BASIC	
N	28	
N_D	7	
N_E	7	
D x E BASIC	4.00 x 4.00	
D2	2.50	2.70
E2	2.50	2.70
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P49EE802NDGI	See page 26	Tray	28-pin VFQFPN	-40° to +85°C
5P49EE802NDGI8		Tape and Reel	28-pin VFQFPN	-40° to +85°C

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
--	10/14/09	R.Willner	Initial Preliminary Datasheet
A	11/20/09	R.Willner	No_PD bit inclusion - 32kHz clock on/off in Config 00.
B	3/25/10	R.Willner	Typographical changes. Correct spread spectrum calculations.
C	6/02/10	R.Willner	Typographical changes. Default configuration.
D	9/08/10	R.Willner	Updated thermal pad and dimensions on package drawing. Input Clock max voltage swing 1.8V. Power ramp sequence.
E	10/29/10	R. Willner	Typographical changes. Loop filter calculations. Default register bit corrections.
F	01/19/11	R. Willner	Corrected notes for top-side marking.
G	04/13/11	R. Willner	1. Updated SCLK and SDA pin descriptions 2. Updated DC Electrical Char table for 1.8V LVTTL; added VIH and VIL. 3. Updated “Lock Time/PLL Lock Time from shutdown mode” Typ. and Max. specs in AC Timing Electrical Char table.
H	05/04/11	R. Willner	Added Landing Pattern diagram.
J	08/24/11	R. Willner	Corrected SRC1 connections in block diagram.
K	0930/11	R. Willner	Updated Power-up/Power-down Sequence notes.
L	10/17/11	R. Willner	1. Added VDDOx specs to Recomended Operations table 2. Updated Power-up/down Sequence diagrams
M	07/25/12	R. Willner	1. Added pin 1 indicator dot on marking diagram. 2. Corrected typo in Register Map table; SLEWx[0:1] was changed to SLEWx[1:0]
N	09/10/15	A. Borodulin	1. Corrected minor textual typos throughout. 2. Update VOH/VOL and VIH/VIL values in 1.8V LVTTL DC table. 3. Update t4 and t5 specs in AC Electrical Characteristics table; added specific 3.3V to title. 4. Created separate 2.5V and 1.8V Ac Electrical Characteristics tables. 5. Added footnotes to Spread Spectrum Generation table.
P	04/01/16	Z. Bhinder	1. Updated Default register Hex values throughout entire Programming Registers table. 2. Updated note 2 under Pin Descriptions.

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