Features

- **True Dual-Ported memory cells** which allow simultaneous reads of the same memory location
- **High-speed access**
  - Commercial: 15/20ns (max.)
  - Industrial: 20ns (max.)
- **Low-power operation**
  - IDT7028L
    - Active: 1W (typ.)
    - Standby: 1mW (typ.)
- **Dual chip enables allow for depth expansion without external logic**
- **IDT7028 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device**
- **M/Ś = VIH for BUSY output flag on Master,**
  **M/Ś = VIL for BUSY input on Slave**
- **Interrupt Flag**
- **On-chip port arbitration logic**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Fully asynchronous operation from either port**
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **TTL-compatible, single 5V (±10%) power supply**
- **Available in a 100-pin TQFP**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram

NOTES:

1. BUSY is an input as a Slave (M/Ś = VIL) and an output when it is a Master (M/Ś = VIH).
2. BUSY and INT are non-tri-state totem-pole outputs (push-pull).
Description

The IDT7028 is a high-speed 64K x 16 Dual-Port Static RAM. The IDT7028 is designed to be used as a stand-alone 1024K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (CE0 and CE1) permit the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 1W of power.

The IDT7028 is packaged in a 100-pin Thin Quad Flatpack (TQFP).

Pin Configurations

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part marking.
### Pin Names

<table>
<thead>
<tr>
<th>Left Port</th>
<th>Right Port</th>
<th>Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE&lt;sub&gt;L&lt;/sub&gt;, CE&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>CE&lt;sub&gt;R&lt;/sub&gt;, CE&lt;sub&gt;IR&lt;/sub&gt;</td>
<td>Chip Enables</td>
</tr>
<tr>
<td>R/W&lt;sub&gt;L&lt;/sub&gt;</td>
<td>R/W&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Read/Write Enable</td>
</tr>
<tr>
<td>OE&lt;sub&gt;L&lt;/sub&gt;</td>
<td>OE&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Output Enable</td>
</tr>
<tr>
<td>A0L - A15L</td>
<td>A0R - A15R</td>
<td>Address</td>
</tr>
<tr>
<td>I/O0L - I/O15L</td>
<td>I/O0R - I/O15R</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>SEM&lt;sub&gt;L&lt;/sub&gt;</td>
<td>SEM&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Semaphore Enable</td>
</tr>
<tr>
<td>UBL</td>
<td>UBR</td>
<td>Upper Byte Select</td>
</tr>
<tr>
<td>LR</td>
<td>LBR</td>
<td>Lower Byte Select</td>
</tr>
<tr>
<td>INTL</td>
<td>INTR</td>
<td>Interrupt Flag</td>
</tr>
<tr>
<td>BUSYL</td>
<td>BUSYR</td>
<td>Busy Flag</td>
</tr>
<tr>
<td>M/S</td>
<td></td>
<td>Master or Slave Select</td>
</tr>
<tr>
<td>Vcc</td>
<td></td>
<td>Power</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Commercial &amp; Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to +7.0 V</td>
<td>V</td>
</tr>
<tr>
<td>T&lt;sub&gt;BIAS&lt;/sub&gt;</td>
<td>Temperature Under Bias</td>
<td>-55 to +125 °C</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;TSTG&lt;/sub&gt;</td>
<td>Storage Temperature</td>
<td>-65 to +150 °C</td>
<td>°C</td>
</tr>
<tr>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>DC Output Current</td>
<td>50 mA</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>Input High Voltage</td>
<td>2.2</td>
<td>—</td>
<td>6.0(2)</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Input Low Voltage</td>
<td>-0.5(1)</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTES:**
1. V<sub>L</sub> ≥ -1.5V for pulse width less than 10ns.
2. V<sub>TERM</sub> must not exceed Vcc + 10%.

### Capacitance

**(Ta = +25°C, f = 1.0MHz)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Capacitance</td>
<td>V&lt;sub&gt;H&lt;/sub&gt; = 3dV</td>
<td>9</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Output Capacitance</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; = 3dV</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

### Maximum Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>GND</th>
<th>Vcc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This is the parameter Ta. This is the “instant on” case temperature.
### Truth Table I: Chip Enable(1,2)

<table>
<thead>
<tr>
<th>CE</th>
<th>(\overline{CE_0})</th>
<th>(\overline{CE_1})</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>(V_{IL})</td>
<td>(V_{IL})</td>
<td>Port Selected (TTL Active)</td>
</tr>
<tr>
<td></td>
<td>(\leq 0.2V)</td>
<td>(\geq V_{CC} - 0.2V)</td>
<td>Port Selected (CMOS Active)</td>
</tr>
<tr>
<td>H</td>
<td>(V_{IH})</td>
<td>(X)</td>
<td>Port Deselected (TTL inactive)</td>
</tr>
<tr>
<td></td>
<td>(X)</td>
<td>(V_{IL})</td>
<td>Port Deselected (TTL inactive)</td>
</tr>
<tr>
<td></td>
<td>(\geq V_{CC} - 0.2V)</td>
<td>(X)</td>
<td>Port Deselected (CMOS inactive)</td>
</tr>
<tr>
<td></td>
<td>(X)</td>
<td>(\leq 0.2V)</td>
<td>Port Deselected (CMOS inactive)</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Chip Enable references are shown above with the actual \(\overline{CE_0}\) and \(\overline{CE_1}\) levels, \(\overline{CE}\) is a reference only.
2. \(\text{\'H\'} = V_{IH} \text{ and } \text{\'L\'} = V_{IL}\).
3. CMOS standby requires \(\text{\'X\'}\) to be either \(\leq 0.2V\) or \(\geq V_{CC} - 0.2V\).

### Truth Table II: Non-Contention Read/Write Control

<table>
<thead>
<tr>
<th>(CE)</th>
<th>(R/W)</th>
<th>(OE)</th>
<th>UB</th>
<th>LB</th>
<th>SEM</th>
<th>I/O8-15</th>
<th>I/O0-7</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>Deselected: Power-Down</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>DATAIN</td>
<td>H</td>
<td>Write to Upper Byte Only</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>DATAIN</td>
<td>DATAIN</td>
<td>Write to Lower Byte Only</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>DATAIN</td>
<td>DATAIN</td>
<td>Write to Both Bytes</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>DATAOUT</td>
<td>High-Z</td>
<td>Read Upper Byte Only</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>DATAOUT</td>
<td>DATAOUT</td>
<td>Read Lower Byte Only</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Outputs Disabled</td>
</tr>
</tbody>
</table>

**NOTES:**
1. \(A_{SL} \neq A_{SR} \neq A_{SL} \neq A_{SR}\).
2. Refer to Chip Enable Truth Table.

### Truth Table III: Semaphore Read/Write Control(1)

<table>
<thead>
<tr>
<th>CE(2)</th>
<th>(R/W)</th>
<th>(OE)</th>
<th>UB</th>
<th>LB</th>
<th>SEM</th>
<th>I/O8-15</th>
<th>I/O0-7</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DATAOUT</td>
<td>DATAOUT</td>
<td>Read Data in Semaphore Flag</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>DATAOUT</td>
<td>DATAOUT</td>
<td>Read Data in Semaphore Flag</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>DATAIN</td>
<td>DATAIN</td>
<td>Write I/O into Semaphore Flag</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>DATAIN</td>
<td>DATAIN</td>
<td>Write I/O into Semaphore Flag</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>——</td>
<td>——</td>
<td>Not Allowed</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>——</td>
<td>——</td>
<td>Not Allowed</td>
</tr>
</tbody>
</table>

**NOTES:**
1. There are eight semaphore flags written to via I/O0 and read from all the I/Os (I/O0-I/O15). These eight semaphore flags are addressed by A0-A2.
2. Refer to Chip Enable Truth Table.
### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>7028L</th>
</tr>
</thead>
<tbody>
<tr>
<td>[IL]</td>
<td>Input Leakage Current (1)</td>
<td>VCC = 5.5V, VIN = 0V to VCC</td>
<td>—</td>
</tr>
<tr>
<td>[ILo]</td>
<td>Output Leakage Current</td>
<td>CE = VH, VOUT = 0V to VCC</td>
<td>—</td>
</tr>
<tr>
<td>Vol</td>
<td>Output Low Voltage</td>
<td>IOL = 4mA</td>
<td>—</td>
</tr>
<tr>
<td>Voh</td>
<td>Output High Voltage</td>
<td>IOH = -4mA</td>
<td>2.4</td>
</tr>
</tbody>
</table>

**NOTES:**
1. At VCC < 2.0V, input leakages are undefined.
2. Refer to Chip Enable Truth Table.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Version</th>
<th>7028L15</th>
<th>7028L20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td>Dynamic Operating Current (Both Ports Active)</td>
<td>CE = VIH, Outputs Disabled, SEM = VIH, f = fMAX(2)</td>
<td>COM’L L</td>
<td>220</td>
<td>340</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>ISB1</td>
<td>Standby Current (Both Ports - TTL Level Inputs)</td>
<td>CE = CE = VIH, SEMR = SEML = VIH, f = fMAX(2)</td>
<td>COM’L L</td>
<td>65</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>75</td>
</tr>
<tr>
<td>ISB2</td>
<td>Standby Current (One Port - TTL Level Inputs)</td>
<td>CE = VIH and CE = VIH, SEM = SEML = VIH, f = fMAX(2), SEMR = SEMR = VIH</td>
<td>COM’L L</td>
<td>145</td>
<td>225</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>130</td>
<td>195</td>
</tr>
<tr>
<td>ISB3</td>
<td>Full Standby Current (Both Ports - All CMOS Level Inputs)</td>
<td>Both Ports CE = VIH and CE = VIH, SEMR = SEML = VIH, or SEMR = SEML = VIH, f = fMAX(2)</td>
<td>COM’L L</td>
<td>0.2</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.2</td>
<td>3.0</td>
</tr>
<tr>
<td>ISB4</td>
<td>Full Standby Current (One Port - All CMOS Level Inputs)</td>
<td>CE = VIH and CE = VIH, SEMR = SEML = VIH, or SEMR = SEML = VIH, f = fMAX(2)</td>
<td>COM’L L</td>
<td>135</td>
<td>220</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>190</td>
</tr>
</tbody>
</table>

**NOTES:**
1. VCC = 5V, TA = +25°C, and are not production tested. ICCDC = 120mA (Typ.)
2. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using “AC Test Conditions” of input levels of GND to 3V.
3. f = 0 means no address or control lines change.
4. Port “A” may be either left or right port. Port “B” is the opposite from port “A”.
5. Refer to Chip Enable Truth Table.
**AC Test Conditions**

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>3ns Max.</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>Figures 1 and 2</td>
</tr>
<tr>
<td>Output Load</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Timing depends on which signal is asserted last, OE, CE, LB or UB.
2. Timing depends on which signal is de-asserted first CE, OE, LB or UB.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tACE, tACE, tAA or tBDD.
5. SEM = Vin.
6. Refer to Chip Enable Truth Table.

**Waveform of Read Cycles**

**Timing of Power-Up Power-Down**
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>7028L15</th>
<th>7028L20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Com’t Only</td>
<td>Com’t &amp; Ind</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>READ CYCLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>tACE</td>
<td>Chip Enable Access Time</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>tAOE</td>
<td>Output Enable Access Time</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tLZ</td>
<td>Output Low-Z Time</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>tPU</td>
<td>Chip Enable to Power Up Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tPD</td>
<td>Chip Disable to Power Down Time</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>tSOP</td>
<td>Semaphore Flag Update Pulse (CE or SEM)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>tSAA</td>
<td>Semaphore Address Access Time</td>
<td></td>
<td>15</td>
</tr>
</tbody>
</table>

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>7028L15</th>
<th>7028L20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Com’t Only</td>
<td>Com’t &amp; Ind</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>Max.</td>
</tr>
<tr>
<td><strong>WRITE CYCLE</strong></td>
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<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>tEW</td>
<td>Chip Enable to End-of-Write</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tAV</td>
<td>Address Valid to End-of-Write</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid to End-of-Write</td>
<td>10</td>
<td>15</td>
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<tr>
<td>tHZ</td>
<td>Output High-Z Time</td>
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<td>tDH</td>
<td>Data Hold Time</td>
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<td>tE2</td>
<td>Write Enable to Output in High-Z</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>tOW</td>
<td>Output Active from End-of-Write</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tSWRD</td>
<td>SEM Flag Write to Read Time</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>tSPS</td>
<td>SEM Flag Contention Window</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, CE = VIL and SEM = VIL. To access semaphore, CE = VIH and SEM = VIL. Either condition must be valid for the entire tSW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
Timing Waveform of Write Cycle No. 1, R/W Controlled Timing\(^{(1,5,8)}\)

<table>
<thead>
<tr>
<th>Timing Waveform of Write Cycle No. 2, CE Controlled Timing(^{(1,5)})</th>
</tr>
</thead>
</table>

### Timing Waveform of Write Cycle No. 1, R/W Controlled Timing\(^{(1,5,8)}\)

**NOTES:**
1. R/W or CE or UB and LB = V\(_{IH}\) during all address transitions.
2. A write occurs during the overlap (t\(_{EW}\) or t\(_{WP}\)) of a CE = V\(_{IL}\) and a R/W = V\(_{IL}\) for memory array writing cycle.
3. twz is measured from the earlier of CE or R/W (or SEM or R/W) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE or SEM = V\(_{IL}\) transition occurs simultaneously with or after the R/W = V\(_{IL}\) transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, CE or R/W.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If OE = V\(_{IH}\) during R/W controlled write cycle, the write pulse width must be the larger of t\(_{WP}\) or (t\(_{WZ}\) + t\(_{OW}\)) to allow the I/O drivers to turn off and data to be placed on the bus for the required t\(_{OW}\). If OE = V\(_{IL}\) during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t\(_{WP}\).
9. To access RAM, CE = V\(_{IH}\) and SEM = V\(_{IH}\). To access semaphore, CE = V\(_{IL}\) and SEM = V\(_{IL}\). t\(_{EW}\) must be met for either condition.
10. Refer to Chip Enable Truth Table.
**Timing Waveform of Semaphore Read after Write Timing, Either Side**

1. \( \overline{CE} = \overline{UB} \) and \( \overline{LB} = V_{IH} \) for the duration of the above timing (both write and read cycle) (Refer to Chip Enable Truth Table).
2. “DATAOUT VALID” represents all I/O's (I/O0 - I/O15) equal to the semaphore value.

**Timing Waveform of Semaphore Write Contention**

1. \( D_{OR} = D_{OL} = V_{IL} \), \( \overline{CE}_{L} = \overline{CE}_{R} = V_{IH} \) or both \( \overline{UB} \) and \( \overline{LB} = V_{IH} \) (Refer to Chip Enable Truth Table).
2. All timing is the same for left and right ports. Port “A” may be either left or right port. “B” is the opposite from port “A”.
3. This parameter is measured from \( R/W^* \) or \( SEM^* \) going HIGH to \( R/W^* \) or \( SEM^* \) going HIGH.
4. If \( t_{SPS} \) is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>7028L15 Com’l Only</th>
<th>7028L20 Com’l &amp; Ind</th>
<th>Unit</th>
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<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>BUSY TIMING (M=P=Vih)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tBAA</td>
<td>BUSY Access Time from Address Match</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tBDA</td>
<td>BUSY Disable Time from Address Not Matched</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tBAC</td>
<td>BUSY Access Time from Chip Enable Low</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tBDC</td>
<td>BUSY Access Time from Chip Enable High</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tAPS</td>
<td>Arbitration Priority Set-up Time (2)</td>
<td>5</td>
<td>—</td>
<td>5</td>
</tr>
<tr>
<td>tBDD</td>
<td>BUSY Disable to Valid Data (3)</td>
<td>—</td>
<td>15</td>
<td>—</td>
</tr>
<tr>
<td>tWH</td>
<td>Write Hold After BUSY (5)</td>
<td>12</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>BUSY TIMING (M=P=Vil)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tB</td>
<td>BUSY Input to Write (6)</td>
<td>0</td>
<td>—</td>
<td>0</td>
</tr>
<tr>
<td>tWH</td>
<td>Write Hold After BUSY (5)</td>
<td>12</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>PORT-TO-PORT DELAY TIMING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tXDD</td>
<td>Write Pulse to Data Delay (3)</td>
<td>—</td>
<td>30</td>
<td>—</td>
</tr>
<tr>
<td>tXCD</td>
<td>Write Data Valid to Read Data Delay (3)</td>
<td>—</td>
<td>25</td>
<td>—</td>
</tr>
</tbody>
</table>

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read and BUSY (M=P=Vih)”.
2. To ensure that the earlier of the two ports wins.
3. taco is a calculated parameter and is the greater of 0, tXDD – tWP (actual) or tXDD – tWP (actual).
4. To ensure that the write cycle is inhibited on port “B” during contention on port “A”.
5. To ensure that a write cycle is completed on port “B” after contention on port “A”.
Timing Waveform of Write with Port-to-Port Read and \( \text{BUSY} \ (M/\overline{S} = V_{IH})^{(2,4,5)} \)

Timing Waveform of Write with \( \overline{\text{BUSY}} \ (M/\overline{S} = V_{IL}) \)

NOTES:
1. To ensure that the earlier of the two ports wins, \( \text{tAPS} \) is ignored for \( M/\overline{S} = V_{IL} \) (SLAVE).
2. \( \overline{CE} = \overline{CE_r} = V_{IL} \), refer to Chip Enable Truth Table.
3. \( \overline{OE} = V_{IL} \) for the reading port.
4. If \( M/\overline{S} = V_{IL} \) (SLAVE), \( \text{BUSY} \) is an input. Then for this example \( \overline{\text{BUSY}} \cdot X' = V_{IH} \) and \( \overline{\text{BUSY}} \cdot \overline{B'} \) input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

NOTES:
1. \( \text{tWH} \) must be met for both \( \overline{\text{BUSY}} \) input (SLAVE) and output (MASTER).
2. \( \text{BUSY} \) is asserted on port "B" blocking \( \overline{R/W} \cdot B' \), until \( \text{BUSY} \cdot B' \) goes HIGH.
3. \( \text{tWH} \) is only for the "Slave" version.
Waveform of BUSY Arbitration Controlled by CE Timing \((M/S = V_{IH})^{(1,3)}\)

ADDRA and "B"

CE"A"

tAPS\(^{(2)}\)

CE"B"

BUSY"B"

ADDRESSES MATCH

Waveform of BUSY Arbitration Cycle Controlled by Address Match Timing \((M/S = V_{IH})^{(1)}\)

ADDR"A"

ADDRESS "N"

tAPS\(^{(2)}\)

ADDR"B"

MATCHING ADDRESS "N"

BUSY"B"

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.
3. Refer to Chip Enable Truth Table.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>7028L15</th>
<th>7028L20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>tINS</td>
<td>Interrupt Set Time</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>tINR</td>
<td>Interrupt Reset Time</td>
<td></td>
<td>15</td>
</tr>
</tbody>
</table>
**Waveform of Interrupt Timing**

1. All timing is the same for left and right ports. Port ‘A’ may be either the left or right port. Port ‘B’ is the port opposite from port ‘A’.
2. See Interrupt Truth Table.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.
5. Refer to Chip Enable Truth Table.

**Truth Table IV — Interrupt Flag**

1. Assumes BUSYL = BUSYR = VIL.
2. If BUSYL = VIH, then no change.
3. If BUSYR = VIH, then no change.
4. INTL and INTTr must be initialized at power-up.
5. Refer to Chip Enable Truth Table.
**Truth Table V — Address BUSY Arbitration**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE&lt;sub&gt;L&lt;/sub&gt;</td>
<td>CE&lt;sub&gt;R&lt;/sub&gt;</td>
<td>A&lt;sub&gt;0&lt;/sub&gt;-A&lt;sub&gt;15&lt;/sub&gt;&lt;sub&gt;L&lt;/sub&gt;</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>NO MATCH</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>MATCH</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>MATCH</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>MATCH</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Pins BUSY<sub>L</sub> and BUSY<sub>R</sub> are both outputs when the part is configured as a master. Both are inputs when configured as a slave. BUSY outputs on the IDT7028 are push-pull, not open drain outputs. On slaves the BUSY input internally inhibits writes.
2. “L” if the inputs to the opposite port were stable prior to the address and enable inputs of this port. “H” if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either BUSYL or BUSYR = LOW will result. BUSYL and BUSYR outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.
4. Refer to Chip Enable Truth Table.

**Truth Table VI — Example of Semaphore Procurement Sequence**

<table>
<thead>
<tr>
<th>Functions</th>
<th>D&lt;sub&gt;o&lt;/sub&gt; - D&lt;sub&gt;15&lt;/sub&gt; Left</th>
<th>D&lt;sub&gt;o&lt;/sub&gt; - D&lt;sub&gt;15&lt;/sub&gt; Right</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Action</td>
<td>1</td>
<td>1</td>
<td>Semaphore free</td>
</tr>
<tr>
<td>Left Port Writes “0” to Semaphore</td>
<td>0</td>
<td>1</td>
<td>Left port has semaphore token</td>
</tr>
<tr>
<td>Right Port Writes “0” to Semaphore</td>
<td>0</td>
<td>1</td>
<td>No change. Right side has no write access to semaphore</td>
</tr>
<tr>
<td>Left Port Writes “1” to Semaphore</td>
<td>1</td>
<td>0</td>
<td>Right port obtains semaphore token</td>
</tr>
<tr>
<td>Left Port Writes “0” to Semaphore</td>
<td>1</td>
<td>0</td>
<td>No change. Left port has no write access to semaphore</td>
</tr>
<tr>
<td>Right Port Writes “1” to Semaphore</td>
<td>0</td>
<td>1</td>
<td>Left port obtains semaphore token</td>
</tr>
<tr>
<td>Left Port Writes “1” to Semaphore</td>
<td>1</td>
<td>1</td>
<td>Semaphore free</td>
</tr>
<tr>
<td>Right Port Writes “0” to Semaphore</td>
<td>1</td>
<td>0</td>
<td>Right port has semaphore token</td>
</tr>
<tr>
<td>Right Port Writes “1” to Semaphore</td>
<td>1</td>
<td>1</td>
<td>Semaphore free</td>
</tr>
<tr>
<td>Left Port Writes “0” to Semaphore</td>
<td>1</td>
<td>1</td>
<td>Left port has semaphore token</td>
</tr>
<tr>
<td>Left Port Writes “1” to Semaphore</td>
<td>1</td>
<td>1</td>
<td>Semaphore free</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7028.
2. There are eight semaphore flags written to via I/O<sub>0</sub> and read from all I/O<sub>s</sub> (I/O<sub>0</sub>-I/O<sub>15</sub>). These eight semaphores are addressed by A<sub>0</sub>-A<sub>7</sub>.
3. CE = V<sub>IL</sub>, SEM = V<sub>IL</sub> to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

**Functional Description**

The IDT7028 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7028 has an automatic power down feature controlled by CE. The CE<sub>L</sub> and CE<sub>R</sub> control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (CE = V<sub>IL</sub>). When a port is enabled, access to the entire memory array is permitted.

**Interrupts**

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (INT<sub>L</sub>) is asserted when the right port writes to memory location FFFE (HEX), where a write is defined as CE<sub>R</sub> = R/W = V<sub>L</sub> per Truth Table IV. The left port clears the interrupt through access of address location FFFF when CE<sub>L</sub> = V<sub>IL</sub>, R/W is a “don’t care”. Likewise, the right port interrupt flag (INT<sub>R</sub>) is asserted when the left port writes to memory location FFFF (HEX) and to clear the interrupt flag (INT<sub>R</sub>), the right port must read the memory location FFFF. The message (16 bits) at FFFE or FFFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations FFFE and FFFF are not used as mailboxes, but as part of the random access memory. Refer to Table IV for the interrupt operation.
Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “busy”. The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT7028 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

Semaphores

The IDT7028 is an extremely fast Dual-Port 64K x16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer’s software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by CE, the Dual-Port RAM enable, and SEM, the semaphore enable. The CE and SEM pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table II where CE and SEM are both HIGH.

Systems which can best use the IDT7028 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7028’s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7028 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called “Token Passing Allocation.” In this method, the state of semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore’s status or remove its request for that semaphore to perform...
Each of the flags has a unique address which can be accessed by either signal (because either signal can be used instead, system contention problems could have occurred during the gap between the read and write cycles. It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side’s semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side’s request latch. The second side’s flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch. The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.
Ordering Information

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
<th>Process/Temperature Range</th>
<th>Notes</th>
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<td>999</td>
<td>A</td>
<td>A</td>
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<td>8</td>
<td>Tube or Tray</td>
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<td>Tape &amp; Reel</td>
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<td></td>
<td>[1]</td>
<td>Commercial (0°C to +70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Industrial (-40°C to +85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PF</td>
<td>100-pin TQFP (PN100)</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td>Speed in nanoseconds</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>L</td>
<td></td>
<td></td>
<td></td>
<td>Low Power</td>
</tr>
<tr>
<td></td>
<td>7028</td>
<td>1024K (64K x 16) Dual-Port RAM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

- 9/30/99: Initial Public Release
- 11/10/99: Replaced IDT logo
- 1/12/01: Page 3: Increased storage temperature parameter
- Clarified TA parameter
- Page 5: DC Electrical parameters—changed wording from "open" to "disabled"
- Page 14: Added IV to Truth Table in "Interrupts" paragraph
- Changed ±200mV to 0mV in notes
- Removed Preliminary status
- 11/19/01: Page 2: Added date revision for pin configuration
- Pages 3, 5, 7, 10 & 12: Removed Industrial temp footnote from all tables
- Pages 5, 7, 10 & 12: Added Industrial temp for 20ns speed to DC and AC Electrical Characteristics
- Page 17: Added Industrial temp offering to 20ns ordering information
- Pages 1 & 17: Replaced TM logo with ® logo
IDT7028L
High-Speed 64K x 16 Dual-Port Static RAM
Industrial and Commercial Temperature Ranges

Datasheet Document History (con’t)

01/29/09: Page 17 Removed “IDT” from orderable part number
07/23/15: Page 1 Added green availability to Features
Page 2 Removed IDT in reference to fabrication
Page 2 Removed date from the 100-pin TQFP configuration
Page 2 & 17 The package code PN100-1 changed to PN100 to match standard package codes
Page 3 Removed Military Information from the Absolute Maximum Ratings table and from the Maximum Operating Temperature and Supply Voltage table
Page 15 Removed overbar from CE1 in figure 3
Page 17 Added Green and Tape & Reel indicators to the Ordering Information and updated footnotes

06/27/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018