Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 7.5ns (max.)
  - Industrial: 12ns (max.)
- Low-power operation
  - IDT70V9089/79L
    - Active: 429mW (typ.)
    - Standby: 1.32mW (typ.)
- Flow-Through or Pipelined output mode on either port via the FT/PIPE pin
- Dual chip enables allow for depth expansion without additional logic

- Counter enable and reset features
- Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 7.5ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 12ns cycle time, 83MHz operation in the Pipelined output mode
- LVTTL-compatible, single 3.3V (±0.3V) power supply
- Available in a 100 pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram

NOTE:
1. A15x is a NC for IDT70V9079.
**Description:**

The IDT70V9089/79 is a high-speed 64/32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9089/79 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 429mW of power.

**Pin Configurations**

![Diagram of Pin Configurations](image)

**NOTES:**

1. A ‘x’ is a NC for IDT70V9079.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
### Pin Names

<table>
<thead>
<tr>
<th>Left Port</th>
<th>Right Port</th>
<th>Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE0L, CE1L</td>
<td>CE0R, CE1R</td>
<td>Chip Enables</td>
</tr>
<tr>
<td>R/WL</td>
<td>R/WR</td>
<td>Read/Write Enable</td>
</tr>
<tr>
<td>OEL</td>
<td>OER</td>
<td>Output Enable</td>
</tr>
<tr>
<td>A0L - A15L</td>
<td>A0R - A15R</td>
<td>Address</td>
</tr>
<tr>
<td>V0L - V0L</td>
<td>V0R - IO7R</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>CLKL</td>
<td>CLKR</td>
<td>Clock</td>
</tr>
<tr>
<td>ADSL</td>
<td>ADSR</td>
<td>Address Strobe</td>
</tr>
<tr>
<td>CNTENL</td>
<td>CNTENR</td>
<td>Counter Enable</td>
</tr>
<tr>
<td>CNTRSTL</td>
<td>CNTRSTR</td>
<td>Counter Reset</td>
</tr>
<tr>
<td>FT/PIPEL</td>
<td>FT/PIPER</td>
<td>Flow Through/Pipeline</td>
</tr>
</tbody>
</table>

### Truth Table I—Read/Write and Enable Control\(^{(1,2,3)}\)

<table>
<thead>
<tr>
<th>OE</th>
<th>CLK</th>
<th>CE0</th>
<th>CE1</th>
<th>R/W</th>
<th>I/O0⁻¹</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>↑</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td></td>
<td>High-Z - Deselected - Power Down</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td></td>
<td>High-Z - Deselected - Power Down</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>DATA(^n)</td>
<td>Write</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>DATA(^n)</td>
<td>Read</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>High-Z</td>
<td>Outputs Disabled</td>
</tr>
</tbody>
</table>

### Truth Table II—Address Counter Control\(^{(1,2,3)}\)

<table>
<thead>
<tr>
<th>External Address</th>
<th>Previous Internal Address</th>
<th>Internal Address Used</th>
<th>CLK</th>
<th>ADS</th>
<th>CNTEN</th>
<th>CNTRST</th>
<th>I/O(^{(3)})</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>An</td>
<td>X</td>
<td>An</td>
<td>↑</td>
<td>L(^{(4)})</td>
<td>X</td>
<td>H</td>
<td>D(^\circ)(^{(n)})</td>
<td>External Address Used</td>
</tr>
<tr>
<td>X</td>
<td>An</td>
<td>An + 1</td>
<td>↑</td>
<td>H</td>
<td>L(^{(5)})</td>
<td>H</td>
<td>D(^\circ)(n+1)</td>
<td>Counter Enabled—Internal Address generation</td>
</tr>
<tr>
<td>X</td>
<td>An + 1</td>
<td>An + 1</td>
<td>↑</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>D(^\circ)(n+1)</td>
<td>External Address Blocked—Counter disabled (An + 1 reused)</td>
</tr>
<tr>
<td>X</td>
<td>A0</td>
<td>↑</td>
<td>X</td>
<td>X</td>
<td>L(^{(4)})</td>
<td>D(^\circ)(0)</td>
<td>Counter Reset to Address 0</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:
1. "H" = V\(^{IH}\), "L" = V\(^{IL}\), "X" = Don't Care.
2. ADS, CNTEN, CNTRST = X.
3. OE is an asynchronous input signal.
**Recommended Operating Temperature and Supply Voltage**

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature</th>
<th>GND</th>
<th>$V_{DD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>0V</td>
<td>3.3V $\pm$ 0.3V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>0V</td>
<td>3.3V $\pm$ 0.3V</td>
</tr>
</tbody>
</table>

NOTES:
1. This is the parameter $Ta$. This is the "instant on" case temperature.

**Recommended DC Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>2.2</td>
<td>—</td>
<td>$V_{DD} + 0.3V$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>-0.3$^2$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTES:
1. $V_{TERM}$ must not exceed $V_{DD} + 0.3V$.
2. $V_{IL} \geq -1.5V$ for pulse width less than 10ns.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Commercial &amp; Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TERM}$ $^2$</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td>$T_{BIAS}$</td>
<td>Temperature Under Bias</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{JN}$</td>
<td>Junction Temperature</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>DC Output Current</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed $V_{DD} + 0.3V$ for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20mA$ for the period of $V_{TERM} \geq V_{DD} + 0.3V$.

**Capacitance** ($TA = +25°C, f = 1.0MHz$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter $^{(1)}$</th>
<th>Conditions $^{(2)}$</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>$V_{IN} = 3dV$</td>
<td>9</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{OUT}$ $^{(3)}$</td>
<td>Output Capacitance</td>
<td>$V_{OUT} = 3dV$</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. $3dV$ references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. $C_{OUT}$ also references $C_{IN}$.
**DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range**

(VDD = 3.3V ± 0.3V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>70V9089/79S</th>
<th>70V9089/79L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Leakage Current</td>
<td>VDD = 3.3V, VIN = 0V to VDD</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Leakage Current</td>
<td>CE0 = VH or CE1 = VL, VOUT = 0V to VDD</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Low Voltage</td>
<td>IO = +4mA</td>
<td>—</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output High Voltage</td>
<td>IO = -4mA</td>
<td>2.4</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTE:**
1. At VDD ≤ 2.0V input leakages are undefined.

**DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range**

(VDD = 3.3V ± 0.3V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Version</th>
<th>70V9089/79X6</th>
<th>70V9089/79X7</th>
<th>70V9089/79X9</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dynamic Operating Current (Both Ports Active)</td>
<td>CE0 and CE1 = VL</td>
<td>COM' L S</td>
<td>220</td>
<td>395</td>
<td>180</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Outputs Disabled</td>
<td></td>
<td>L</td>
<td>220</td>
<td>350</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Standby Current (Both Ports - TTL Level Inputs)</td>
<td>CE0 and CE1 = VH</td>
<td>COM' L S</td>
<td>70</td>
<td>145</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = fMAX(1)</td>
<td>L</td>
<td>70</td>
<td>130</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Standby Current (One Port - TTL Level Inputs)</td>
<td>CE0 = VL and CE1 = VIH</td>
<td>COM' L S</td>
<td>150</td>
<td>280</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = fMAX(1)</td>
<td></td>
<td>L</td>
<td>150</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Full Standby Current (Both Ports - CMOS Level Inputs)</td>
<td>Both Ports CE0 and CE1</td>
<td>COM' L S</td>
<td>1.0</td>
<td>5</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Outputs Disabled, f = fMAX(1)</td>
<td></td>
<td>L</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Full Standby Current (One Port - CMOS Level Inputs)</td>
<td>CE0 = 0.2V and CE1 = 0.2V</td>
<td>COM' L S</td>
<td>140</td>
<td>270</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = fMAX(1)</td>
<td></td>
<td>L</td>
<td>140</td>
<td>240</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tCYC, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. VDD = 3.3V, TA = 25°C for Typ, and are not production tested. ICC (f=0) = 90mA (Typ).
5. CE0 = VL means CE0X = VL and CE1X = VH
CE0 = VH means CE0X = VH or CE1X = VL
CE0 ≤ 0.2V means CE0X < 0.2V and CE1X = VH
CE0 ≥ VDD - 0.2V means CE0X ≥ VDD - 0.2V or CE1X ≤ 0.2V
"X" represents "L" for left port or "R" for right port.
6. 'X' in part number indicates power rating (S or L).
### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VDD = 3.3V ± 0.3V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Version</th>
<th>70V9089/79X12 (Com’l &amp; Ind)</th>
<th>70V9089/79X15 (Com’l Only)</th>
<th>Typ. (1)</th>
<th>Max.</th>
<th>Typ. (2)</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Dynamic Operating Current</td>
<td>CE and CER = VIL Outputs Disabled, f = fMAX(1)</td>
<td>COM’L S</td>
<td>150</td>
<td>240</td>
<td>130</td>
<td>220</td>
<td>130</td>
<td>220</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>150</td>
<td>215</td>
<td>130</td>
<td>185</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>150</td>
<td>215</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>150</td>
<td>215</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB1</td>
<td>Standby Current</td>
<td>CE and CER = VIL f = fMAX(1)</td>
<td>COM’L S</td>
<td>40</td>
<td>65</td>
<td>30</td>
<td>55</td>
<td>30</td>
<td>55</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>40</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>40</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>40</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB2</td>
<td>Standby Current</td>
<td>CE&lt; VIL and CEB = VIL f = fMAX(1)</td>
<td>COM’L S</td>
<td>100</td>
<td>160</td>
<td>90</td>
<td>150</td>
<td>90</td>
<td>130</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>100</td>
<td>140</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>100</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>100</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB3</td>
<td>Full Standby Current</td>
<td>Both Ports CE and CER ≥ VDD - 0.2V or VIL ≤ 0.2V, Active Port Outputs Disabled, f = fMAX(1)</td>
<td>COM’L S</td>
<td>1.0</td>
<td>5</td>
<td>1.0</td>
<td>5</td>
<td>1.0</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>0.4</td>
<td>3</td>
<td>0.4</td>
<td>3</td>
<td>0.4</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>0.4</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>0.4</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB4</td>
<td>Full Standby Current</td>
<td>CE&lt; 0.2V and CEB &gt; VDD - 0.2V or VIL ≤ 0.2V, Active Port Outputs Disabled, f = fMAX(1)</td>
<td>COM’L S</td>
<td>90</td>
<td>150</td>
<td>80</td>
<td>140</td>
<td>80</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>90</td>
<td>130</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND S</td>
<td>90</td>
<td>140</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:
1. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tCYC, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. VDD = 3.3V, TA = 25°C for Typ, and are not production tested. ICC(=0) = 90mA (Typ).
5. CE< VIL means CE< VIL = VIL and CE< 0.2V = VIL
CE< VIL means CE< VIL = VIL or CE< 0.2V = VIL
CE< 0.2V means CE< 0.2V = VIL and CE< 0.2V = VIL
CE> VDD - 0.2V means CE> VDD - 0.2V or CE> 0.2V
CE> 0.2V means CE> 0.2V = VIL or CE> 0.2V = VIL

   "X" represents "L" for left port or "R" for right port.
6. 'X' in part number indicates power rating (S or L).
AC Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>3ns Max.</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>Figures 1, 2 and 3</td>
</tr>
</tbody>
</table>

Figure 1. AC Output Test load.

Figure 2. Output Test Load
(For tCKLZ, tCKHZ, toLz, and toHZ).
*Including scope and jig.

![AC Test Conditions Diagram](image)

Figure 3. Typical Output Derating (Lumped Capacitive Load).

10 pF is the I/O capacitance of this device, and 30pF is the AC Test Load Capacitance.

$\Delta tCD_1$, $\Delta tCD_2$
(Typical, ns)

Capacitance (pF)
### AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)\(^{(3,4)}\) \((V_{DD} = 3.3 \text{V} \pm 0.3, T_A = 0°C \text{ to } +70°C)\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V9089/79X6 Com'il Only</th>
<th>70V9089/79X7 Com'il Only</th>
<th>70V9089/79X9 Com'il Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCYC1</td>
<td>Clock Cycle Time (Flow-Through)(^{(2)})</td>
<td>19</td>
<td>22</td>
<td>25</td>
</tr>
<tr>
<td>tCYC2</td>
<td>Clock Cycle Time (Pipelined)(^{(2)})</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tCH1</td>
<td>Clock High Time (Flow-Through)(^{(2)})</td>
<td>6.5</td>
<td>7.5</td>
<td>12</td>
</tr>
<tr>
<td>tCL1</td>
<td>Clock Low Time (Flow-Through)(^{(2)})</td>
<td>6.5</td>
<td>7.5</td>
<td>12</td>
</tr>
<tr>
<td>tCH2</td>
<td>Clock High Time (Pipelined)(^{(2)})</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>tCL2</td>
<td>Clock Low Time (Pipelined)(^{(2)})</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>tr</td>
<td>Clock Rise Time</td>
<td>—</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tf</td>
<td>Clock Fall Time</td>
<td>—</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tSA</td>
<td>Address Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHA</td>
<td>Address Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tSC</td>
<td>Chip Enable Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHC</td>
<td>Chip Enable Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tSW</td>
<td>R/W Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tWH</td>
<td>R/W Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tID</td>
<td>Input Data Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHD</td>
<td>Input Data Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tAD</td>
<td>ADS Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHD</td>
<td>ADS Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tCN</td>
<td>CNTEN Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHC</td>
<td>CNTEN Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tSRST</td>
<td>CNTRST Setup Time</td>
<td>3.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>tHRST</td>
<td>CNTRST Hold Time</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable to Data Valid</td>
<td>—</td>
<td>6.5</td>
<td>7.5</td>
</tr>
<tr>
<td>tOLZ</td>
<td>Output Enable to Output Low-Z(^{(1)})</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>tOHZ</td>
<td>Output Enable to Output High-Z(^{(1)})</td>
<td>1</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>tCDV</td>
<td>Clock to Data Valid (Flow-Through)(^{(2)})</td>
<td>—</td>
<td>15</td>
<td>18</td>
</tr>
<tr>
<td>tCD2</td>
<td>Clock to Data Valid (Pipelined)(^{(2)})</td>
<td>—</td>
<td>6.5</td>
<td>7.5</td>
</tr>
<tr>
<td>tDC</td>
<td>Data Output Hold After Clock High</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>tCH2</td>
<td>Clock High to Output High-Z(^{(1)})</td>
<td>2</td>
<td>9</td>
<td>2</td>
</tr>
<tr>
<td>tCL2</td>
<td>Clock High to Output Low-Z(^{(1)})</td>
<td>2</td>
<td>9</td>
<td>2</td>
</tr>
</tbody>
</table>

### Port-to-Port Delay

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V9089/79X6 Com'il Only</th>
<th>70V9089/79X7 Com'il Only</th>
<th>70V9089/79X9 Com'il Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCWDD</td>
<td>Write Port Clock High to Read Data Delay</td>
<td>—</td>
<td>24</td>
<td>28</td>
</tr>
<tr>
<td>tCCS</td>
<td>Clock-to-Clock Setup Time</td>
<td>—</td>
<td>9</td>
<td>10</td>
</tr>
</tbody>
</table>

\(\text{NOTES:}\)

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The Pipelined output parameters (tCYC2, tCL2) apply to either or both left and right ports when FT/PIPE = VIH. Flow-through parameters (tCYC1, tCDV) apply when FT/PIPE = VIH for that port.
4. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (OE) and FT/PIPE. FT/PIPE should be treated as a DC signal, i.e. steady state during operation.
5. ‘X’ in part number indicates power rating (S or L).
AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) \(^{(3,4)}\) (V\text{DD} = 3.3V \pm 0.3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V9089/79X12 Com\text{I} &amp; Ind</th>
<th>70V908979X15 Com\text{I} Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{CYC}1</td>
<td>Clock Cycle Time (Flow-Through) (^{(2)})</td>
<td>30</td>
<td>35</td>
</tr>
<tr>
<td>t\text{CYC}2</td>
<td>Clock Cycle Time (Pipelined) (^{(2)})</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>t\text{CH1}</td>
<td>Clock High Time (Flow-Through) (^{(2)})</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>t\text{CL1}</td>
<td>Clock Low Time (Flow-Through) (^{(2)})</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>t\text{CH2}</td>
<td>Clock High Time (Pipelined) (^{(2)})</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>t\text{CL2}</td>
<td>Clock Low Time (Pipelined) (^{(2)})</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>t\text{R}</td>
<td>Clock Rise Time</td>
<td>—</td>
<td>3</td>
</tr>
<tr>
<td>t\text{F}</td>
<td>Clock Fall Time</td>
<td>—</td>
<td>3</td>
</tr>
<tr>
<td>t\text{SA}</td>
<td>Address Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HA}</td>
<td>Address Hold Time</td>
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<td>1</td>
</tr>
<tr>
<td>t\text{SC}</td>
<td>Chip Enable Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HC}</td>
<td>Chip Enable Hold Time</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t\text{SW}</td>
<td>R\text{/W} Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HW}</td>
<td>R\text{/W} Hold Time</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t\text{SD}</td>
<td>Input Data Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HD}</td>
<td>Input Data Hold Time</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t\text{SD}</td>
<td>ADS Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HD}</td>
<td>ADS Hold Time</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t\text{SCN}</td>
<td>CNTEN Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HCN}</td>
<td>CNTEN Hold Time</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>t\text{SRST}</td>
<td>CNTRST Setup Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>t\text{HRST}</td>
<td>CNTRST Hold Time</td>
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<td>1</td>
</tr>
<tr>
<td>t\text{OE}</td>
<td>Output Enable to Data Valid</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>t\text{ELZ}</td>
<td>Output Enable to Output Low-Z (^{(1)})</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>t\text{EHZ}</td>
<td>Output Enable to Output High-Z (^{(1)})</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>t\text{CD1}</td>
<td>Clock to Data Valid (Flow-Through) (^{(2)})</td>
<td>—</td>
<td>25</td>
</tr>
<tr>
<td>t\text{CD2}</td>
<td>Clock to Data Valid (Pipelined) (^{(2)})</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>t\text{DC}</td>
<td>Data Output Hold After Clock High</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>t\text{CKHZ}</td>
<td>Clock High to Output High-Z (^{(1)})</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>t\text{CKLZ}</td>
<td>Clock High to Output Low-Z (^{(1)})</td>
<td>2</td>
<td>9</td>
</tr>
<tr>
<td>Port-to-Port Delay</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\text{CD0D}</td>
<td>Write Port Clock High to Read Data Delay</td>
<td>—</td>
<td>40</td>
</tr>
<tr>
<td>t\text{CCS}</td>
<td>Clock-to-Clock Setup Time</td>
<td>—</td>
<td>15</td>
</tr>
</tbody>
</table>

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
   This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t\text{CYC}2, t\text{CD0}) apply to either or both left and right ports when \text{FT/PIPE} = \text{VH}. Flow-through parameters (t\text{CYC}1, t\text{CD1}) apply when \text{FT/PIPE} = \text{VL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\text{OE}) and \text{FT/PIPE}, \text{FT/PIPE} should be treated as a DC signal, i.e. steady state during operation.
4. ‘X’ in part number indicates power rating (S or L).
Timing Waveform of Read Cycle for Flow-Through Output (\(\text{FT/PIPE}^{x} = \text{V}_{\text{IL}}\))(3,6)

Timing Waveform of Read Cycle for Pipelined Output (\(\text{FT/PIPE}^{x} = \text{V}_{\text{IH}}\))(3,6)

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. \(\overline{OE}\) is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. \(\text{ADS} = \text{V}_{\text{IL}}\) and \(\text{CNTRST} = \text{V}_{\text{IH}}\).
4. The output is disabled (High-impedance state) by \(\overline{CE0} = \text{V}_{\text{IH}}\) or \(\overline{CE1} = \text{V}_{\text{IL}}\) following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since \(\text{ADS} = \text{V}_{\text{IL}}\) constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "x" denotes Left or Right port. The diagram is with respect to that port.
Timing Waveform of a Bank Select Pipelined Read\(^{(1,2)}\)

\[
\begin{align*}
&\text{CLK} & & t_{SC} & & t_{HC} \\
&\text{ADDRESS}(B1) & & A_0 & & A_1 & & A_2 & & A_3 & & A_4 & & A_5 & & A_6 \\
&\text{CE}_0(B1) & & t_{SA} & & t_{HA} & & t_{SC} & & t_{HC} & & t_{SC} & & t_{HC} \\
&\text{DATAOUT}(B1) & & Q_0 & & Q_1 & & Q_2 & & Q_3 & & Q_4 \\
&\text{ADDRESS}(B2) & & A_0 & & A_1 & & A_2 & & A_3 & & A_4 & & A_5 & & A_6 \\
&\text{CE}_0(B2) & & t_{SA} & & t_{HA} & & t_{SC} & & t_{HC} & & t_{SC} & & t_{HC} \\
&\text{DATAOUT}(B2) & & D_0 & & D_1 & & D_2 & & D_3 & & D_4 & & D_5 \\
\end{align*}
\]

Timing Waveform of a Bank Select Flow-Through Read\(^{(6)}\)

\[
\begin{align*}
&\text{CLK} & & t_{SC} & & t_{HC} \\
&\text{ADDRESS}(B1) & & A_0 & & A_1 & & A_2 & & A_3 & & A_4 & & A_5 & & A_6 \\
&\text{CE}_0(B1) & & t_{SA} & & t_{HA} & & t_{SA} & & t_{HA} & & t_{SA} & & t_{HA} \\
&\text{DATAOUT}(B1) & & D_0 & & D_1 & & D_2 & & D_3 & & D_4 & & D_5 & & D_6 \\
&\text{ADDRESS}(B2) & & A_0 & & A_1 & & A_2 & & A_3 & & A_4 & & A_5 & & A_6 \\
&\text{CE}_0(B2) & & t_{SA} & & t_{HA} & & t_{SA} & & t_{HA} & & t_{SA} & & t_{HA} \\
&\text{DATAOUT}(B2) & & D_0 & & D_1 & & D_2 & & D_3 & & D_4 & & D_5 & & D_6 \\
\end{align*}
\]

**NOTES:**

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9089/79 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. OE and ADS = VIL; CE\(_1(B1)\), CE\(_1(B2)\), R/W and CNTRST = VIH.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. CE\(_0\) and ADS = VIL; CE\(_1\) and CNTRST = VIH.
5. OE = VIL for the Right Port, which is being read from. OE = VIH for the Left Port, which is being written to.
6. If t\(_{CCS}\) ≤ maximum specified, then data from right port READ is not valid until the maximum specified for t\(_{CWDD}\).
   If t\(_{CCS}\) > maximum specified, then data from right port READ is not valid until t\(_{CCS}\) + t\(_{CD1}\). t\(_{CWDD}\) does not apply in this case.
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. CE0 and ADS = VIL; CEN and CNTRST = VIH.
3. OE = VIL for the Port "B", which is being read from. OE = VIH for the Port "A", which is being written to.
4. If \( t_{CCS} \leq \) maximum specified, then data from right port READ is not valid until the maximum specified for \( t_{CWDD} \).
   If \( t_{CCS} > \) maximum specified, then data from right port READ is not valid until \( t_{CCS} + t_{CD1} \). \( t_{CWDD} \) does not apply in this case.
5. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)(3)

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$ and ADS = $V_{IL}$; $\overline{CE}_1$ and $\overline{CNTRST} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since ADS = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.
Timing Waveform of Flow-Through Read-to-Write-to-Read (\(\overline{OE} = V_{IL}\))(3)

Timing Waveform of Flow-Through Read-to-Write-to-Read (\(\overline{OE}\) Controlled)(3)

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \(\overline{CE}_0\) and \(\overline{ADS} = V_{IL}\); \(CE_1\) and \(CNTRST = V_{IH}\).
4. Addresses do not have to be accessed sequentially since \(\overline{ADS} = V_{IL}\) constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. *NOP* is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.
Timing Waveform of Pipelined Read with Address Counter Advance\(^{(1)}\)

Timing Waveform of Flow-Through Counter Read with Address Counter Advance\(^{(1)}\)

NOTES:
1. \(\overline{CE}\) and \(\overline{OE} = \overline{V}_{IL}\); \(CE = V_{IH}\), and \(\overline{CNTRST} = V_{IH}\).
2. If there is no address change via \(\overline{ADS} = \overline{V}_{IL}\) (loading a new address) or \(\overline{CNTEN} = \overline{V}_{IL}\) (advancing the address), i.e. \(\overline{ADS} = V_{IH}\) and \(\overline{CNTEN} = V_{IH}\), then the data output remains constant for subsequent clocks.
Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)\(^{(1)}\)

Timing Waveform of Counter Reset (Pipelined Outputs)\(^{(2)}\)

NOTES:
1. \(\overline{CE} = \text{VIL} \) and \(R/W = \text{VIL} \); \(CE = \text{VIL} \) and \(CNTRST = \text{VIL} \).
2. \(CE = \text{VIL} \); \(CE = \text{VIL} \).
3. The "Internal Address" is equal to the "External Address" when \(ADS = \text{VIL} \) and equals the counter output when \(ADS = \text{VIL} \).
4. Addresses do not have to be accessed sequentially since \(ADS = \text{VIL} \) constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. ADDR0 will be accessed. Extra cycles are shown here simply for clarification.
7. \(CNTEN = \text{VIL} \) advances Internal Address from \('A_n' to 'A_{n+1}'\). The transition shown indicates the time required for the counter to advance. The \('A_{n+1}'\) address is written to during this cycle.
**Functional Description**

The IDT70V9089/79 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the counter registers for fast interleaved memory applications.

A HIGH on CE0 or a LOW on CE1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9089/79’s for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with CE0 LOW and CE1 HIGH to reactivate the outputs.

**Depth and Width Expansion**

The IDT70V9089/79 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9089/79 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.

![Figure 4. Depth and Width Expansion with IDT70V9089/79](image)

**NOTE:**

1. A16 is for IDT70V9089. A15 is for IDT70V9079.

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**IDT Clock Solution for IDT70V9089/79 Dual-Port**

<table>
<thead>
<tr>
<th>IDT Dual-Port Part Number</th>
<th>Dual-Port I/O Specifications</th>
<th>Clock Specifications</th>
<th>IDT PLL Clock Device</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Voltage I/O</td>
<td>Input Capacitance</td>
<td>Input Duty Cycle Requirement</td>
</tr>
<tr>
<td></td>
<td>Dual-Port I/O Specifications</td>
<td></td>
<td>Maximum Frequency</td>
</tr>
<tr>
<td></td>
<td>Voltage</td>
<td>I/O</td>
<td>Input Capacitance</td>
</tr>
<tr>
<td>70V9089/79</td>
<td>3.3</td>
<td>LVTTL</td>
<td>9pF</td>
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<tr>
<td></td>
<td>PLL</td>
<td>Non-PLL</td>
<td>Clock Device</td>
</tr>
</tbody>
</table>

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Ordering Information

Ordering Information for Flow-through Devices

Orderable Part Information

Datasheet Document History

01/18/99:
- Initiated datasheet document history
- Converted to new format
- Cosmetic and typographical corrections
- Added additional notes to pin configurations
- Added Depth and Width Expansion section.
Datasheet Document History (con't.)

06/11/99: Page 3 Deleted note 6 for Table II
11/12/99: Replaced IDT logo
03/31/00: Combined Pipelined 70V9089 family and Flow-through 70V908 family offerings into one data sheet
           Changed ±200mV in waveform notes to 0mV
           Added corresponding part chart with ordering information
01/10/01: Page 3 Changed information in Truth Table II
           Page 4 Increased storage temperature parameters
          Clarified Ta parameter
           Page 5 DC Electrical parameters--changed wording from "open" to "disabled"
           Remved Preliminary Status
01/15/04: Consolidated multiple devices into one datasheet
           Changed ±200mV in waveform notes to 0mV
           Added corresponding part chart with ordering information
           Page 2 Added date revision to pin configuration
           Page 4 Added Junction Temperature to Absolute Maximum Ratings Table
           Added Ambient Temperature footnote
           Page 5 Added l-temp numbers for 9ns speed to the DC Electrical Characteristics Table
           Added 6ns & 7ns speeds DC power numbers to the DC Electrical Characteristics Table
           Page 7 Added l-temp for 9ns speed to AC Electrical Characteristics Table
           Added 6ns & 7ns speeds AC timing numbers to the AC Electrical Characteristics Table
           Page 16 Added 6ns & 7ns speeds grade and 9ns I-temp to ordering information
           Added IDT Clock Solution Table
           Pages 1 & 17 Replaced ® IDT logo with ™ new logo
05/11/04: Pages 1 & 19 Added 7ns speed grade to ordering information
           Page 5 Added 7ns speed DC power numbers to the DC Electrical Characteristics Table
           Page 8 Added 7ns speed AC timing numbers to the AC Electrical Characteristics Table
12/01/05: Page 1 Added green parts availability to features
           Page 18 Added green indicator to ordering information
01/19/09: Page 18 Removed "IDT" from orderable part number
07/26/10: Page 8 In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range
           values located in the table, the commercial TA header note has been removed
           Pages 10-14 In order to correct the footnotes of timing diagrams, CNTEN has been removed to reconcile the footnotes with
           the CNTEN logic definition found in Truth Table II - Address Counter Control
07/15/14: Page 1 Replaced Industrial 9ns with 12ns. Replaced Low Power Operation Standby from 600mW (typ) to
           1.32mW (typ) in the Features
           Page 2 Corrected some text typos
           Page 5 Removed the 9ns Industrial temp power values for the S & L offering in the DC Elec Chars table
           Page 6 Added the 12ns Industrial temp power value for the L offering in the DC Elec Chars table
           Pages 8 & 9 Updated the column headings of the AC Elec Chars table to indicate the Commercial and Industrial
           speed grade offerings
           Page 18 Updated all the Commercial and Industrial speed grade offerings and added
           Tape & Reel to Ordering Information
           Page 2 & 18 The label PN100-T changed to PN100 to match the standard package code
           Page 18 Corrected Old Flow-through Part number in table 13 to 70V907S/L25 & S/L30
02/20/18: Product Discontinuation Notice - PDN# SP-17-02
           Last time buy expires June 15, 2018
09/25/19: Page 1 & 18 Deleted obsolete Commercial speed grades 6/9/12/15ns in Features and Ordering Information
           Page 2 Rotated PNG100 TQFP pin configuration to accurately reflect pin 1 orientation
           Page 18 Added Orderable Part Information table