CMOS DUAL ASYNCHRONOUS FIFO
DUAL 256 x 9, DUAL 512 x 9,
DUAL 1,024 x 9, DUAL 2,048 x 9,
DUAL 4,096 x 9, DUAL 8,192 x 9

IDT7280
IDT7281
IDT7282
IDT7283
IDT7284
IDT7285

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:
- The IDT7280 is equivalent to two IDT7200 256 x 9 FIFOs
- The IDT7281 is equivalent to two IDT7201 512 x 9 FIFOs
- The IDT7282 is equivalent to two IDT7202 1,024 x 9 FIFOs
- The IDT7283 is equivalent to two IDT7203 2,048 x 9 FIFOs
- The IDT7284 is equivalent to two IDT7204 4,096 x 9 FIFOs
- The IDT7285 is equivalent to two IDT7205 8,192 x 9 FIFOs
- Low power consumption
  — Active: 685 mW (max.)
  — Power-down: 83 mW (max.)
- Ultra high speed—12 ns access time
- Asynchronous and simultaneous read and write
- Offers optimal combination of data capacity, small foot print and functional flexibility
- Ideal for bi-directional, width expansion, depth expansion, bus-matching, and data sorting applications
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CMOS technology
- Space-saving TSSOP
- Industrial temperature range (–40°C to +85°C) is available

DESCRIPTION:
The IDT7280/7281/7282/7283/7284/7285 are dual-FIFO memories that load and empty data on a first-in/first-out basis. These devices are functional and compatible to two IDT7200/7201/7202/7203/7204/7205 FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and write are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write (W) and Read (R) pins.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user’s option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit (RT) capability that allows for reset of the read pointer to its initial position when RT is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

These FIFOs are fabricated using high-speed CMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM

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**PIN CONFIGURATION**

```
FPA  1  o  56  XTA
QAD  2  55  DAd
QA1  3  54  DA1
QA2  4  53  DA2
QA3  5  52  DA3
QA6  6  51  DAs
GND  7  50  WA
QA9  8  49  DAb
QA10 9  48  DAa
QA11 10  47  DAs
QA12 11  46  DAa
QA13 12  45  DAs
XOA/QA13 13  44  FLAR TA
EFA  14  43  ASA
FFB  15  42  XIB
QB0  16  41  DB0
QB1  17  40  DB1
QB2  18  39  DB2
QB3  19  38  DB3
QB6  20  37  DB6
QB7  21  36  WB
RB  22  35  VCC
QB8  23  34  DB8
QB10 24  33  DB10
QB11 25  32  DB11
QB12 26  31  DB12
QB15 27  30  DB15
XOB/QB18 28  29  FLB/RTB
EFB  29  30  RSB
```

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Commercial &amp; Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM</td>
<td>Terminal Voltage with Respect to GND</td>
<td>–0.5 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–55 to +125°C</td>
<td>°C</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>–50 to +50 mA</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

1. For RT/RS/XI input, Vih = 2.6V (commercial).
2. 1.5V undershoots are allowed for 10ns once per cycle.

**DC ELECTRICAL CHARACTERISTICS**

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = –40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Commercial &amp; Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IIL(2)</td>
<td>Input Leakage Current (Any Input)</td>
<td>–1 to +1</td>
<td>μA</td>
</tr>
<tr>
<td>IOL(3)</td>
<td>Output Leakage Current</td>
<td>–10 to +10</td>
<td>μA</td>
</tr>
<tr>
<td>VOH</td>
<td>Output Logic “1” Voltage</td>
<td>2.4 to 2.4</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Logic “0” Voltage</td>
<td>0.4 to 0.4</td>
<td>V</td>
</tr>
<tr>
<td>ICC1(4)</td>
<td>Active Power Supply Current (both FIFOs)</td>
<td>125 to 150</td>
<td>mA</td>
</tr>
<tr>
<td>ICC2(4)</td>
<td>Standby Current (R = W = RS = FL/RT = V/1H)</td>
<td>15</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Measurements with 0.4 ≤ VIN ≤ VCC.
3. R ≥ Vih, 0.4 ≤ VOUT ≤ VCC.
4. Tested with outputs open (IOUT = 0).
5. Tested at f = 20 MHz.
6. Typical ICC1 = 2*I5 + 2*IS + 0.02*Cl*1s (in mA) with VCC = 5V, TA = 25°C, IS = WCLK frequency, RCLK frequency (in MHz, using TTL levels), data switching at fS/2, Cl = capacitive load (in pF).
7. All Inputs = VCC - 0.2V or GND + 0.2V.

**AC TEST CONDITIONS**

- Input Pulse Levels: GND to 3.0V
- Input Rise/Fall Times: 5ns
- Input Timing Reference Levels: 1.5V
- Output Reference Levels: 1.5V
- Output Load: See Figure 1

**CAPACITANCE** (TA = +25°C, f = 1.0 MHz)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Condition</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>VIN = 0V</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td>VOUT = 0V</td>
<td>8</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Characterized values, not currently tested.
### AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Industrial: Vcc = 5V ± 10%, TA = –40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Commercial &amp; Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>tS</td>
<td>Shift Frequency</td>
<td>—</td>
<td>50</td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>tA</td>
<td>Access Time</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tRR</td>
<td>Read Recovery Time</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tRPW</td>
<td>Read Pulse Width(3)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tHLZ</td>
<td>Read Pulse Low to Data Bus at Low Z(4)</td>
<td>3</td>
<td>—</td>
</tr>
<tr>
<td>tWLZ</td>
<td>Write Pulse High to Data Bus at Low Z(4,5)</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid from Read Pulse High</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>tHIZ</td>
<td>Read Pulse High to Data Bus at High Z(4)</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>tWPW</td>
<td>Write Pulse Width(3)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tIS</td>
<td>Data Set-up Time</td>
<td>9</td>
<td>—</td>
</tr>
<tr>
<td>tIH</td>
<td>Data Hold Time</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tRSC</td>
<td>Reset Cycle Time</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>tNS</td>
<td>Reset Pulse Width(3)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tRSS</td>
<td>Reset Set-up Time(4)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tRSR</td>
<td>Reset Recovery Time</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tRTC</td>
<td>Retransmit Cycle Time</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td>tRT</td>
<td>Retransmit Pulse Width(3)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tRTS</td>
<td>Retransmit Set-up Time(4)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tTRR</td>
<td>Retransmit Recovery Time</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tEF</td>
<td>Reset to Empty Flag Low</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tHFF</td>
<td>Reset to Half-Full and Full Flag High</td>
<td>—</td>
<td>17</td>
</tr>
<tr>
<td>tRFH</td>
<td>Retransmit Low to Flags Valid</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>tREF</td>
<td>Read Low to Empty Flag Low</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tRHF</td>
<td>Read High to Full Flag High</td>
<td>—</td>
<td>14</td>
</tr>
<tr>
<td>tRPE</td>
<td>Read Pulse Width after EF High</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tWFE</td>
<td>Write High to Empty Flag High</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tWFF</td>
<td>Write Low to Full Flag Low</td>
<td>—</td>
<td>14</td>
</tr>
<tr>
<td>tWHF</td>
<td>Write Low to Half-Full Flag Low</td>
<td>—</td>
<td>17</td>
</tr>
<tr>
<td>tWHF</td>
<td>Read High to Half-Full Flag High</td>
<td>—</td>
<td>17</td>
</tr>
<tr>
<td>tWPF</td>
<td>Write Pulse Width after FF High</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tXOL</td>
<td>Read/Write to X0 Low</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tXOH</td>
<td>Read/Write to X0 High</td>
<td>—</td>
<td>12</td>
</tr>
<tr>
<td>tX</td>
<td>X1 Pulse Width(3)</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tXR</td>
<td>X1 Recovery Time</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>tXIS</td>
<td>X1 Set-up Time</td>
<td>8</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for the 15ns speed grade is available as a standard device.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.
SIGNAL DESCRIPTIONS

INPUTS:
DATA IN (D0 – D8)
Data inputs for 9-bit wide data.

CONTROLS:
RESET (RS)
Reset is accomplished whenever the Reset (RS) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read Enable (R) and Write Enable (W) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., tRss before the rising edge of RS) and should not change until tRsr after the rising edge of RS. Half-Full Flag (HF) will be reset to HIGH after Reset (RS).

WRITE ENABLE (W)
A write cycle is initiated on the falling edge of this input if the Full Flag (FF) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable (W). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag (HF) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (HF) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag (FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag (FF) will go HIGH after tRF, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from W, so external changes in W will not affect the FIFO when it is full.

READ ENABLE (R)
A read cycle is initiated on the falling edge of the Read Enable (R) provided the Empty Flag (EF) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable (R) goes HIGH, the Data Outputs (Q0 – Q8) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag (EF) will go LOW, allowing the “final” read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid read operation has been accomplished, the Empty Flag (EF) will go HIGH after tREF and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from R so external changes in R will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT (FL/RT)
This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In (XI).

These devices can be made to retransmit data when the Retransmit Enable control (RT) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable (R) and Write Enable (W) must be in the HIGH state during retransmit. This feature is useful when less than 256/512/1,024/2,048/4,096/8,192 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag (HF), depending on the relative locations of the read and write pointers.

EXPANSION IN (XI)
This input is a dual-purpose pin. Expansion In (XI) is grounded to indicate an operation in the single device mode. Expansion In (XI) is connected to Expansion Out (XO) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:
FULL FLAG (FF)
The Full Flag (FF) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset (RS), the Full-Flag (FF) will go LOW after 256 writes for IDT7280, 512 writes for the IDT7281, 1,024 writes for the IDT7282, 2,048 writes for the IDT7283, 4,096 writes for the IDT7284 and 8,192 writes for the IDT7285.

EMPTY FLAG (EF)
The Empty Flag (EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG (XO/HF)
This is a dual-purpose output. In the single device mode, when Expansion In (XI) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag (HF) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (HF) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In (XI) is connected to Expansion Out (XO) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0 – Q8)
Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read (R) is in a HIGH state.
NOTES:
1. EF, FF, HF may change status during Reset, but flags will be valid at tRSC.
2. W and R = V_H around the rising edge of RS.

Figure 2. Reset

Figure 3. Asynchronous Write and Read Operation

Figure 4. Full Flag From Last Write to First Read
Figure 5. Empty Flag From Last Read to First Write

Figure 6. Retransmit

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse
OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. FF is monitored on the device where W is used; EF is monitored on the device where R is used).

SINGLE DEVICE MODE

A single IDT7280/7281/7282/7283/7284/7285 may be used when the application requirements are for 256/512/1,024/2,048/4,096/8,192 words or less. These FIFOs are in a Single Device Configuration when the Expansion In (XI) control input is grounded (see Figure 12).

DEPTH EXPANSION

These devices can easily be adapted to applications when the requirements are for greater than 256/512/1,024/2,048/4,096/8,192 words. Figure 14 demonstrates a four-FIFO Depth Expansion using two IDT7280/7281/7282/7283/7284/7285s. Any depth can be attained by adding additional IDT7280/7281/7282/7283/7284/7285s. These FIFOs operate in the Depth Expansion mode when the following conditions are met:

1. The first FIFO must be designated by grounding the First Load (FL) control input.
2. All other FIFOs must have FL in the HIGH state.
3. The Expansion Out (XO) pin of each device must be tied to the Expansion In (XI) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag (FF) and Empty Flag (EF). This requires the ORing of all EFs and ORing of all FFs (i.e. all must be set to generate the correct composite FF or EF). See Figure 14.
5. The Retransmit (RT) function and Half-Full Flag (HF) are not available in the Depth Expansion Mode.
**USAGE MODES:**

**WIDTH EXPANSION**

Word width may be increased simply by connecting the corresponding input control signals of multiple FIFOs. Status flags (EF, FF and HF) can be detected from any one FIFO. Figure 13 demonstrates an 18-bit word width by using the two FIFOs contained in the IDT7280/7281/7282/7283/7284/7285s. Any word width can be attained by adding FIFOs (Figure 13).

**BIDIRECTIONAL OPERATION**

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7280/7281/7282/7283/7284/7285s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

**DATA FLOW-THROUGH**

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in \((t_{WEF} + t_A)\) ns after the rising edge of \(W\), called the first write edge, and it remains on the bus until the \(R\) line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after \(tr_{HZ}\) ns. The \(EF\) line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The \(R\) line causes the \(FF\) to be deasserted but the \(W\) line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of \(W\), the new word is loaded in the FIFO. The \(W\) line must be toggled when \(FF\) is not asserted to write new data in the FIFO and to increment the write pointer.

**COMPOUND EXPANSION**

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).
TABLE 1 — RESET AND RETRANSMIT
Single Device Configuration/Width Expansion Mode

<table>
<thead>
<tr>
<th>Mode</th>
<th>Inputs</th>
<th>Internal Status</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RS</td>
<td>RT</td>
<td>XI</td>
</tr>
<tr>
<td>Reset</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>Retransmit</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read/Write</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Pointer will increment if flag is High.

TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE
Depth Expansion/Compound Expansion Mode

<table>
<thead>
<tr>
<th>Mode</th>
<th>Inputs</th>
<th>Internal Status</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RS</td>
<td>FL</td>
<td>XI</td>
</tr>
<tr>
<td>Reset First Device</td>
<td>0</td>
<td>0</td>
<td>(1)</td>
</tr>
<tr>
<td>Reset All Other Devices</td>
<td>0</td>
<td>1</td>
<td>(1)</td>
</tr>
<tr>
<td>Read/Write</td>
<td>1</td>
<td>X</td>
<td>(1)</td>
</tr>
</tbody>
</table>

**NOTE:**
1. XI is connected to XO of previous device. See Figure 14. RS = Reset Input, FL/RT = First Load/Retransmit, EF = Empty Flag Output, FF = Full Flag Output, XI = Expansion Input, HF = Half-Full Flag Output.

Figure 14. Block Diagram of 1,024 x 9, 2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9 FIFO Memory (Depth Expansion)
NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

Figure 16. Bidirectional FIFO Mode
Figure 17. Read Data Flow-Through Mode

Figure 18. Write Data Flow-Through Mode
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
<th>Process/ Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>XXXX</td>
<td>X</td>
<td>XXXX</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Blank**: Tube or Tray Tape and Reel
- **1**: Commercial (0°C to +70°C)
- **1(1)**: Industrial (-40°C to +85°C)
- **G(1)**: Green
- **PA**: Thin Shrink SOIC (TSSOP, SO56-2)
- **12**: Commercial Only
- **15**: Commercial and Industrial
- **L**: Low Power

<table>
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<tr>
<th>Access Time (tA)</th>
<th>Speed in Nanoseconds</th>
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<td>3208 drw 21</td>
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**Notes:**
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Green parts are available. For specific speeds and packages contact your local sales office.

**LEAD FINISH** (SnPb) parts are in EOL process. **Product Discontinuation Notice - PDN# SP-17-02**

**Device Type**
- **7280**: 256 x 9 — CMOS Dual Asynchronous FIFO
- **7281**: 512 x 9 — CMOS Dual Asynchronous FIFO
- **7282**: 1,024 x 9 — CMOS Dual Asynchronous FIFO
- **7283**: 2,048 x 9 — CMOS Dual Asynchronous FIFO
- **7284**: 4,096 x 9 — CMOS Dual Asynchronous FIFO
- **7285**: 8,192 x 9 — CMOS Dual Asynchronous FIFO

**Tape and Reel**

**Tube or Tray**

**DATASHEET DOCUMENT HISTORY**

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<td>01/13/2009</td>
<td>12</td>
<td>pg. 12.</td>
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<td>06/29/2012</td>
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