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# 1 PIN ASSIGNMENT

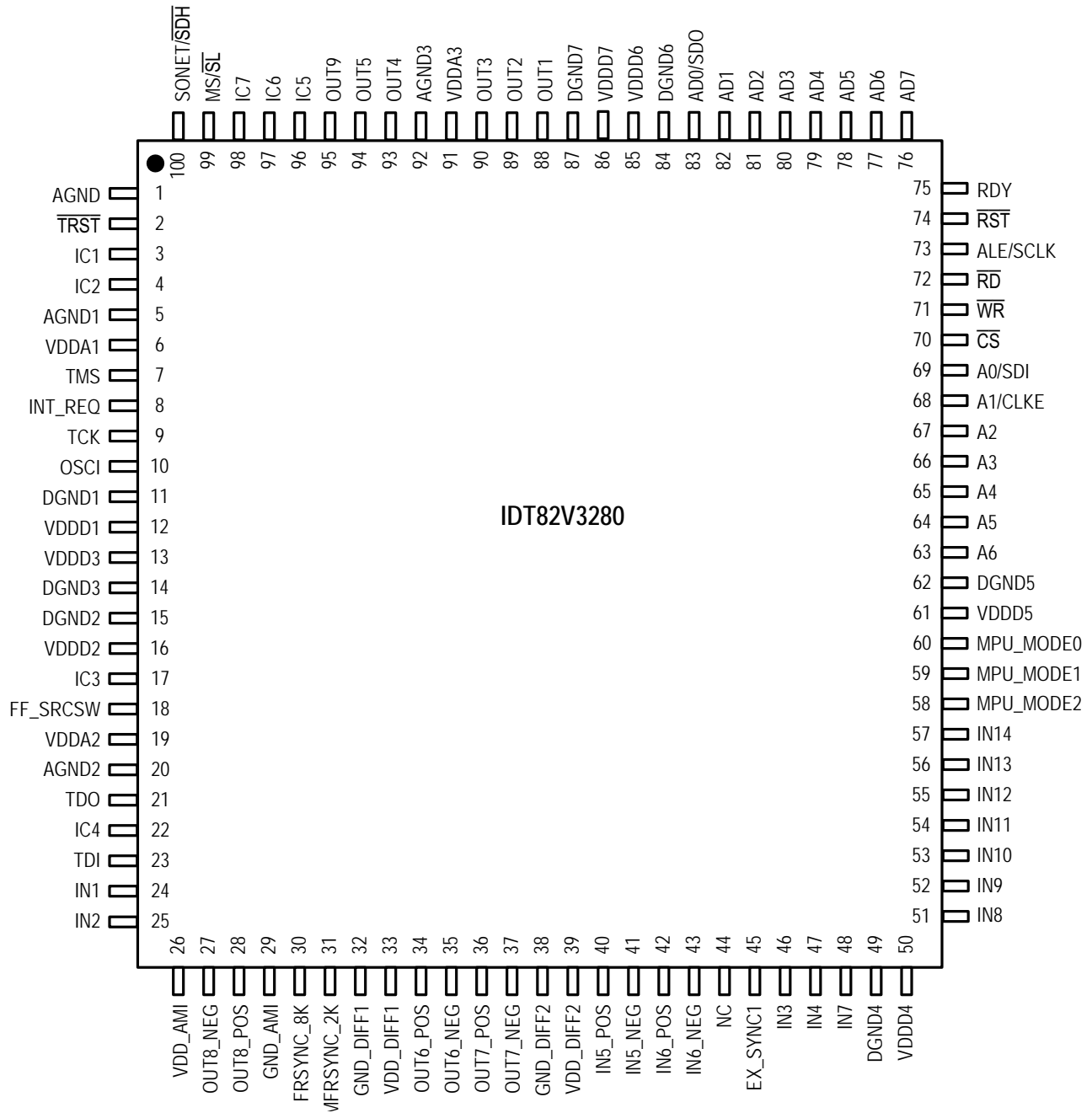


Figure 2. Pin Assignment (Top View)





































































































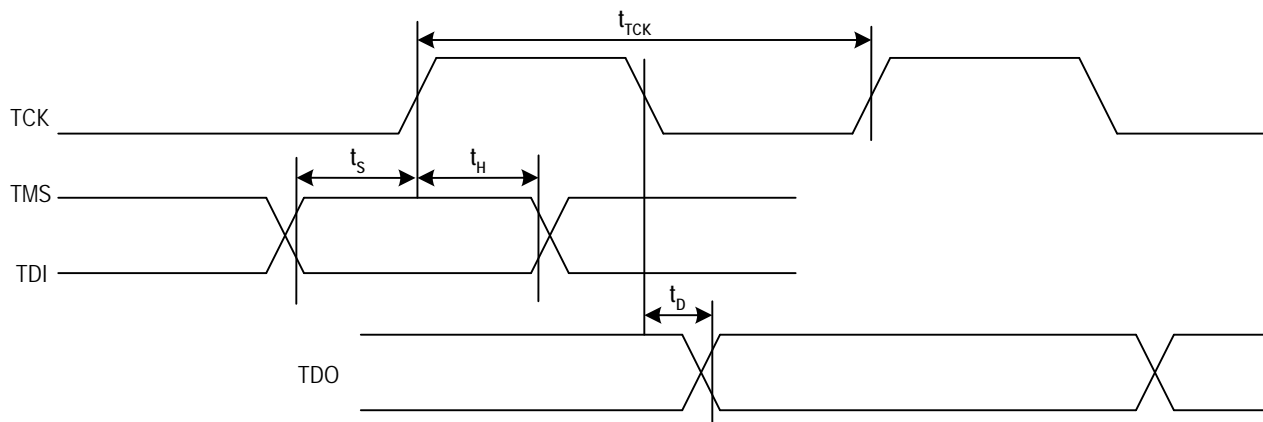


## 6 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The  $\overline{\text{TRST}}$  pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in [Figure 26](#).



**Figure 26. JTAG Interface Timing Diagram**

**Table 41: JTAG Timing Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{TCK}$	TCK period	100			ns
$t_s$	TMS / TDI to TCK setup time	25			ns
$t_H$	TCK to TMS / TDI Hold Time	25			ns
$t_D$	TCK to TDO delay time			50	ns































































































































































































































































