700MHz, Low Jitter, Crystal-to-3.3V Differential LVPECL Frequency

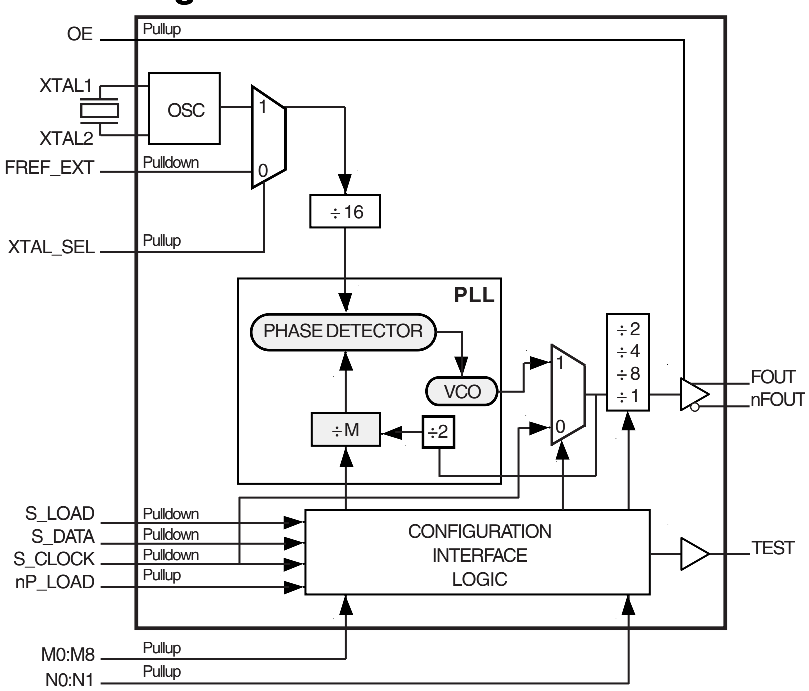
General Description

The 84330C is a general purpose, single output high frequency synthesizer. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The output can be configured to divide the VCO frequency by 1, 2, 4, and 8. Output frequency steps as small as 250kHz to 2MHz can be achieved using a 16MHz crystal depending on the output divider settings.

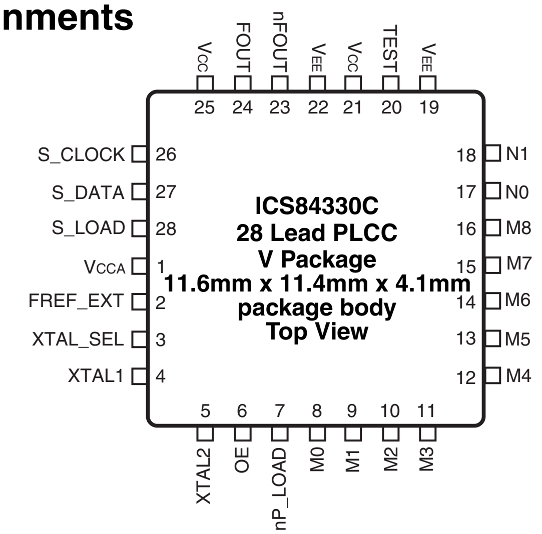
Features

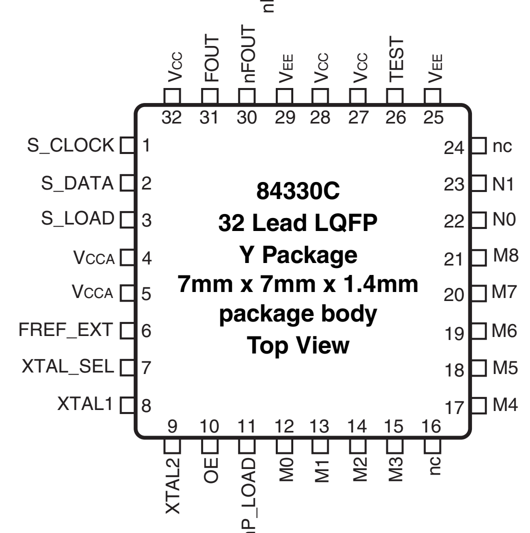
- Fully integrated PLL, no external loop filter requirements
- One differential 3.3V LVPECL output
- Crystal oscillator interface: 10MHz to 25MHz
- Output frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming M and N dividers during power-up
- RMS period jitter: 5ps (maximum)
- Cycle-to-cycle jitter: 40ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignments





Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.

The 84330C features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A quartz crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal, this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 84330C support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fXTAL}{16} \times 2M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as 125 ≤ M ≤ 350. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fXTAL}{16} \times \frac{2M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T2:T0. The internal registers T2:T0 determine the state of the TEST output as follows in the table below:

T2	T1	T0	TEST Output	f_{OUT}
0	0	0	Shift Register Out	f_{OUT}
0	0	1	HIGH	f_{OUT}
0	1	0	PLL Reference XTAL ÷16	f_{OUT}
0	1	1	(VCO ÷ M)/2 (non 50% Duty Cycle M Divider)	f_{OUT}
1	0	0	f_{OUT}, LVCMOS Output Frequency < 200MHz	f_{OUT}
1	0	1	LOW	f_{OUT}
1	1	0	(S_CLOCK ÷ M)/2 (non 50% Duty Cycle M Divider)	S_CLOCK ÷ N Divider
1	1	1	f_{OUT} ÷ 4	f_{OUT}

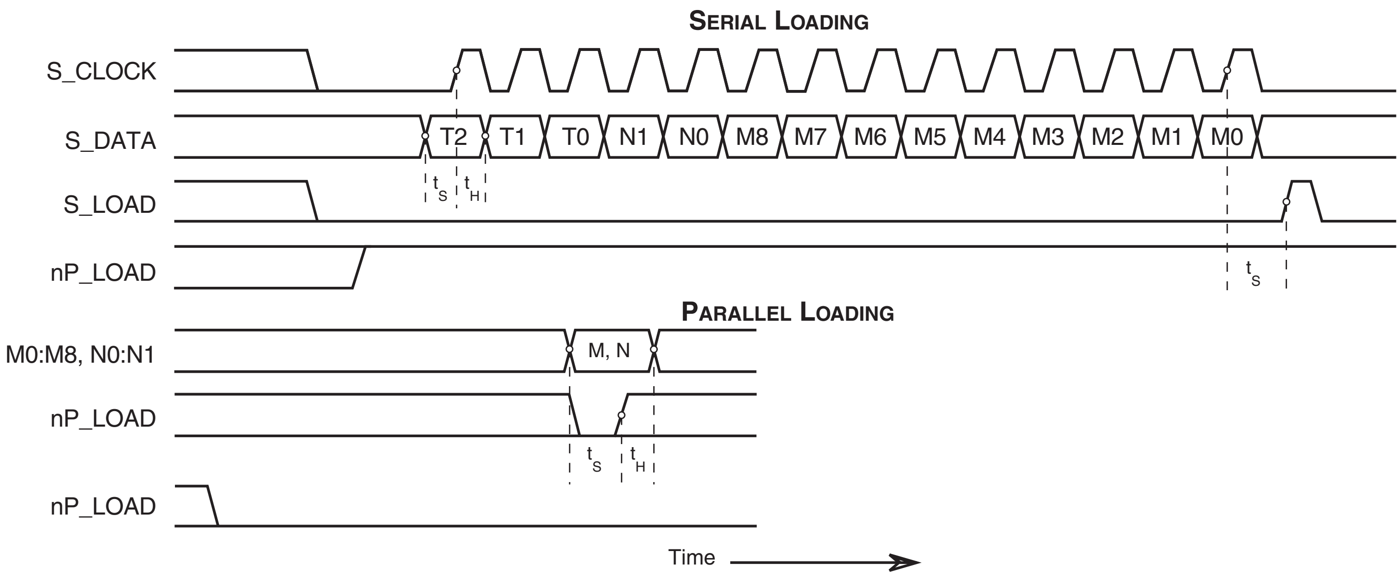


Figure 1. Parallel & Serial Load Operations

Table 1. Pin Descriptions

Name	Type		Description
V_{CCA}	Power		Analog supply pin.
XTAL1, XTAL2			Crystal oscillator interface. XTAL1 is an oscillator input, XTAL2 is an oscillator output.
XTAL_SEL	Input	Pullup	Selects between the crystal oscillator or FREF_EXT inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects FREF_EXT when LOW. LVCMOS / LVTTL interface levels.
OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels.
nP_LOAD	Input	Pullup	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divide value. LVCMOS / LVTTL interface levels.
M0, M1, M2 M3, M4, M5 M6, M7, M8	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
N0, N1	Input	Pullup	Determines N output divider value as defined in Table 3C Function Table. LVCMOS / LVTTL interface levels.
V_{EE}	Power		Negative supply pins.
TEST	Output		Test output which is used in the serial mode of operation. Single-ended LVPECL interface levels.
V_{CC}	Power		Core supply pins.
nFOUT, FOUT	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
nc	Unused		No connect.
FREF_EXT	Input	Pulldown	PLL reference input. LVCMOS / LVTTL interface levels.
S_CLOCK	Input	Pulldown	Clocks the serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
S_LOAD	Input	Pulldown	Controls transition of data from shift register into the M divider. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs						
nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	Conditions
X	X	X	X	X	X	Reset. M and N bits are all set HIGH.
L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST mode 000.
↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
H	X	X	↓	L	Data	M divider and N output divider values are latched.
H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	125	0	0	1	1	1	1	1	0	1
252	126	0	0	1	1	1	1	1	1	0
254	127	0	0	1	1	1	1	1	0	1
256	128	0	1	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	348	1	0	1	0	1	1	1	0	0
698	349	1	0	1	0	1	1	1	0	1
700	350	1	0	1	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 16MHz.

Table 3C. Programmable Output DividerFunction Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	2	125	350
0	1	4	62.5	175
1	0	8	31.25	87.5
1	1	1	250	700

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA} 28 Lead PLCC 32 Lead LQFP 32 Lead VFQFN	 37.8°C/W (0 lfpm) 47.9°C/W (0 lfpm) 37.0°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				160	mA
I_{CCA}	Analog Supply Current				16	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	M0-M8, N0, N1, OE, nP_LOAD, XTAL_SEL	$V_{CC} = V_{IN}$ = 3.465V			5	µA
		S_LOAD, S_CLOCK FREF_EXT, S_DATA	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	M0-M8, N0, n1, OE, nP_LOAD, XTAL_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		S_LOAD, S_CLOCK FREF_EXT, S_DATA	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} -2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

Table 6. Input Frequency Characteristics, V_{CC} = 3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL; NOTE 1		10		25	MHz
		S_CLOCK				50	MHz
		FREF_EXT; NOTE 2		10			MHz

NOTE 1: For the crystal frequency range, the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz to 700MHz. Using the minimum input frequency of 10MHz, valid values of M are 200 ≤ M ≤ 511. Using the maximum input frequency of 25MHz, valid values of M are 80 ≤ M ≤ 224.
NOTE 2: Maximum frequency on FREF_EXT is dependent on the internal M counter limitations. See Application Information Section for recommendations on optimizing the performance using the FREF_EXT input.

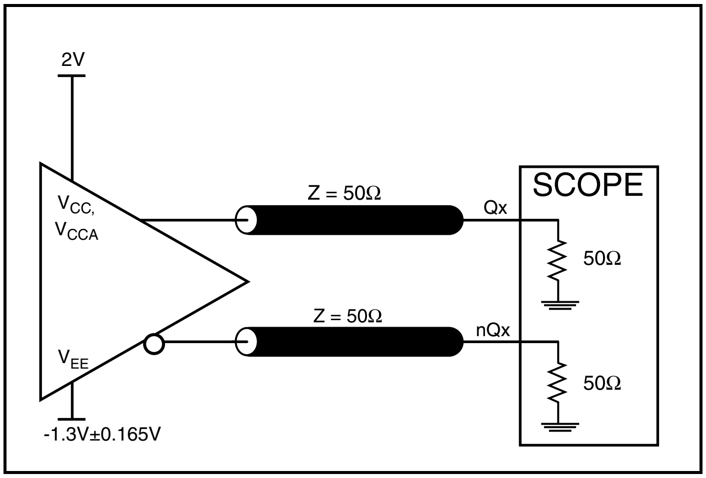
AC Electrical Characteristics

Table 7. AC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

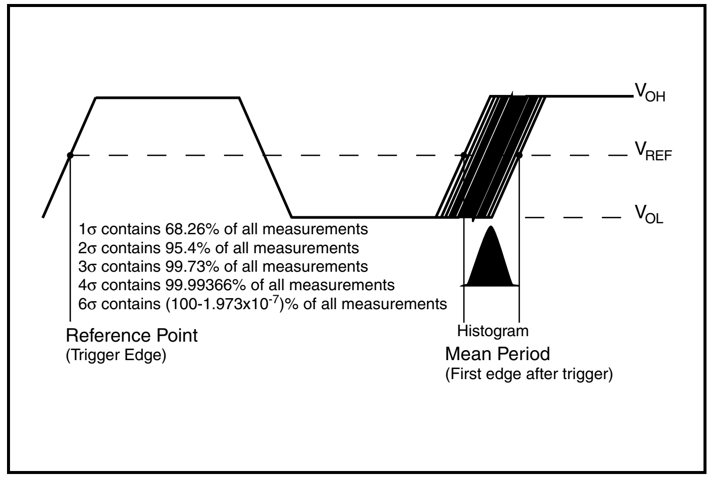
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					700	MHz
*t*jit(per)	Period Jitter, RMS; NOTE 1. 2					5	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2					40	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		600	ns
t_S	Setup Time	S_DATA to S_CLOCK		20			ns
		S_CLOCK to S_LOAD		20			ns
		M, N to nP_LOAD		20			ns
t_H	Hold Time	S_DATA to S_CLOCK		20			ns
		M, N to nP_LOAD		20			ns
t_L	PLL Lock Time					10	ms
odc	Output Duty Cycle			45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information section.
NOTE: Characterized using 16MHz XTAL.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: See Applications section.

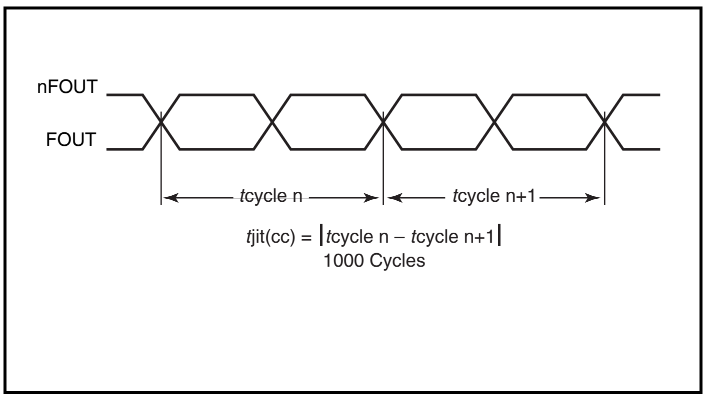
Parameter Measurement Information



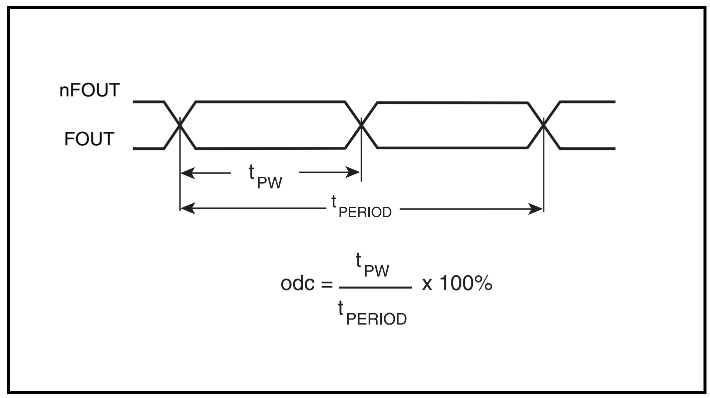
3.3/3.3V LVPECL Output Load AC Test Circuit



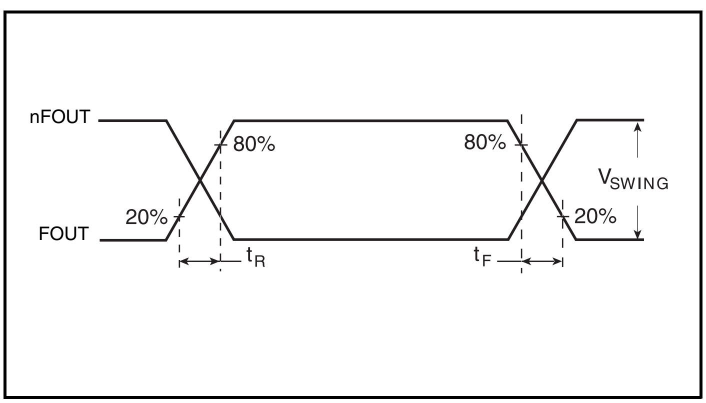
Period Jitter



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter perform- ance, power supply isolation is required. The 84330C provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

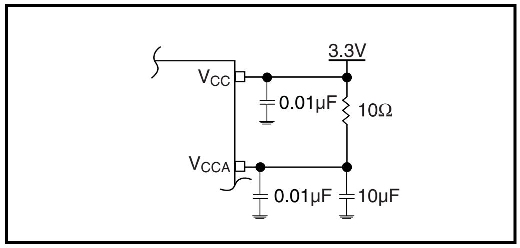


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

TEST Output

The unused TEST output can be left floating. There should be no trace attached.

LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

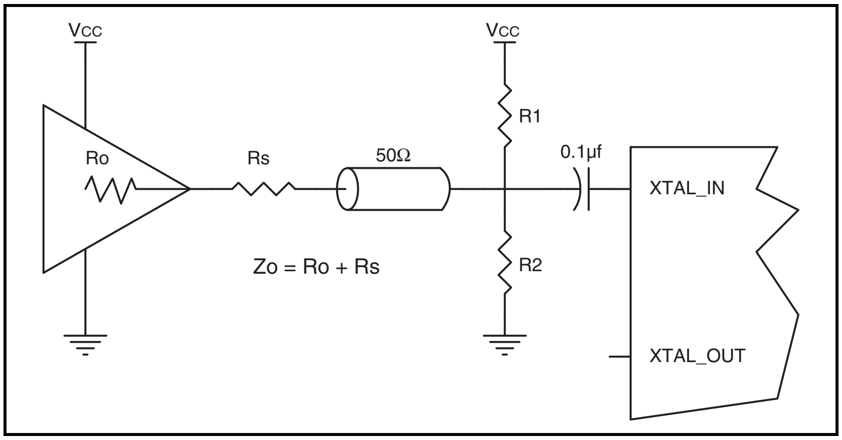


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

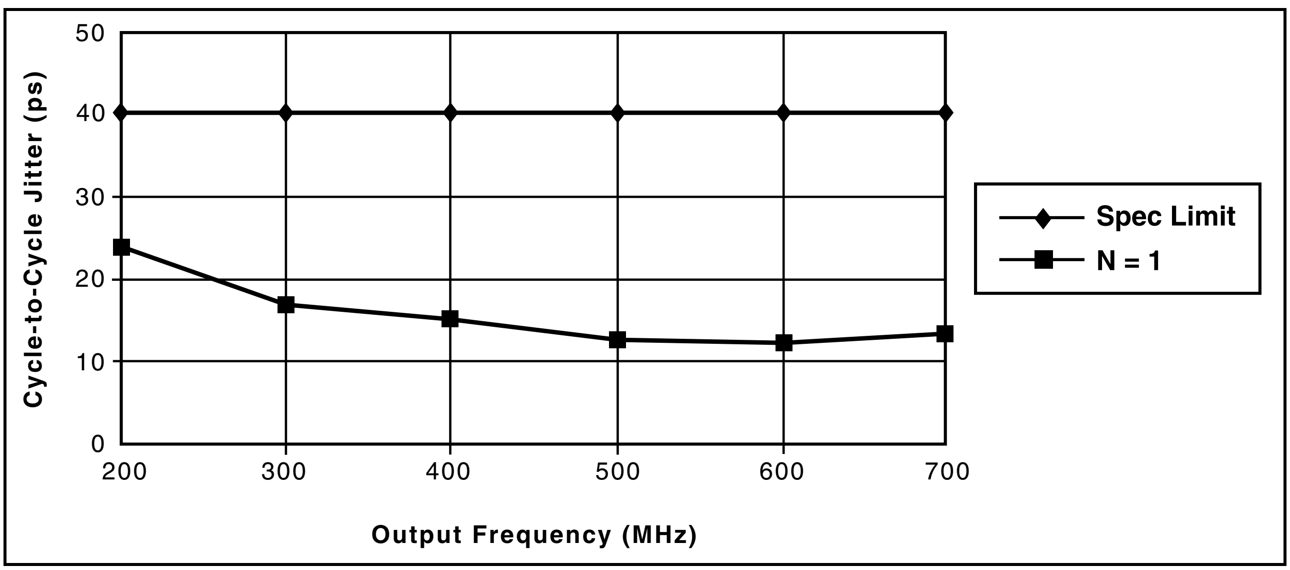


Figure 4. Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz crystal)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

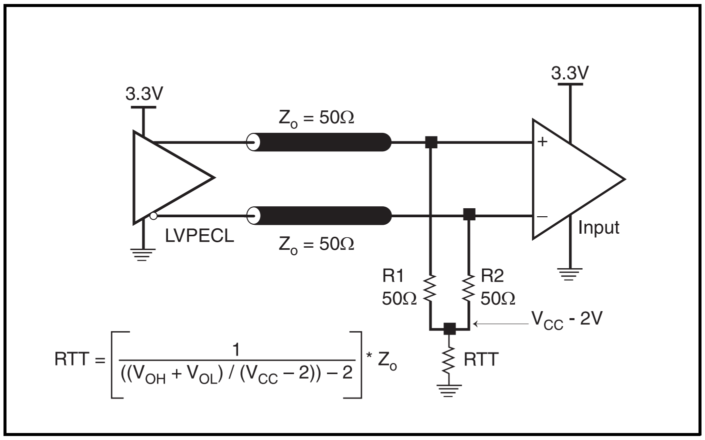


Figure 5A. 3.3V LVPECL Output Termination

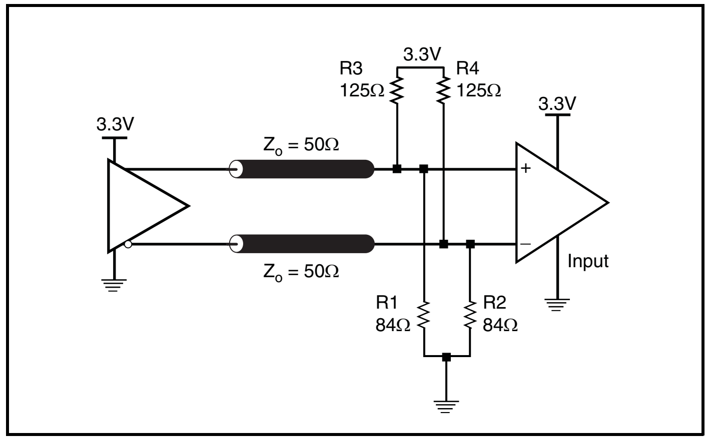


Figure 5B. 3.3V LVPECL Output Termination

Layout Guideline

The schematic of the 84330C layout example used in this layout guideline is shown in *Figure 6A.* The 84330C recommended PCB board layout for this example is shown in *Figure 6B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

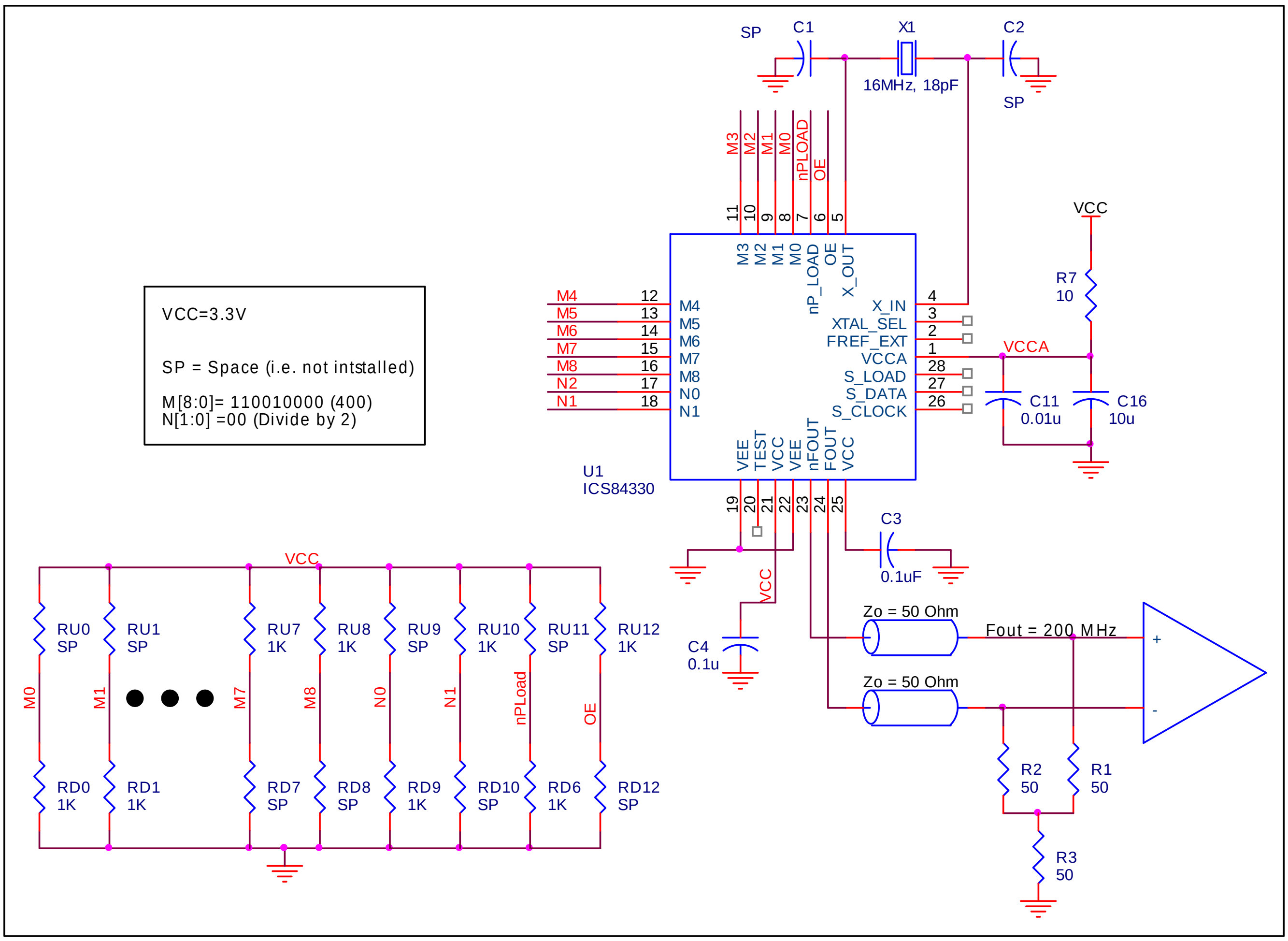


Figure 6A. 84330C Schematic of Recommended Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C3 and C4, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.

- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.

- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.

- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.

- Make sure no other signal traces are routed between the clock trace pair.

- The matching termination resistors should be located as close to the receiver input pins as possible.

Crystal

The crystal X1 should be located as close as possible to the pins 4 (XTAL1) and 5 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

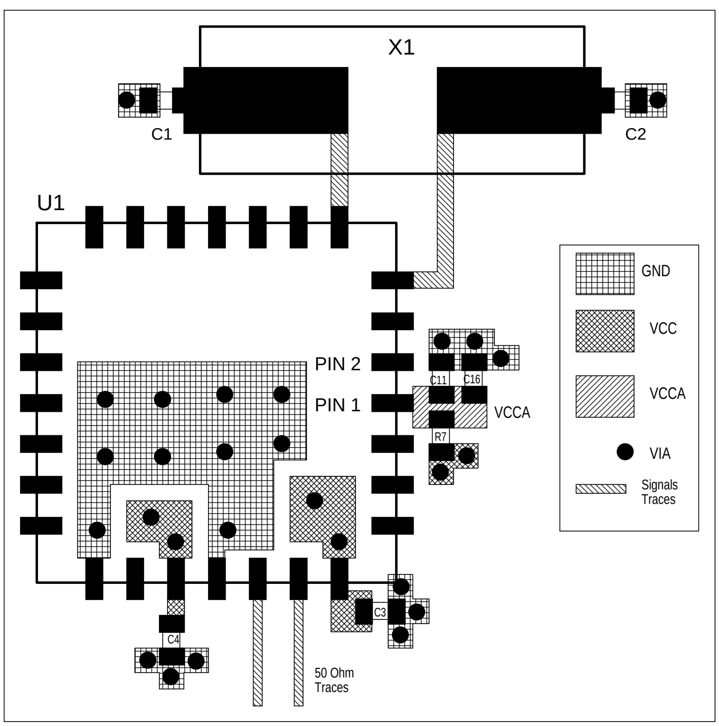


Figure 6B. 84330C PCB Board Layout for 84330C

Power Considerations

This section provides information on power dissipation and junction temperature for the 84330C.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 84330C is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 176mA = **609.8mW**
- Power (outputs)$_{MAX}$=**30mW/Loaded Output Pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 609.8mW + 30mW = **639.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 8A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.640W * 31.1°C/W = 89.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 8A. Thermal Resistance θ_{JA} for 28 Lead PLCC, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

Table 8B. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Table 8C. Thermal Resistance θ_{JA} for 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

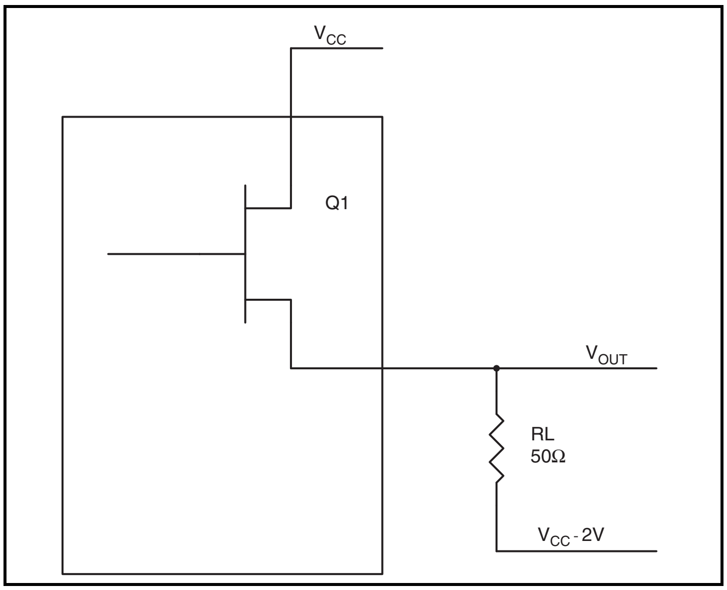


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9A. θ_{JA} vs. Air Flow Table for a 28 Lead PLCC

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

Table 9B. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Table 9C. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for 84330C is: 4498

Pin compatible with the MC12430

Package Outline and Package Dimensions

Package Outline - V Suffix for 28 Lead PLCC

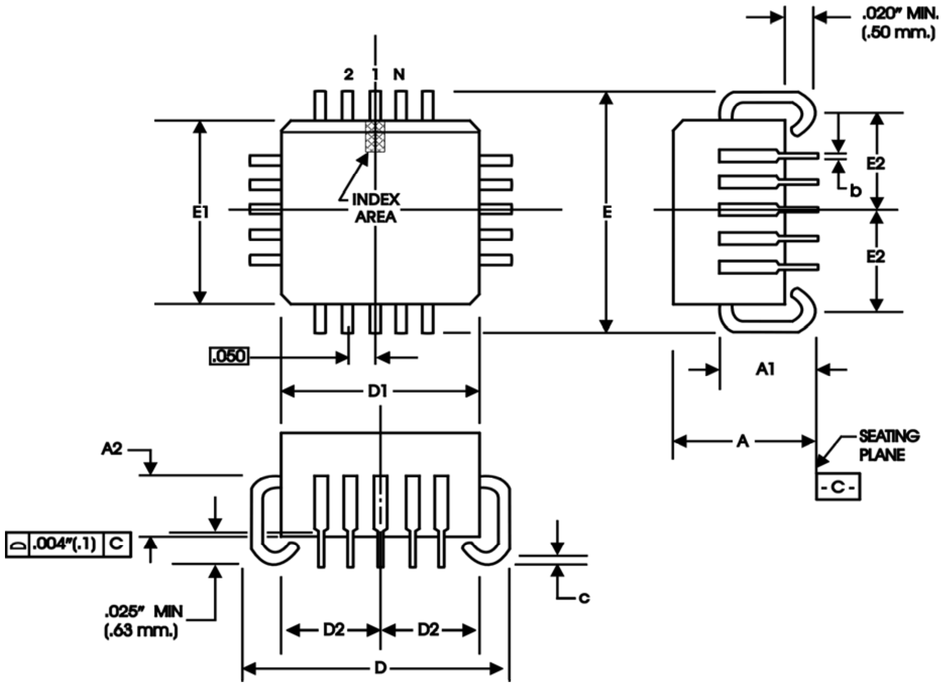


Table 10A. Package Dimensions for 28 Lead PLCC

JEDEC Variation All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D/E	12.32	12.57
D1/E1	11.43	11.58
D2/E2	5.21	5.46

Reference Document: JEDEC Publication 95, MS-018

Package Outline - Y Suffix for 32 Lead LQFP

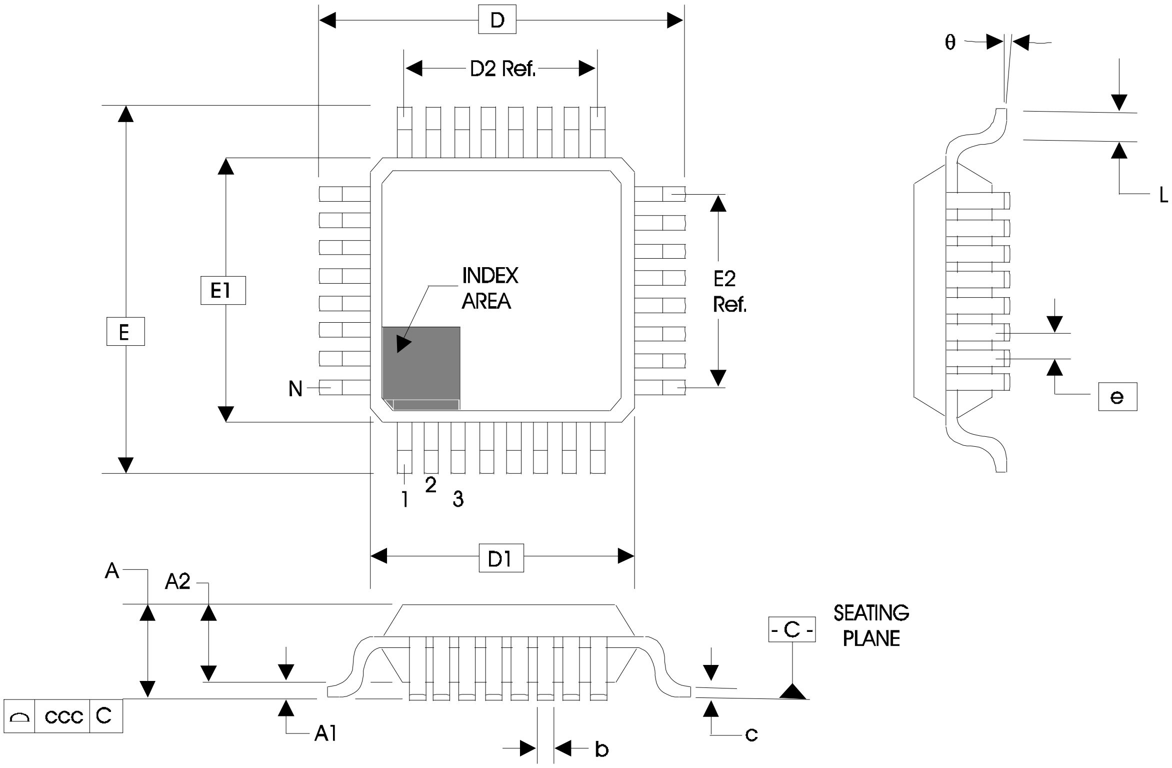


Table 10B. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBA All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
84330CVLN	ICS84330CVLN	“Lead-Free” 28 Lead PLCC	Tube	0°C to 70°C
84330CVLNT	ICS84330CVLN	“Lead-Free” 28 Lead PLCC	500 Tape & Reel	0°C to 70°C
84330CYLN	ICS84330CYLN	“Lead-Free/Annealed” 32 Lead LQFP	Tube	0°C to 70°C
84330CYLNT	ICS84330CYLN	“Lead-Free/Annealed” 32 Lead LQFP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LN" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	 T1 T4B T5	2 3 5 6 8	Updated Parallel & Serial Load Operations Diagram. Pin Description Table - description to TEST output should read Single-ended LVPECL interface levels instead of LVCMOS/LVTTL interface levels. LVCMOS Table - V_{OH}/V_{OL} levels added TEST pin and changed V_{OH} min. from 2.6V to V_{CC} - 1.4V; changed V_{OL} max. from 0.5V to V_{CC} - 1.7V. Crystal Characteristics Table - changed ESR from 70Ω max. to 50Ω max. Updated LVPECL Output Termination diagrams.	8/28/03
B	T4B	5	Deleted V_{OH} & V_{OL} row entries from LVCMOS Table.	9/10/03
B	T12	18	Added Lead-Free/Annealed to the Part Ordering Information Table.	6/1/04
B	 T12	1 18	Features Section added Lead-Free bullet. Ordering Information Table - added PLCC Lead-Free part number.	10/5/04
B		1	Features Section - corrected Output Frequency Range from 25MHz to 31.25MHz	12/7/04
C	T3A T4C	4 5 13 - 14	Parallel & Serial Mode Function Table - corrected 3rd line in S_LOAD column from “X” to “L”. LVPECL DC Characteristics Table - corrected V_{OH} max. from V_{CC} -1.0V to V_{CC} -0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max. in Table 4C.	4/10/07
C	 T10A	8 17	Added *Recommendations for Unused Input and Output Pins.* Package Dimension Table - D2/E2 changed the min. from 4.85 to 5.21 and the max. from 5.56 to 5.46.	1/28/09
D	 T10C T11	1 5 18 19	Added 32 VFQFN Pin Assignment. Absolute Maximum Ratings - add 32 VFQFN Package Thermal Impedance. Added 32 VFQFN Package Dimensions and Diagram. Ordering Information Table - added 32 VFQFN ordering information.	7/17/09
D	T11	19	Ordering Information - removed leaded devices and the CKLF package. Updated data sheet format.	4/22/15

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