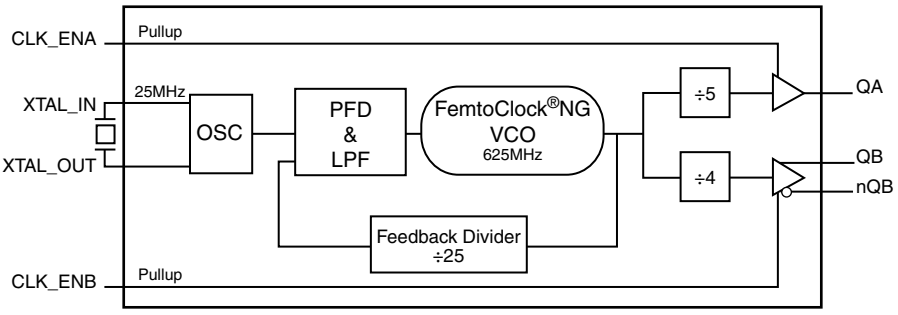
General Description

The 843N252-45 is a 1 LVPECL and 1 LVCMOS output Synthesizer optimized to generate Ethernet reference clock frequencies. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. Using a 25MHz parallel resonant crystal, the following frequencies can be generated: 156.25MHz and 125MHz. With a very low phase noise VCO it is targeted to achieve 0.4ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843N252-45 is packaged in a small 16-pin TSSOP package.

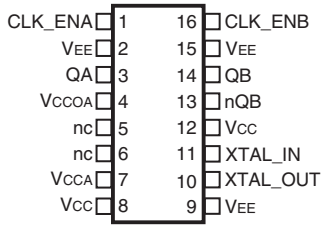
Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- One differential 3.3V LVPECL output and one LVCMOS/LVTTL output
- Crystal oscillator interface designed for a 25MHz parallel resonant crystal
- A 25MHz crystal generates output frequencies of: 156.25MHz and 125MHz
- VCO frequency: 625MHz
- RMS Phase Jitter @ 156.25MHz, (12kHz – 20MHz) using a 25MHz crystal: 0.33ps (typical)
- RMS Phase Jitter @ 125MHz, (12kHz – 20MHz) using a 25MHz crystal: 0.39ps (typical)
- Power supply noise rejection PSNR: -60dB (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



843N252-45

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_ENA	Input	Pullup	Clock enable pin. LVCMOS/LVTTL interface levels. See Table 3A.
2, 9, 15	V_{EE}	Power		Negative supply pins.
3	QA	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
4	V_{CCOA}	Power		Output supply pin for QA output.
5, 6	nc	Unused		No connect.
7	V_{CCA}	Power		Analog supply pin.
8, 12	V_{CC}	Power		Power supply pin.
10 11	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.
13, 14	nQB, QB	Output		Differential output pair. LVPECL interface levels.
16	CLK_ENB	Input	Pullup	Clock enable pin. LVCMOS/LVTTL interface levels. See Table 3B.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance		$V_{CC} = V_{CCO\_A} = 3.465V$		7		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	QA	$V_{CCO\_A} = 3.465V$		15		Ω

Function Tables

Table 3A. CLK_ENA Function Table

Input	Outputs
CLK_ENA	QA
0	High-Impedance
1	Active

Table 3B. CLK_ENB Function Table

Input	Outputs	
CLK_ENB	QB	nQB
0	HIGH	LOW
1	Active	Active

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCOA} + 0.5V
Outputs, I_O (LVPECL) Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	94.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCOA} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.14	3.3	V_{CC}	V
V_{CCOA}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current				14	mA
I_{EE}	Power Supply Current	No Load			124	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCOA} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_ENA, CLK_ENB	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK_ENA, CLK_ENB	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{CCOA} = 3.3V \pm 5\%$	2.3			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCOA} = 3.3V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCOA}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.75	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.55		1.05	V

NOTE 1: Output termination with 50Ω to V_{CC} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

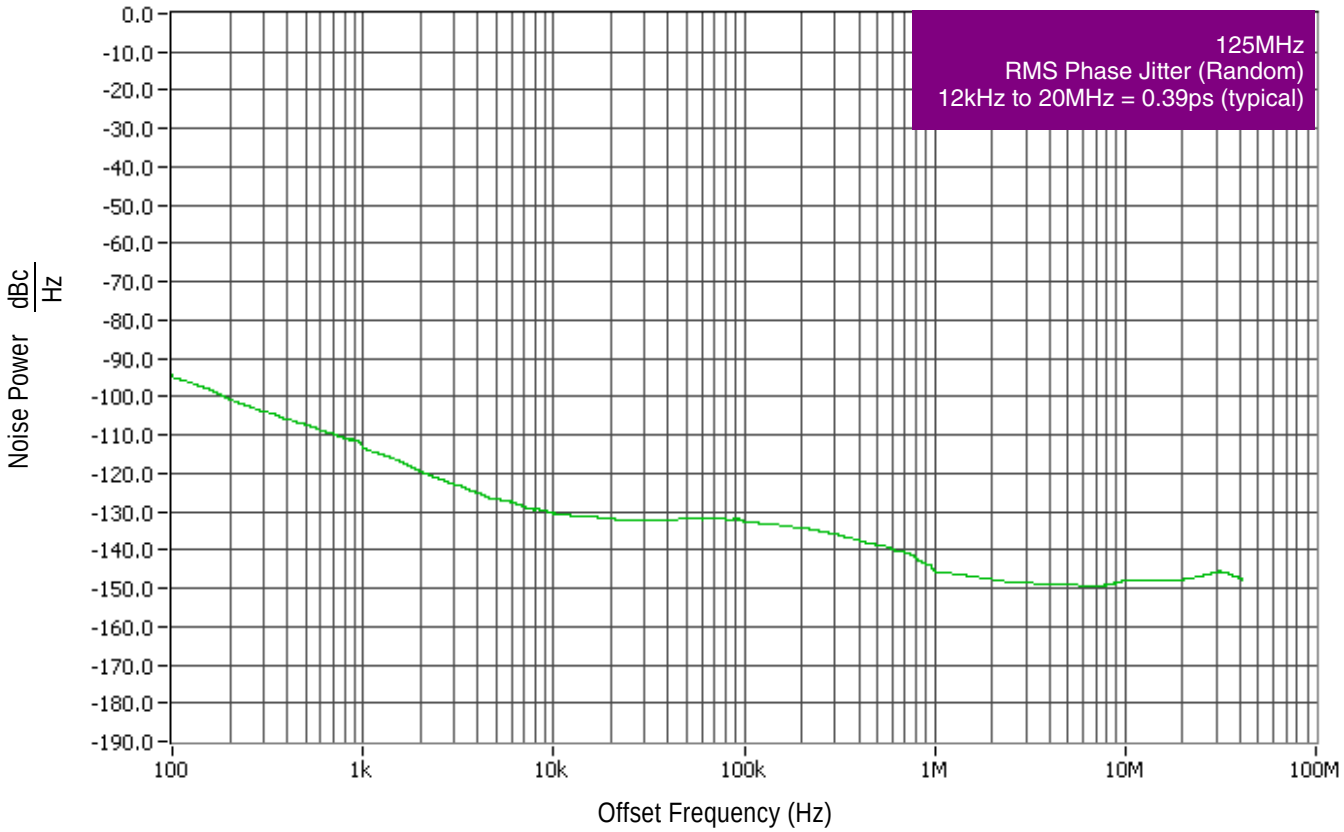
AC Electrical Characteristics

Table 6. AC Characteristics, V_{CC} = V_{CCOA} = 3.3V ± 5%, V_{EE} = 0V, T_A = 0°C to 70°C

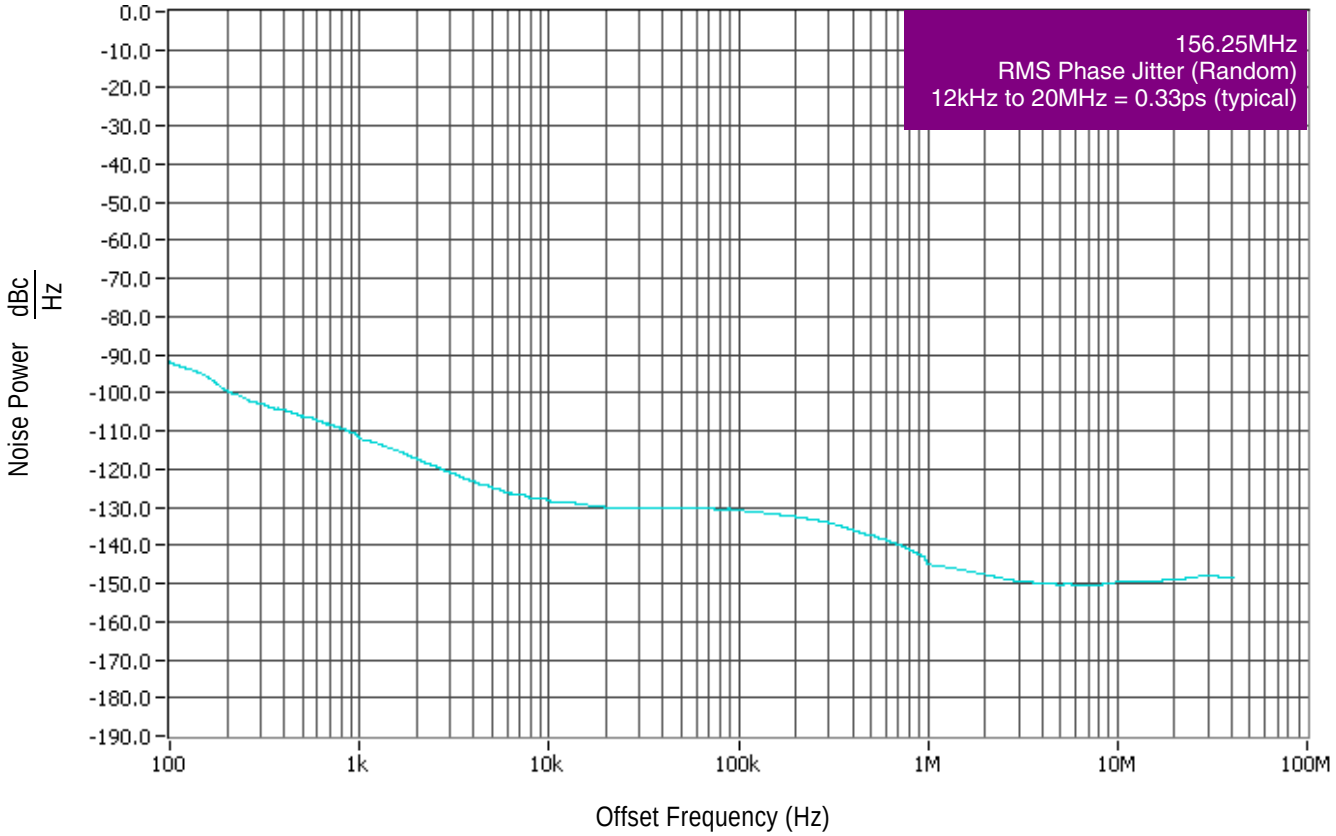
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA			125		MHz
		QB, nQB			156.25		MHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 1	QA	125MHz, Integration Range: 12kHz – 20MHz		0.39		ps
		QB, nQB	156.25MHz, Integration Range: 12kHz – 20MHz		0.33		ps
PSNR	Power Supply Noise Reduction		From DC to 10MHz		-60		dB
t_R / t_F	Output Rise/Fall Time	QA	20% to 80%	250		500	ps
		QB, nQB	20% to 80%	150		300	ps
odc	Output Duty Cycle	QA		47		53	%
		QB, nQB		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Using a 25MHz, 12pF quartz crystal.
NOTE 1: Please refer to the Phase Noise plots.

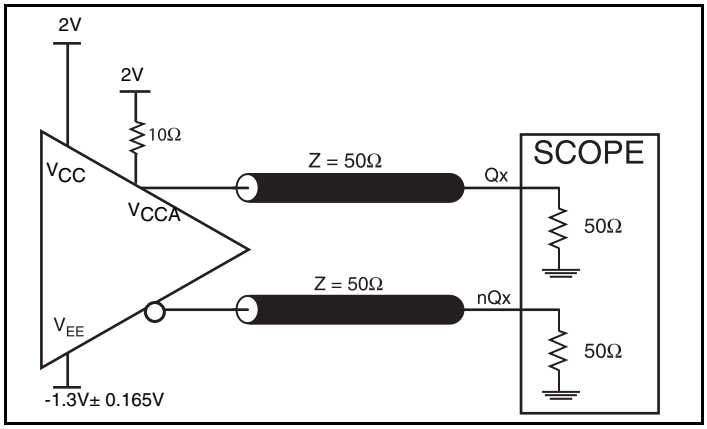
Typical Phase Noise at 125MHz



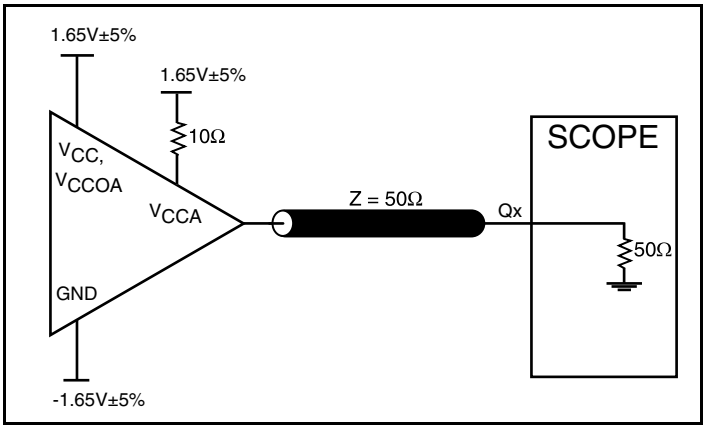
Typical Phase Noise at 156.25MHz



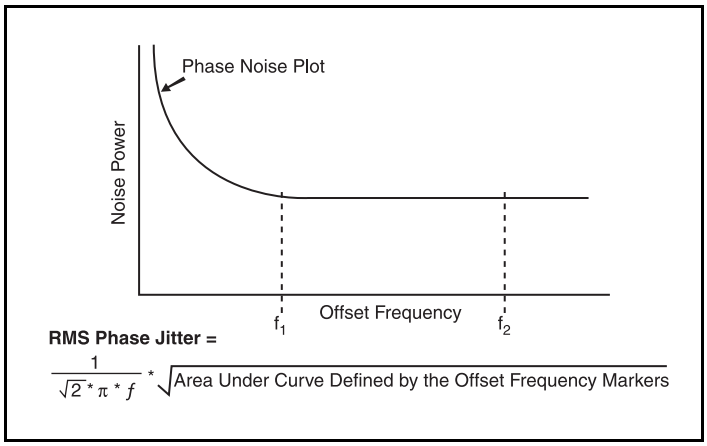
Parameter Measurement Information



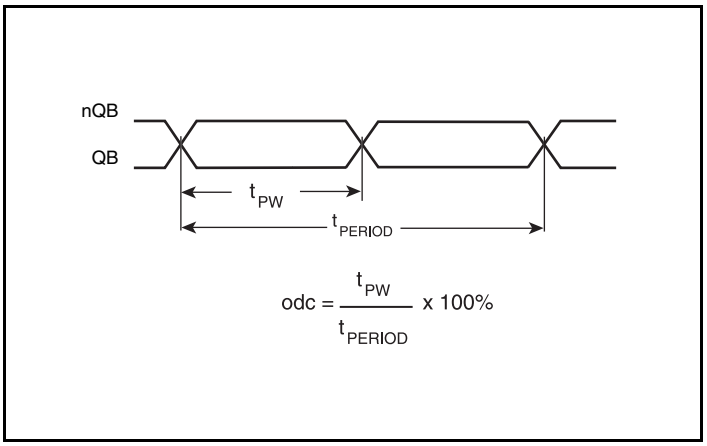
3.3V LVPECL Output Load AC Test Circuit



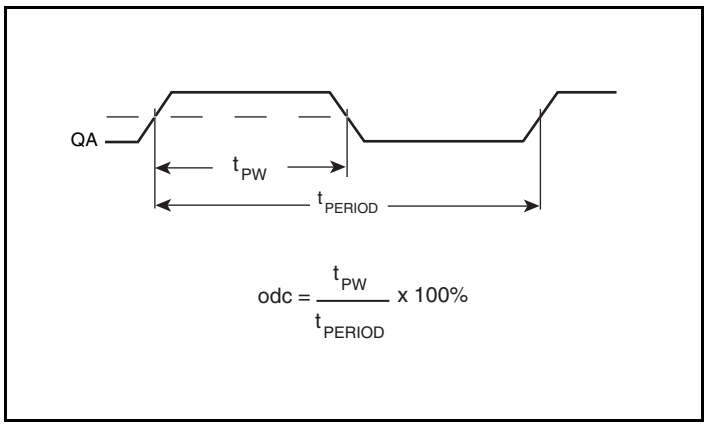
3.3V LVCMOS Output Load AC Test Circuit



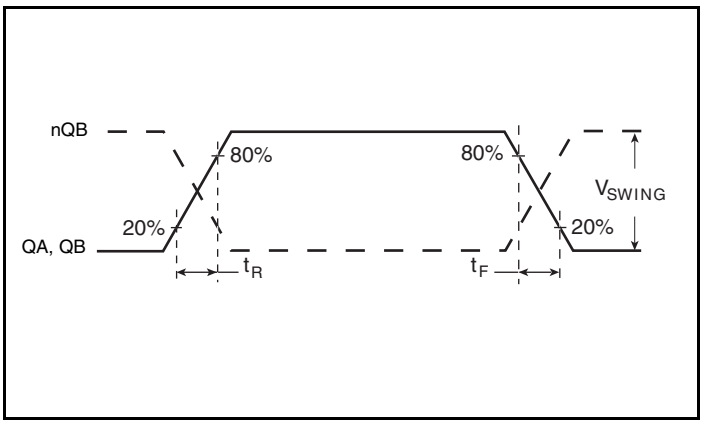
RMS Phase Jitter



LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

The unused LVCMOS output can be left floating. There should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

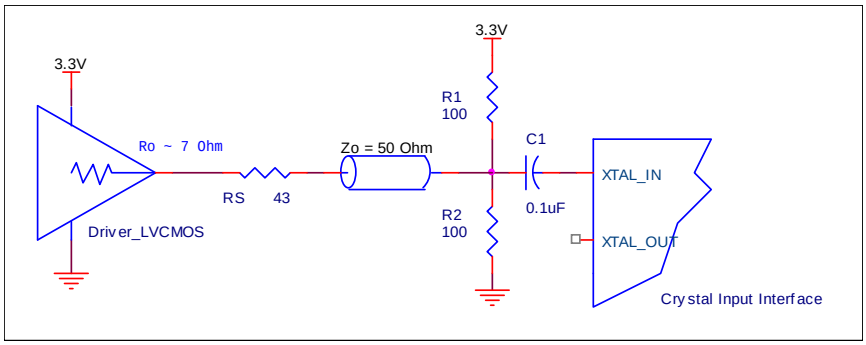


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

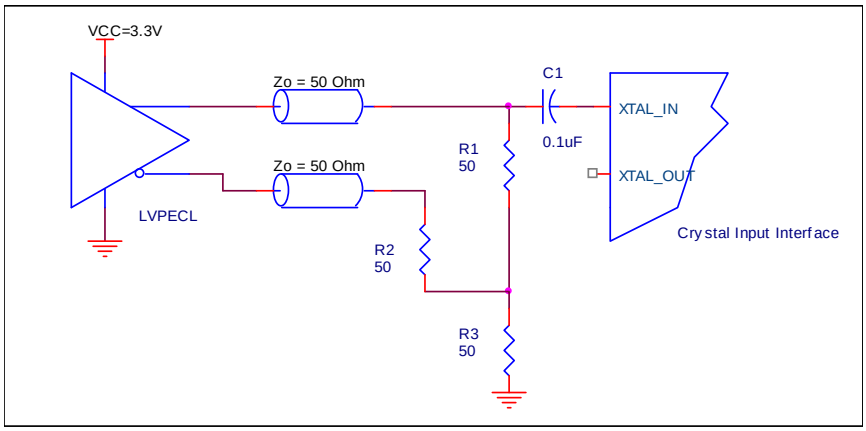


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

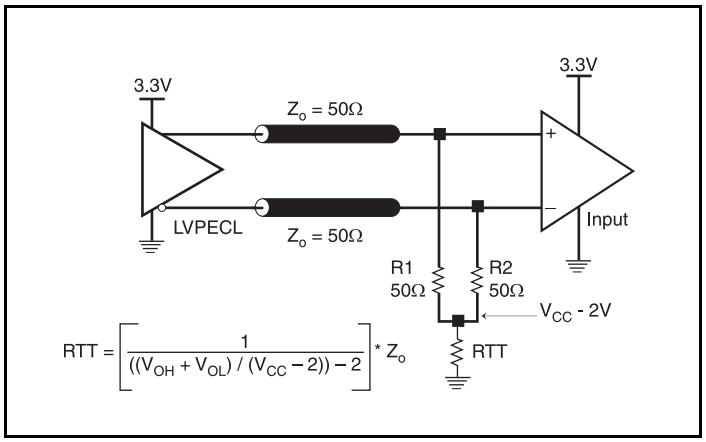


Figure 2A. 3.3V LVPECL Output Termination

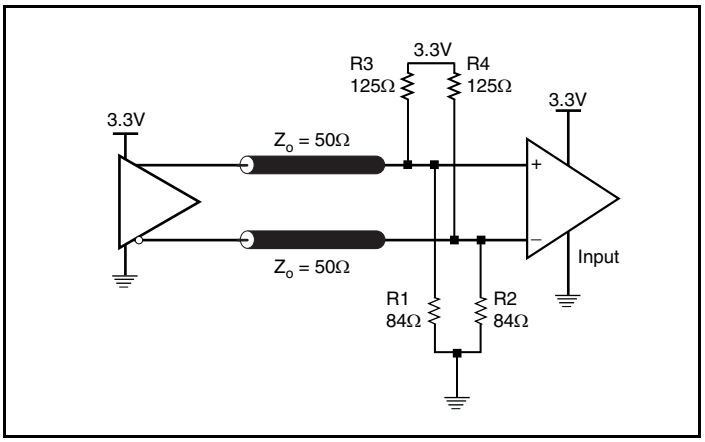


Figure 2B. 3.3V LVPECL Output Termination

Schematic Example

Figure 3 shows an example of 843N252-45 application schematic. In this example, the device is operated at $V_{CC} = V_{CCA} = V_{CCOA} = 3.3V$. If the12pF parallel resonant 25MHz crystal is used; the load capacitance C1 = 5pF and C2 = 5pF are recommended for frequency accuracy. If the 18pF parallel resonant 25MHz crystal is used; the load capacitance C1 = 15pF and C2 = 15pF are recommended. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 843N252-45 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

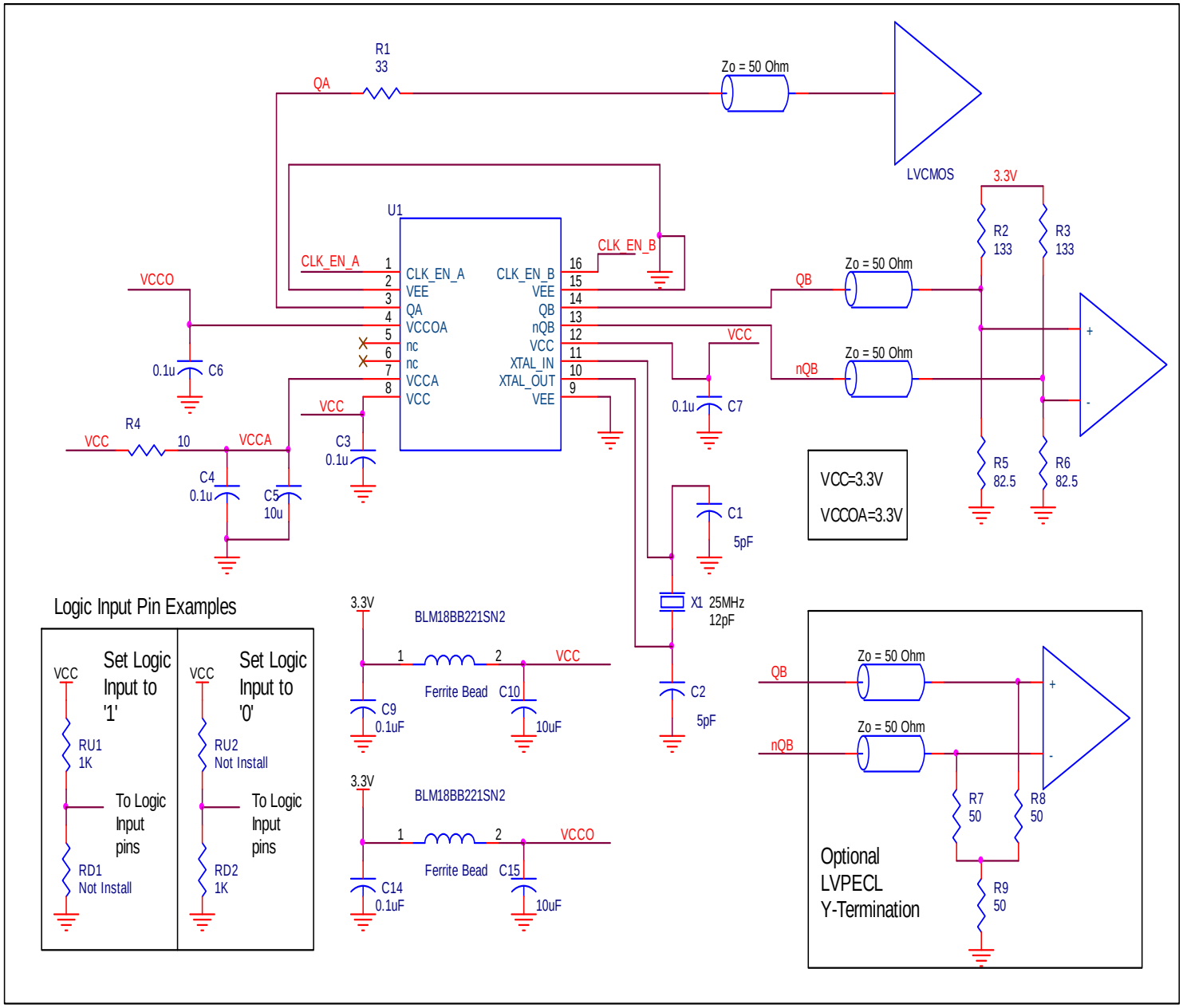


Figure 3. 843N252-45 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843N252-45.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843N252-45 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Core and LVPECL Output Power Dissipation

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 124mA = **429.66mW**
- Power (LVPECL) = **33.75mW/Loaded Output pair**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{CCOA}/2$
  Output Current $I_{OUT} = V_{CCOA\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 15Ω)] = **26.65mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 15Ω * $(26.65mA)^2$ = **10.65mW per output**
- **Dynamic Power Dissipation at 125MHz**
  Power $(125MHz) = C_{PD}$ * Frequency * $(V_{CCOA})^2$ = 7pF * 125MHz * $(3.465V)^2$ = **10.51mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (LVPECL) + Power (R_{OUT}) + Power (125MHz)
  = 429.66mW + 33.75mW + 10.65mW + 10.51mW
  = 484.57mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 94.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.485W * 94.8°C/W = 116°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16 Lead TSSOP Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	94.8°C/W	90.4°C/W	88.3°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4.*

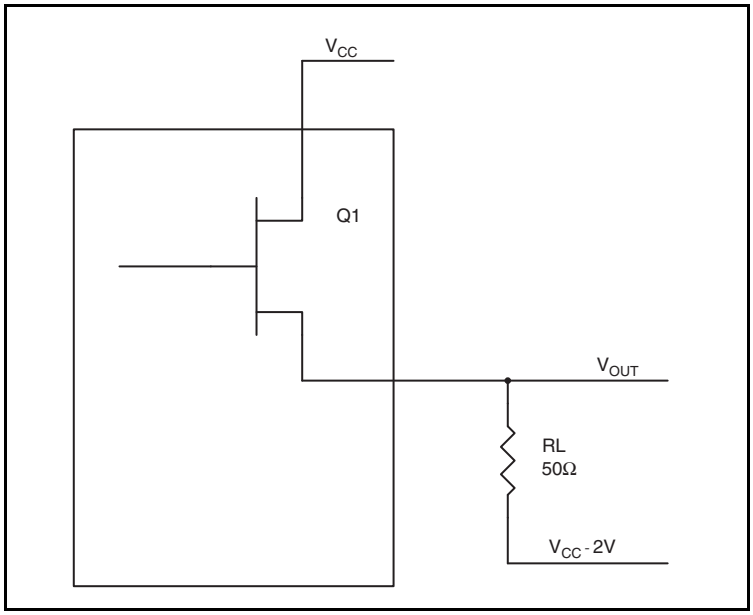


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.75V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.5V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.5V}$
-

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX})$
$= [(2V – 0.75V)/50\Omega] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX})$
$= [(2V – 1.5V)/50\Omega] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.75mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	94.8°C/W	90.4°C/W	88.3°C/W

Transistor Count

The transistor count for 843N252-45 is: 2039

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

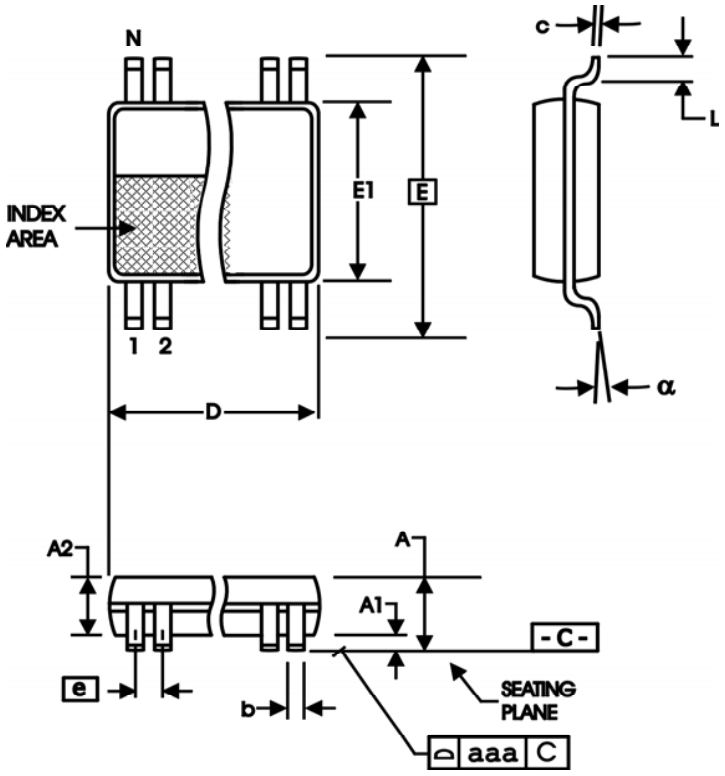


Table 9. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843N252GG-45LF	N252G45L	“Lead-Free” 16 Lead TSSOP	Tube	0°C to 70°C
843N252GG-45LFT	N252G45L	“Lead-Free” 16 Lead TSSOP	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		3	Supply Voltage, $V_{CC.}$ Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03.	6/10/11
A			Removed ICS from the part number where needed. Ordering information - Removed quantity from tape and reel. Deleted LF note below table. Updated data sheet header and footer.	4/20/16

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