GENERAL DESCRIPTION

The ICS8440259D-45 is a 9 output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, the device will generate both 156.25MHz, 125MHz and 3.90625MHz clocks with mixed LVDS and LVCMOS/LVTTL output levels. The ICS8440259D-45 uses IDT’s 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440259D-45 is packaged in a small, 5mm x 5mm VFQFN package that is optimum for applications with space limitations.

FEATURES

- One differential LVDS output at 156.25MHz or 125MHz
- Four differential LVDS outputs at 125MHz
- Three LVCMOS/LVTTL single-ended outputs at 125MHz
- One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- VCO range: 510MHz - 650MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.34ps (typical), LVDS output
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.31ps (typical), LVDS output
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

PIN ASSIGNMENT

IC8440259D-45 32-Lead VFQFN 5mm x 5mm x 0.925mm package body K Package Top View

BLOCK DIAGRAM

[Diagram showing the block diagram of the synthesizer, including the reference clock (REF_CLK), phase detector (Phase Detector), voltage-controlled oscillator (VCO), and output buffers (Q0 to Q8).]

[Diagram showing the pin assignment with numbers and corresponding functions.]
# Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>Q0, nQ0</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>3, 9, 15, 17, 21, 32</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>4, 5</td>
<td>Q1, nQ1</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>6, 12</td>
<td>V_{DD, LVDS}</td>
<td>Power</td>
<td>Output supply pins for Qx/nQx LVDS outputs.</td>
</tr>
<tr>
<td>7, 8</td>
<td>Q2, nQ2</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>10, 11</td>
<td>Q3, nQ3</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>13, 14</td>
<td>Q4, nQ4</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>16, 27</td>
<td>V_{DD}</td>
<td>Power</td>
<td>Core supply pins.</td>
</tr>
<tr>
<td>18, 20, 22, 24</td>
<td>Q5, Q6, Q7, Q8</td>
<td>Output</td>
<td>Single-ended clock outputs. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>19, 23</td>
<td>V_{DD, LVCMOS}</td>
<td>Power</td>
<td>Output supply pins for Q5:Q8 LVCMOS outputs.</td>
</tr>
<tr>
<td>25</td>
<td>V_{DD}</td>
<td>Power</td>
<td>Analog supply pin.</td>
</tr>
<tr>
<td>26</td>
<td>nPLL_BYPASS</td>
<td>Input</td>
<td>Pullup Input select and PLL bypass control pin. See Table 3B.</td>
</tr>
<tr>
<td>28</td>
<td>F_SEL</td>
<td>Input</td>
<td>Pulldown Frequency select pin. See Table 3A.</td>
</tr>
<tr>
<td>29</td>
<td>REF_CLK</td>
<td>Input</td>
<td>Pulldown Single-ended LVCMOS/LVTTL reference clock input.</td>
</tr>
<tr>
<td>30, 31</td>
<td>XTAL_IN, XTAL_OUT</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.</td>
</tr>
</tbody>
</table>

**NOTE:** Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

# Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{IN}</td>
<td>Input Capacitance</td>
<td>V_{DD}, V_{DD, LVCMOS} = 3.465V</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>C_{PD}</td>
<td>Power Dissipation Capacitance</td>
<td>V_{DD}, V_{DD, LVCMOS} = 3.465V</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>pF</td>
</tr>
<tr>
<td>R_{PULLDOWN}</td>
<td>Input Pulldown Resistor</td>
<td>Q5:Q8</td>
<td>51</td>
<td>51</td>
<td>51</td>
<td>kΩ</td>
</tr>
<tr>
<td>R_{OUT}</td>
<td>Output Impedance</td>
<td>Q5:Q8</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>Ω</td>
</tr>
</tbody>
</table>

# Table 3A. Frequency Select Function Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output Divider</th>
<th>Q0/n0 Q0 Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5</td>
<td>125MHz (default)</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>156.25MHz</td>
</tr>
</tbody>
</table>

# Table 3B. PLL Bypass and Input Select Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>PLL Bypass</th>
<th>Input Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>nPLL_BYPASS</td>
<td>PLL Bypassed</td>
<td>REF_CLK</td>
</tr>
<tr>
<td>0</td>
<td>PLL Enabled</td>
<td>XTAL_IN/XTAL_OUT (default)</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings**

Supply Voltage, $V_{dd}$ 4.6V

Inputs, $V_i$ -0.5V to $V_{dd} + 0.5V$

Outputs, $I_o$ (LVCMOS) -0.5V to $V_{dd,LVCMOS} + 0.5V$

Outputs, $I_o$ (LVDS)

- Continuous Current 10mA
- Surge Current 15mA

Operating Temperature Range, $T_A$ -40°C to +85°C

Storage Temperature, $T_{STG}$ -65°C to 150°C

Package Thermal Impedance, $\theta_{JA}$ 37°C/W (0 mps)

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. Power Supply DC Characteristics, $V_{dd} = V_{dd,LVCMOS} = V_{dd,LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO 70°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>Analog Supply Voltage</td>
<td>$V_{dd} - 0.35$</td>
<td>3.3</td>
<td>$V_{dd}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO,LVCMOS}$, $V_{DDO,LVDS}$</td>
<td>Output Supply Voltage</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{dd}$</td>
<td>Power Supply Current</td>
<td></td>
<td>118</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDA}$</td>
<td>Analog Supply Current</td>
<td></td>
<td>35</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO,LVCMOS}$</td>
<td>LVCMS Output Supply Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO,LVDS}$</td>
<td>LVDS Output Supply Current</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**TABLE 4B. LVCMS/LVTTL DC Characteristics, $T_A = 0°C$ TO 70°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_H$</td>
<td>Input High Voltage</td>
<td>REF_CLK (PD)</td>
<td>2</td>
<td>$V_{dd} + 0.3$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_L$</td>
<td>Input Low Voltage</td>
<td>REF_CLK (PD)</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_H$</td>
<td>Input High Current</td>
<td>REF_CLK (PD)</td>
<td>150</td>
<td>5</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_L$</td>
<td>Input Low Current</td>
<td>REF_CLK (PD)</td>
<td>-5</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>Q5:Q8</td>
<td>$I_{OH} = -12mA$</td>
<td>2.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>Q5:Q8</td>
<td>$I_{OL} = 12mA$</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTE 1:** Outputs terminated with 50Ω to $V_{dd,LVCMOS}/2$. See Parameter Measurement Information, Output Load Test Circuit diagram.
# Table 4C. LVDS DC Characteristics, \( V_{DD} = V_{DDO_LVDS} = 3.3V \pm 5\% \), \( TA = 0°C \) to 70°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} )</td>
<td>Differential Output Voltage</td>
<td></td>
<td>300</td>
<td>400</td>
<td>545</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{DD} )</td>
<td>( V_{DD} ) Magnitude Change</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Offset Voltage</td>
<td></td>
<td>1.25</td>
<td>1.35</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>( \Delta V_{OS} )</td>
<td>( V_{OS} ) Magnitude Change</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

# Table 5. Crystal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE: Characterized using an 18pF parallel resonant crystal.

# Table 6. AC Characteristics, \( V_{DD} = V_{DDO_LVCMOS} = V_{DDO_LVDS} = 3.3V \pm 5\% \), \( TA = 0°C \) to 70°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{out} )</td>
<td>Output Frequency</td>
<td>Q0/nQ0:Q4/nQ4</td>
<td></td>
<td>125</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q5:Q7</td>
<td></td>
<td>125</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q8</td>
<td></td>
<td>3.90625</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0/nQ0</td>
<td></td>
<td>156.25</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q(1:4)/nQ[1:4]</td>
<td></td>
<td>125</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{jit})</td>
<td>RMS Phase Jitter (Random); NOTE 1</td>
<td>Q(0:4)/nQ[0:4]</td>
<td>125MHz, (1.875MHz - 20MHz)</td>
<td>0.34</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0/nQ0</td>
<td>156.25MHz, (1.875MHz - 20MHz)</td>
<td>0.31</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q5:Q7</td>
<td>125MHz, (1.875MHz - 20MHz)</td>
<td>0.48</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{r} / t_{f} )</td>
<td>Output Rise/Fall Time</td>
<td>Q(0:4)/nQ[0:4]</td>
<td>PLL Mode, 125MHz, 30% to 70%</td>
<td>1.00E-10</td>
<td>1.02E-09</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q(0:4)/nQ[0:4]</td>
<td>PLL Mode, 125MHz, 20% to 80%</td>
<td>1.50E-10</td>
<td>5.50E-10</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0/nQ0</td>
<td>PLL Mode, 156.25MHz, 20% to 80%</td>
<td>2.50E-10</td>
<td>3.75E-10</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q5:Q7</td>
<td>PLL Mode, 125MHz, 20% to 80%</td>
<td>4.00E-10</td>
<td>1.15E-09</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q8 (NOTE 2)</td>
<td>3.90625MHz, 20% to 80%</td>
<td>6.50E-10</td>
<td>1.35E-09</td>
<td>s</td>
</tr>
<tr>
<td>( odc )</td>
<td>Output Duty Cycle, PLL Mode</td>
<td>Q(0:4)/nQ[0:4]</td>
<td>125MHz</td>
<td>47</td>
<td>53</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0/nQ0</td>
<td>156.25MHz</td>
<td>48</td>
<td>52</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q5:Q7</td>
<td>125MHz</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q8</td>
<td>3.90625MHz</td>
<td>49</td>
<td>51</td>
<td>%</td>
</tr>
<tr>
<td>( odc )</td>
<td>Output Duty Cycle, BYPASS Mode</td>
<td>Q(0:4)/nQ[0:4]</td>
<td>125MHz</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0/nQ0</td>
<td>156.25MHz</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q5:Q7</td>
<td>125MHz</td>
<td>45</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q8</td>
<td>3.90625MHz</td>
<td>49</td>
<td>51</td>
<td>%</td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 fpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Please refer to the Phase Noise Plots.

NOTE 2: Output loaded with 100Ω differential and 15pF loads.
TYPICAL PHASE NOISE AT 125MHz (LVDS @ 3.3V)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

OFFSET FREQUENCY (Hz)

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**Typical Phase Noise at 156.25MHz (LVDS @ 3.3V)**

![Phase Noise Graph]

- **Carrier**: 156.249632 MHz
- **Noise**: -8.376 dBm
- **X**: Start 1.875 MHz, Stop 20 MHz, Center 10.9375 MHz, Span 18.125 MHz
- **Analysis Range X**: Band Marker
- **Analysis Range Y**: Band Marker
- **Integ Noise**: -73.4152 dBc / 17.8 MHz
- **RMS Noise**: 301.825 μrad
- **17.2933 mdeg**
- **RMS Jitter**: 307.437 fs
- **Residual FM**: 2.87605 kHz
Typical Phase Noise at 125MHz (LVCMOS @ 3.3V)

Phase Noise 10.00dB/Ref -20.00dBc/Hz

Offset Frequency (Hz)

Noise Power dBc/Hz

Carrier 124.999662 MHz 6.309 dBm

>1kHz: -119.2740 dBc/Hz
X kHz: Start 1.875 MHz
Stop 20 MHz
Center 10.9375 MHz
Span 18.125 MHz

Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -71.4209 dBc / 17.8 MHz

RMS Noise: 379.726 μrad
21.7567 mdeg

RMS Jitter: 483.484 fscc
Residual FM: 2.63173 kHz
**Parameter Measurement Information**

### 3.3V LVDS Output Load AC Test Circuit

![Diagram of 3.3V LVDS Output Load AC Test Circuit]

- **3.3V±5% Power Supply**
- **VDD, VDDO_LVDS**
- **VDDA**
- **10Ω**
- **Z = 50Ω**
- **VOD**

### 3.3V LVDS Output Load AC Test Circuit with 18pF

![Diagram of 3.3V LVDS Output Load AC Test Circuit with 18pF]

- **1.65V±5%**
- **VDD, VDDO_LVCMOS**
- **1.65V±5%**
- **-1.65V±5%**
- **10Ω**
- **Z = 50Ω**
- **VOD**

### 3.3V LVCMOS Output Load AC Test Circuit

- **nQ0:nQ4**
- **Q0:Q4**
- **VOD**
- **tR**
- **tF**

### RMS Phase Jitter

![Diagram of RMS Phase Jitter]

- **Phase Noise Plot**
- **Noise Power**
- **Phase Noise Mask**
- **Offset Frequency**
- **f₁**
- **f₂**

- **RMS Jitter = \sqrt{\text{Area Under the Masked Phase Noise Plot}}**

### LVDS Output Rise/Fall Time

- **nQ0:nQ4**
- **Q0:Q4**
- **80%**
- **20%**
- **VOD**
- **tR**
- **tF**

- **70%**
- **30%**

---

**ICS8440259D-45**

**FEMTOCLOCK™ CRYSTAL/LVCMOS-TO-LVDS/ LVCMOS FREQUENCY SYNTHESIZER**

---

**IDT™ / ICS™ LVDS/LVCMOS FREQUENCY SYNTHESIZER**

8  

**ICS8440259DK-45 REV.A FEBRUARY 26, 2009**
PARAMETER MEASUREMENT INFORMATION, CONTINUED

LVCMOS OUTPUT RISE/FALL TIME

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP
APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8440259D-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. \( V_{DD} \), \( V_{DDA} \), \( V_{DDO\_LVDS} \) and \( V_{DDO\_LVCMOS} \) should be individually connected to the power supply plane through vias, and 0.01\( \mu \)F bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic \( V_{DD} \) pin and also shows that \( V_{DDA} \) requires that an additional 10\( \Omega \) resistor along with a 10\( \mu \)F bypass capacitor be connected to the \( V_{DDA} \) pin.

![Figure 1. Power Supply Filtering](image)

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1k\( \Omega \) resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k\( \Omega \) resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS
All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1k\( \Omega \) resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS
All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUTS
All unused LVDS output pairs can be either left floating or terminated with 100\( \Omega \) across. If they are left floating, there should be no trace attached.
**CRYSTAL INPUT INTERFACE**

The ICS8440259D-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in Figure 2 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

![Figure 2. Crystal Input Interface](image)

**LVCMOS TO XTAL INTERFACE**

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in Figure 3. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

![Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface](image)
3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 4. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 5. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.
POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8440259D-45. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840259D-45 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{PP} = 3.3V + 5\% = 3.465V$, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = $V_{DD\_{\text{MAX}}} \times (I_{DD} + I_{DC\_LVDS} + I_{DDA}) = 3.465V \times (118mA + 160mA + 35mA) = 1084.545mW$

LVCMOS Output Power Dissipation

- Power (LVCMOS, no-load) = $V_{DD\_{\text{MAX}}} \times I_{DC\_LVCMOS} = 3.465V \times 10mA = 34.65mW$
- Output Impedance $R_{\text{OUT}}$, Power Dissipation due to Loading 50Ω to $V_{DO}/2$
  - Output Current $I_{\text{OUT}} = \frac{V_{DD\_\text{MAX}}}{2 \times (50\Omega + R_{\text{OUT}})} = \frac{3.465V}{2 \times (50\Omega + 25\Omega)} = 23.1mA$
  - Power Dissipation on the $R_{\text{OUT}}$ per LVCMOS output
    - Power ($R_{\text{OUT}}$) = $R_{\text{OUT}} \times (I_{\text{OUT}})^2 = 25\Omega \times (23.1mA)^2 = 13.3mW\text{ per output}$
- Total Power Dissipation on the $R_{\text{OUT}}$
  - Total Power ($R_{\text{OUT}}$) = 13.3mW \times 4 = 53.2mW
- Dynamic Power Dissipation at 125MHz
  - Power (125MHz) = $C_{PD} \times \text{Frequency} \times (V_{DD\_\text{MAX}})^2 = 15pF \times 125MHz \times (3.465V)^2 = 22.5mW\text{ per output}$
  - Total Power (125MHz) = 22.5mW \times 3 = 67.5mW
- Dynamic Power Dissipation at 3.9MHz
  - Power (3.9MHz) = $C_{PD} \times \text{frequency} \times (V_{DD\_\text{MAX}})^2 = 15pF \times 3.90625MHz \times (3.465V)^2 = 0.7mW\text{ per output}$

Total Power Dissipation

- Total Power
  - = Power (core, LVDS) + Power (LVCMOS-no load) + Total Power ($R_{\text{OUT}}$) + Total Power (125MHz) + Total Power (3.9MHz)
  - = 1084.545mW + 34.65mW + 53.2mW + 67.5mW + 0.7mW
  - = 1240.595mW
2. Junction Temperature.

Junction temperature, $T_J$, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for $T_J$ is as follows: $T_J = \theta_{JA} \times P_{d_{total}} + T_A$

$T_J = $ Junction Temperature  

$\theta_{JA} = $ Junction-to-Ambient Thermal Resistance  

$P_{d_{total}} = $ Total Device Power Dissipation (example calculation is in section 1 above)  

$T_A = $ Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7.

Therefore, $T_J$ for an ambient temperature of 70°C with all outputs switching is:

$$70°C + 1.241W \times 37°C/W = 115.9°C.$$  

This is below the limit of 125°C.

This calculation is only an example. $T_J$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

| Table 7. Thermal Resistance $\theta_{JA}$ for 32-Lead VFQFN, Forced Convection |
|---------------------------------|-----|-----|-----|
| $\theta_{JA}$ vs. Air Flow (Meters per Second) | 0   | 1   | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.0°C/W | 32.4°C/W | 29.0°C/W |
## Reliability Information

### Table 8. $\theta_{JA}$ vs. Air Flow Table for 32 Lead VFQFN

<table>
<thead>
<tr>
<th>Air Flow (Meters per Second)</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>37.0°C/W</td>
<td>32.4°C/W</td>
<td>29.0°C/W</td>
</tr>
</tbody>
</table>

## Transistor Count

The transistor count for ICS8440259D-45 is: 2975
NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page.

### Table 9. Package Dimensions

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>JEDEC VARIATION</th>
<th>VHHD-2</th>
<th>ALL DIMENSIONS IN MILLIMETERS</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MINIMUM</td>
<td>NOMINAL</td>
</tr>
<tr>
<td>N</td>
<td></td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>0.80</td>
<td>--</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>A3</td>
<td></td>
<td>0.25 Ref.</td>
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</tr>
<tr>
<td>b</td>
<td></td>
<td>0.18</td>
<td>0.25</td>
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<tr>
<td>N_b</td>
<td></td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>N_e</td>
<td></td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>D</td>
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<td></td>
<td>5.00 BASIC</td>
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<tr>
<td>D2</td>
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<td>1.25</td>
<td>2.25</td>
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<tr>
<td>E</td>
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<td>5.00 BASIC</td>
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</tr>
<tr>
<td>E2</td>
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<tr>
<td>e</td>
<td></td>
<td></td>
<td>0.50 BASIC</td>
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<tr>
<td>L</td>
<td></td>
<td>0.30</td>
<td>0.40</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MO-220
TABLE 10. ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8440259DK-45LF</td>
<td>ICS0259D45L</td>
<td>32 Lead &quot;Lead-Free&quot; VFQFN</td>
<td>Tray</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>8440259DK-45LFT</td>
<td>ICS0259D45L</td>
<td>32 Lead &quot;Lead-Free&quot; VFQFN</td>
<td>1000 Tape &amp; Reel</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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