Description
The 853S202 is a 12:2 Differential-to-LVPECL Clock Multiplexer which can operate up to 3GHz. The 853S202 has twelve selectable differential clock inputs, any of which can be independently routed to either of the two LVDS outputs. The CLKx, nCLKx input pairs can accept LVPECL or LVDS levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits.

Features
- High speed 12.2 differential multiplexer
- Two differential 3.3V or 2.5V LVPECL outputs
- Twelve selectable differential clock or data inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS
- Maximum output frequency: 3GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nCLKx input
- Propagation delay: 1.15ns (maximum)
- Input skew: 150ps (maximum)
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.114ps (typical) @ 155.52MHz, 3.3V
- Full 3.3V or 2.5V operating supply mode
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignments

Block Diagram
### Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CLK2</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>2</td>
<td>nCLK2</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>3, 4, 9, 10</td>
<td>SELA_0, SELA_1, SELA_2, SELA_3</td>
<td>Input</td>
<td>Pulldown Clock select pins for Bank A output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3B.</td>
</tr>
<tr>
<td>5, 18, 32, 43</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Power</td>
<td>Power supply pins.</td>
</tr>
<tr>
<td>6, 7</td>
<td>QA, nQA</td>
<td>Output</td>
<td>Clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>8, 15, 22, 29, 39, 46</td>
<td>V&lt;sub&gt;EE&lt;/sub&gt;</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>11</td>
<td>CLK3</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>12</td>
<td>nCLK3</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>13</td>
<td>nCLK4</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>14</td>
<td>CLK4</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>16</td>
<td>nCLK5</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>17</td>
<td>CLK5</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>19</td>
<td>OEA</td>
<td>Input</td>
<td>Pullup Output enable pin. Controls enabling and disabling of QA, nQA output pair. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>20</td>
<td>CLK6</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>21</td>
<td>nCLK6</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>23</td>
<td>CLK7</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>24</td>
<td>nCLK7</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>25</td>
<td>nCLK8</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>26</td>
<td>CLK8</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>27, 28, 33, 34</td>
<td>SELB_3, SELB_2, SELB_1, SELB_0</td>
<td>Input</td>
<td>Pulldown Clock select pins for Bank B output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3C.</td>
</tr>
<tr>
<td>30, 31</td>
<td>nQB, QB</td>
<td>Output</td>
<td>Clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>35</td>
<td>nCLK9</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>36</td>
<td>CLK9</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
<tr>
<td>37</td>
<td>nCLK10</td>
<td>Input</td>
<td>Pullup/Pulldown Inverting differential clock input. V&lt;sub&gt;CC&lt;/sub&gt;/2 default when left floating.</td>
</tr>
<tr>
<td>38</td>
<td>CLK10</td>
<td>Input</td>
<td>Pulldown Non-inverting differential clock input.</td>
</tr>
</tbody>
</table>
Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>nCLK11</td>
<td>Input Pulldown</td>
<td>Inverting differential clock input. ( V_{CC}/2 ) default when left floating.</td>
</tr>
<tr>
<td>41</td>
<td>CLK11</td>
<td>Input Pulldown</td>
<td>Non-inverting differential clock input.</td>
</tr>
<tr>
<td>42</td>
<td>OEB</td>
<td>Input Pullup</td>
<td>Output enable pin. Controls enabling and disabling of QB, nQB output pair.</td>
</tr>
<tr>
<td>44</td>
<td>CLK0</td>
<td>Input Pulldown</td>
<td>Non-inverting differential clock input.</td>
</tr>
<tr>
<td>45</td>
<td>nCLK0</td>
<td>Input Pulldown</td>
<td>Inverting differential clock input. ( V_{CC}/2 ) default when left floating.</td>
</tr>
<tr>
<td>47</td>
<td>CLK1</td>
<td>Input Pulldown</td>
<td>Non-inverting differential clock input.</td>
</tr>
<tr>
<td>48</td>
<td>nCLK1</td>
<td>Input Pulldown</td>
<td>Inverting differential clock input. ( V_{CC}/2 ) default when left floating.</td>
</tr>
</tbody>
</table>

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Capacitance</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R&lt;sub&gt;PULLUP&lt;/sub&gt;</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R&lt;sub&gt;PULLDOWN&lt;/sub&gt;</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

Function Tables

Table 3A. OEA, OEB Control Input Function Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>OEA, OEB</td>
<td>QA, nQA, QB, nQB</td>
</tr>
<tr>
<td>0</td>
<td>Disabled (Logic LOW)</td>
</tr>
<tr>
<td>1</td>
<td>Active (default)</td>
</tr>
</tbody>
</table>
### Table 3B. SEL_A Control Input Function Table

<table>
<thead>
<tr>
<th>SELA_3</th>
<th>SELA_2</th>
<th>SELA_1</th>
<th>SELA_0</th>
<th>Input Selected to QA, nQA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CLK0, nCLK0 (default)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>CLK1, nCLK1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>CLK2, nCLK2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CLK3, nCLK3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>CLK4, nCLK4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>CLK5, nCLK5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>CLK6, nCLK6</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CLK7, nCLK7</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CLK8, nCLK8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>CLK9, nCLK9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>CLK10, nCLK10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CLK11, nCLK11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Output at logic LOW</td>
</tr>
</tbody>
</table>

### Table 3C. SEL_B Control Input Function Table

<table>
<thead>
<tr>
<th>SELB_3</th>
<th>SELB_2</th>
<th>SELB_1</th>
<th>SELB_0</th>
<th>Input Selected to QA, nQA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CLK0, nCLK0 (default)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>CLK1, nCLK1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>CLK2, nCLK2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CLK3, nCLK3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>CLK4, nCLK4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>CLK5, nCLK5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>CLK6, nCLK6</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CLK7, nCLK7</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>CLK8, nCLK8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>CLK9, nCLK9</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>CLK10, nCLK10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>CLK11, nCLK11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Output at logic LOW</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Output at logic LOW</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{CC}$</td>
<td>4.6V</td>
</tr>
<tr>
<td>Inputs, $V_i$</td>
<td>-0.5V to $V_{CC} + 0.5V$</td>
</tr>
<tr>
<td>Outputs, $I_O$</td>
<td></td>
</tr>
<tr>
<td>Continuous Current</td>
<td></td>
</tr>
<tr>
<td>Surge Current</td>
<td>50mA</td>
</tr>
<tr>
<td></td>
<td>100mA</td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>70.2°C/W (0 lpm)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Characteristic Tables

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>No Load</td>
<td>85</td>
<td>95</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4B. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>No Load</td>
<td>80</td>
<td>88</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{CC} = 3.3V$</td>
<td>2.2</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.5V$</td>
<td>1.7</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{CC} = 3.3V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.5V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$V_{CC} = V_{IN} = 3.465V$ or 2.625V</td>
<td>150</td>
<td></td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SELA[3:0], SELB[3:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OEA, OEB</td>
<td>$V_{CC} = V_{IN} = 3.465V$ or 2.625V</td>
<td>5</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{CC} = 3.465V$ or 2.625V, $V_{IN} = 0V$</td>
<td>-5</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SELA[3:0], SELB[3:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OEA, OEB</td>
<td>$V_{CC} = 3.465V$ or 2.625V, $V_{IN} = 0V$</td>
<td>-150</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 4D. Differential DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>CLK[0:11] $V_{CC} = V_{IN} = 3.465V$ or $2.625V$</td>
<td>150</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCLK[0:11] $V_{CC} = V_{IN} = 3.465V$ or $2.625V$</td>
<td>150</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>CLK[0:11] $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$</td>
<td>$-5$</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>nCLK[0:11] $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$</td>
<td>$-150$</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td>Peak-to-Peak Input Voltage;</td>
<td></td>
<td>0.15</td>
<td>1.5</td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{CMR}$</td>
<td>Common Mode Input Voltage: NOTE 1, 2</td>
<td></td>
<td>$V_{EE} + 0.5$</td>
<td></td>
<td>$V_{CC} - 0.85$</td>
<td>$V$</td>
</tr>
</tbody>
</table>

**NOTE 1:** Common mode voltage is defined as $V_{ih}$.
**NOTE 2:** For single ended applications, the maximum input voltage for CLKx, nCLKx is $V_{CC} + 0.3V$.

### Table 4E. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V$, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{CC} - 1.2$</td>
<td></td>
<td>$V_{CC} - 0.8$</td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{CC} - 2.0$</td>
<td></td>
<td>$V_{CC} - 1.7$</td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.6</td>
<td></td>
<td>1.0</td>
<td></td>
<td>$V$</td>
</tr>
</tbody>
</table>

**NOTE 1:** Outputs terminated with $50\Omega$ to $V_{CC} - 2V$. 
# AC Characteristics Table

**Table 5A. AC Characteristics, \( V_{CC} = 3.3V \pm 5\% \), \( T_A = -40^\circ C \) to \( 85^\circ C \)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{OUT} )</td>
<td>Output Frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay, Low to High; NOTE 1</td>
<td></td>
<td>450</td>
<td>600</td>
<td>850</td>
<td>ps</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay, High to Low; NOTE 1</td>
<td></td>
<td>450</td>
<td>600</td>
<td>850</td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(o)} )</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td>14</td>
<td>50</td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(i)} )</td>
<td>Input Skew; NOTE 3</td>
<td></td>
<td></td>
<td>30</td>
<td>150</td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(pp)} )</td>
<td>Part-to-Part Skew; NOTE 3, 4</td>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>ps</td>
</tr>
<tr>
<td>( f_{jit} )</td>
<td>Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5</td>
<td>155.52MHz, Integration Range: 12kHz - 20MHz</td>
<td>0.114</td>
<td>0.152</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>( t_{R} / t_{F} )</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>55</td>
<td></td>
<td>250</td>
<td>ps</td>
</tr>
<tr>
<td>( odc )</td>
<td>Output Duty Cycle; NOTE 6</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>( MUX_{ISOLATION} )</td>
<td>MUX Isolation</td>
<td>( f_{OUT} &lt; 1.2GHz )</td>
<td></td>
<td></td>
<td>75</td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. Note that phase noise may increase slightly with higher operating temperature. However, they will remain in spec as long as the maximum transistor junction temperature is not violated. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from \( V_{CC}/2 \) of the input to \( V_{CC}/2 \) of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at \( V_{CC}/2 \).

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at \( V_{CC}/2 \).

NOTE 5: Driving only one input clock.

NOTE 6: The output duty cycle will depend on the input duty cycle.
Table 5B. AC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{OUT}$</td>
<td>Output Frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Propagation Delay, Low to High; NOTE 1</td>
<td></td>
<td>450</td>
<td>630</td>
<td>875</td>
<td>ps</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Propagation Delay, High to Low; NOTE 1</td>
<td></td>
<td>450</td>
<td>630</td>
<td>875</td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(i)}$</td>
<td>Input Skew; NOTE 3</td>
<td></td>
<td>14</td>
<td>50</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(pp)}$</td>
<td>Part-to-Part Skew; NOTE 3, 4</td>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>ps</td>
</tr>
<tr>
<td>$j_{it}$</td>
<td>Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5</td>
<td>155.52MHz, Integration Range: 12kHz - 20MHz</td>
<td>0.147</td>
<td>0.215</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{R} / t_{F}$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>55</td>
<td>250</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$o_{dc}$</td>
<td>Output Duty Cycle; NOTE 6</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>$MUX_{ISOLATION}$</td>
<td>MUX Isolation</td>
<td>$f_{OUT} &lt; 1.2GHz$</td>
<td>75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. Note that phase noise may increase slightly with higher operating temperature. However, they will remain in spec as long as the maximum transistor junction temperature is not violated. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from $V_{CC}/2$ of the input to $V_{CC}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CC}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{CC}/2$.
NOTE 5: Driving only one input clock.
NOTE 6: The output duty cycle will depend on the input duty cycle.
Additive Phase Jitter (3.3V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the $\text{dBc Phase Noise}$. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a $\text{dBc}$ value, which simply means dBm at a specified offset from the fundamental.

By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using the Rhode & Schwartz SMA100 as the input source.
Additive Phase Jitter (2.5V)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the dBc Phase Noise. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a dBc value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using the Rhode & Schwartz SMA100 as the input source.
Parameter Measurement Information

3.3V Output Load Test Circuit

2.5V Output Load Test Circuit

Differential Input Level

Part-to-Part Skew

Output Skew

Propagation Delay
Parameter Measurement Information, continued

**Output Duty Cycle/Pulse Width/Period**

\[ odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\% \]

**Input Skew**

\[ tsk(i) = |t_{PD1} - t_{PD2}| \]

**Output Rise/Fall Time**
Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs
For applications requiring only one differential input, the unused CLK and nCLK input can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK pin to ground.

LVCMOS Control Pins
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage \( V_1 = V_{CC}/2 \) is generated by the bias resistors \( R_1 \) and \( R_2 \). The bypass capacitor \( C_1 \) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of \( R_1 \) and \( R_2 \) might need to be adjusted to position the \( V_1 \) in the center of the input voltage swing. For example, if the input clock swing is 2.5V and \( V_{CC} = 3.3V \), \( R_1 \) and \( R_2 \) value should be adjusted to set \( V_1 \) at 1.25V. The values below are for when both the single ended swing and \( V_{CC} \) are at the same voltage. This configuration requires that the sum of the output impedance of the driver (\( R_o \)) and the series resistance (\( R_s \)) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, \( R_3 \) and \( R_4 \) in parallel should equal the transmission line impedance. For most 50Ω applications, \( R_3 \) and \( R_4 \) can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however \( V_{IL} \) cannot be less than -0.3V and \( V_{IH} \) cannot be more than \( V_{CC} + 0.3V \). Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

![Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels](image-url)
### 3.3V Differential Clock Input Interface

The CLK / nCLK accepts LVDS, LVPECL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 2A to 2C show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

**Figure 2A.** CLK/nCLK Input Driven by a 3.3V LVPECL Driver

**Figure 2B.** CLK/nCLK Input Driven by a 3.3V LVPECL Driver

**Figure 2C.** CLK/nCLK Input Driven by a 3.3V LVDS Driver
2.5V Differential Clock Input Interface

The CLK / nCLK accepts LVDS, LVPECL and other differential signals. Both \( V_{SWING} \) and \( V_{OH} \) must meet the \( V_{PP} \) and \( V_{CMR} \) input requirements. Figures 3A to 3C show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 3A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

Figure 3B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

Figure 3C. CLK/nCLK Input Driven by a 2.5V LVDS Driver
Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 4A. 3.3V LVPECL Output Termination

Figure 4B. 3.3V LVPECL Output Termination
Termination for 2.5V LVPECL Outputs

*Figure 5A and Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C*.

**Figure 5A. 2.5V LVPECL Driver Termination Example**

**Figure 5B. 2.5V LVPECL Driver Termination Example**

**Figure 5C. 2.5V LVPECL Driver Termination Example**
Power Considerations

This section provides information on power dissipation and junction temperature for the 853S202. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S202 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- **Power (core)$_{\text{MAX}}$** = $V_{CC\_\text{MAX}} \times I_{EE\_\text{MAX}} = 3.465V \times 94mA = 325.71mW$
- **Power (outputs)$_{\text{MAX}}$** = $29.4mW/\text{Loaded Output pair}$
  - If all outputs are loaded, the total power is $2 \times 29.4mW = 58.8mW$

**Total Power** (3.465V, with all outputs switching) = $325.71W + 58.8mW = 384.51mW$

2. Junction Temperature.

Junction temperature, $T_j$, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_j$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for $T_j$ is as follows: $T_j = \theta_{JA} \times P_d\_\text{total} + T_A$

- $T_j$ = Junction Temperature
- $\theta_{JA}$ = Junction-to-Ambient Thermal Resistance
- $P_d\_\text{total}$ = Total Device Power Dissipation (example calculation is in section 1 above)
- $T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{ JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70.2°C/W per Table 6 below.

Therefore, $T_j$ for an ambient temperature of 85°C with all outputs switching is:

$$85°C + 0.385W \times 70.2°C/W = 112°C.$$ This is below the limit of 125°C.

This calculation is only an example. $T_j$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance $\theta_{JA}$ for 48 Lead LQFP, Forced Convection

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>70.2°C/W</td>
<td>60.4°C/W</td>
<td>56.9°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.
The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.
The LVPECL output driver circuit and termination are shown in Figure 4.

![LVPECL Driver Circuit and Termination](image)

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.8V$
  
  \[(V_{CC_MAX} - V_{OH_MAX}) = 0.8V\]

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
  
  \[(V_{CC_MAX} - V_{OL_MAX}) = 1.7V\]

$P_{d_H}$ is power dissipation when the output drives high.
$P_{d_L}$ is the power dissipation when the output drives low.

\[
P_{d_H} = \left[\frac{(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L}{(V_{CC_MAX} - V_{OH_MAX})}\right] \times (V_{CC_MAX} - V_{OH_MAX}) = \left[\frac{2V}{50\Omega}\right] \times 0.8V = 19.20mW
\]

\[
P_{d_L} = \left[\frac{(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L}{(V_{CC_MAX} - V_{OL_MAX})}\right] \times (V_{CC_MAX} - V_{OL_MAX}) = \left[\frac{2V}{50\Omega}\right] \times 1.7V = 10.20mW
\]

Total Power Dissipation per output pair = $P_{d_H} + P_{d_L} = 29.4mW$
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 48 Lead LQFP

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>$\theta_{JA}$ vs. Air Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>70.2°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for 853S202 is: 8,537

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available.

Ordering Information

Table 9. Ordering Information

<table>
<thead>
<tr>
<th>Orderable Part Number</th>
<th>Marking</th>
<th>Package</th>
<th>Carrier Type</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>853S202AYILF</td>
<td>ICS53S202AIL</td>
<td>Lead-Free 7 x 7 mm, 1.4 pitch 48-LQFP</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>853S202AYILFT</td>
<td>ICS53S202AIL</td>
<td>Lead-Free 7 x 7 mm, 1.4 pitch 48-LQFP</td>
<td>Tape and Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 23, 2018</td>
<td>• Updated the maximum values for $t_{PLH}$ and $t_{PHL}$ in Table 5A and Table 5B</td>
</tr>
<tr>
<td></td>
<td>• Updated the package outline drawings; however, no technical changes</td>
</tr>
<tr>
<td></td>
<td>• Completed other minor improvements throughout the document</td>
</tr>
<tr>
<td>October 4, 2016</td>
<td>• Corrected Tape &amp; Reel Orderable Part Number.</td>
</tr>
<tr>
<td></td>
<td>• Deleted “ICS” prefix and “I” suffix from the part number.</td>
</tr>
<tr>
<td></td>
<td>• Updated datasheet header/footer.</td>
</tr>
</tbody>
</table>

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as “IDT”) reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT’s sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT’s products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary. Integrated Device Technology, Inc. All rights reserved.

©2018 Integrated Device Technology, Inc. 20 July 23, 2018
# PR/PRG32

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>JEDEC VARIATION</th>
<th>BBA</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>.05</td>
<td>.10</td>
<td>.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>9.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>7.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>9.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>7.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>3.37</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b1</td>
<td>.35</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>cccc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>dddd</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# PR/PRG48

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>JEDEC VARIATION</th>
<th>BBC</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>.05</td>
<td>.10</td>
<td>.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>9.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>7.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>9.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>7.00 BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>48</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>.17</td>
<td>.22</td>
<td>.27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b1</td>
<td>.17</td>
<td>.20</td>
<td>.23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cccc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>dddd</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5M–1982.
2. Top package may be smaller than bottom package by .15 mm.
3. Dimensions D and E are to be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is .25 millimeter per side. D1 and E1 are maximum body size dimensions, including mold mismatch.
5. Details of pin 1 identifier are optional, but must be located within the zone indicated.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion is .08 millimeter in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Exact shape of each corner is optional.
8. These dimensions apply to the flat section of the lead between .10 and .25 millimeter from the lead tip.
9. All dimensions are in millimeters.
10. This outline conforms to JEDEC Publication MS-026, variations BBA & BBC.

---

**LAND PATTERN DIMENSIONS**

- **MIN** | **MAX**
- P      | 9.80 | 10.00
- P1     | 6.80 | 7.00
- P2     | 5.60 | 5.80
- X      | .40  | .60
- e      | .20  | .25
- N      | 32   | 48

- **MIN** | **MAX**
- P      | 9.80 | 10.00
- P1     | 6.80 | 7.00
- P2     | 5.60 | 5.80
- X      | .40  | .60
- e      | .20  | .25
- N      | 32   | 48