Description

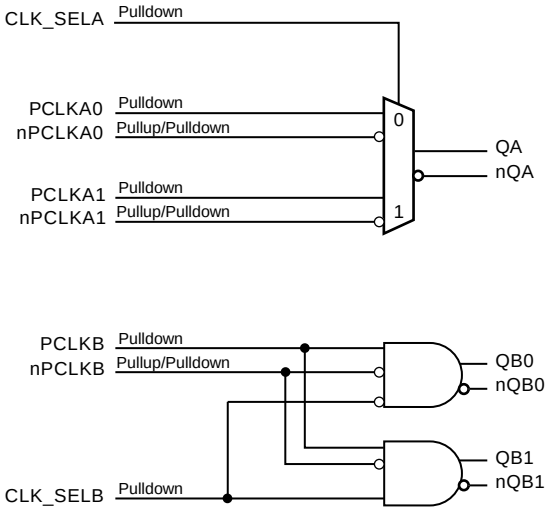
The 855S54 is a dual 2:1 and 1:2 Multiplexer. The 2:1 Multiplexer allows one of two inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device is useful for multiplexing multi-rate Ethernet PHYs which have 100 Mbit and 1 Gbit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. See Application Section for further information.

The 855S54 is optimized for applications requiring very high performance and has a maximum operating frequency of 2.5GHz. The device is packaged in a small, 3 x 3 mm VFQFN package, making it ideal for use on space-constrained boards.

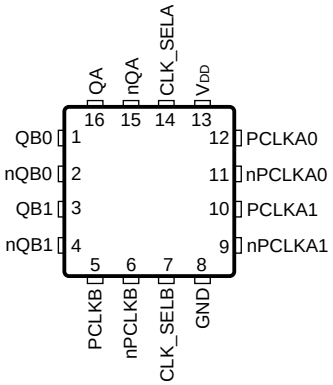
Features

- Three differential LVDS output pairs
- Three differential LVPECL clock input pairs
- PCLKx pair can accept the following differential input levels: LVPECL and LVDS
- Maximum output frequency: 2.5GHz
- Additive phase jitter, RMS: 0.035ps (typical)
- Propagation delay: 450ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



855S54

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVDS interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVDS interface levels.
5	PCLKB	Input	Pulldown	Non-inverting LVPECL differential clock input.
6	nPCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7	CLK_SELB	Input	Pulldown	Clock select pin for QBx outputs. When HIGH, selects QB1, nQB1 outputs. When LOW, selects QB0, nQB0 outputs. See Table 3B. LVCMOS/LVTTL interface levels.
8	GND	Power		Power supply ground.
9	nPCLKA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
10	PCLKA1	Input	Pulldown	Non-inverting LVPECL differential clock input.
11	nPCLKA0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
12	PCLKA0	Input	Pulldown	Non-inverting LVPECL differential clock input.
13	V_{DD}	Power		Positive supply pin.
14	CLK_SELA	Input	Pulldown	Clock select pin for PCLKA inputs. When HIGH, selects PCLKA1/nPCLKA1 inputs. When LOW, selects PCLKA0/nPCLKA0 inputs. See Table 3A. LVCMOS/LVTTL interface levels.
15, 16	nQA, QA	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pullup Resistor			37.5		kΩ
$R_{VDD}/2$	RPullup/Pulldown Resistor			37.5		kΩ

Function Tables

Table 3A. Control Input Function Table, Bank A

Bank A	
Control Input	**Outputs**
CLK_SELA	**QA, nQA**
0 (default)	Selects PCLKA0, nPCLKA0
1	Selects PCLKA1, nPCLKA1

Table 3B. Control Input Function Table, Bank B

Bank B		
Control Input	**Outputs**	
CLK_SELB	**QB0, nQB0**	**QB1, nQB1**
0 (default)	Follows PCLKB input	Logic Low
1	Logic Low	Follows PCLKB input

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	V_{DD} = 2.625V, V_{IN} = 0V	-10			µA

Table 4C. DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IH}	Input High Current	PCLKAx, PCLKB nPCLKx, nPCLKB			150			150			150	µA
I_{IL}	Input Low Current	nPCLKAx, nPCLKB PCLKAx, PCLKB	-150			-150			-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.2	0.15		1.2	0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		1.2		V_{DD}	1.2		V_{DD}	1.2		V_{DD}	V

NOTE 1: V_{IL} should not be less than -0.3V
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OD}	Differential Output Voltage	750	1000	1250	750	1000	1320	750	1000	1370	mV
ΔV_{OD}	V_{OD} Magnitude Change		30	50		30	50		30	50	mV
V_{OUT}	Single-ended Output Voltage Swing	375	500	625	375	500	660	375	500	685	mV
V_{OS}	Offset Voltage	0.82	1.30	1.78	0.85	1.33	1.80	0.90	1.35	1.85	V
ΔV_{OS}	V_{OS} Magnitude Change		10	50		10	50		10	50	mV

NOTE: Refer to Parameter Measurement Information, *2.5V Output Load Test Circuit diagram.*

AC Electrical Characteristics

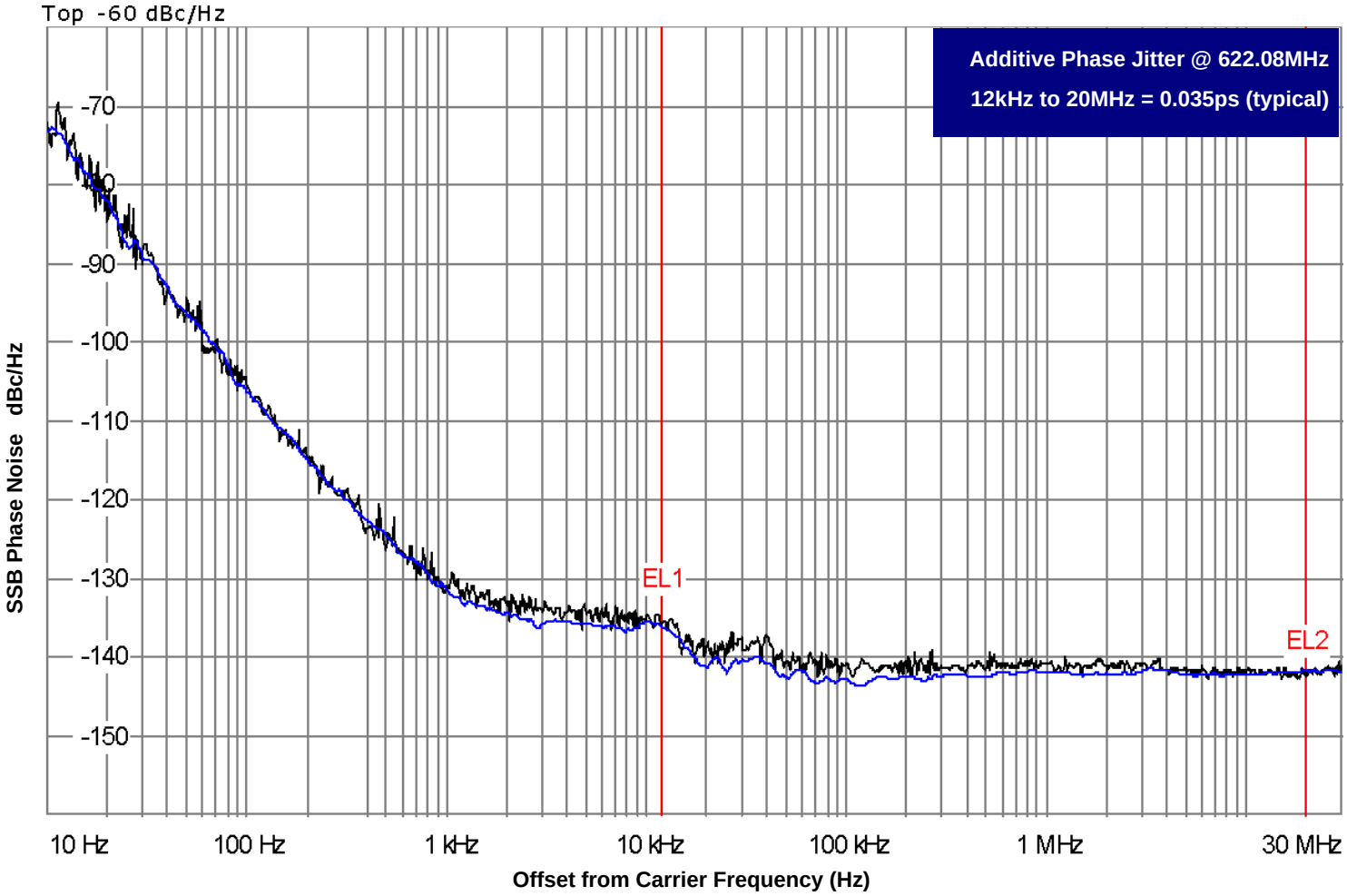
Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		230		450	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2	622.08MHz Integration Range: 12kHz - 20MHz		0.035		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				200	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		260	ps
odc	Output Duty Cycle		44		56	%
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 5	f_{OUT} = 622.08MHz, V_{OUT} = 400mV		65		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at ≤ 1.0GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Measured using clock input at 622.08MHz.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Q/nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

Additive Phase Jitter

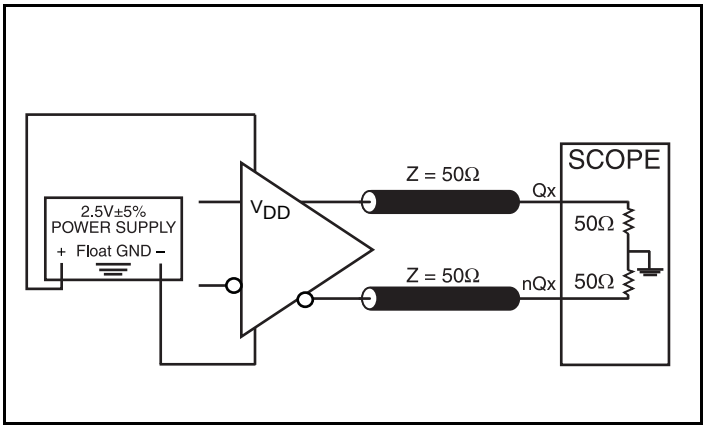
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



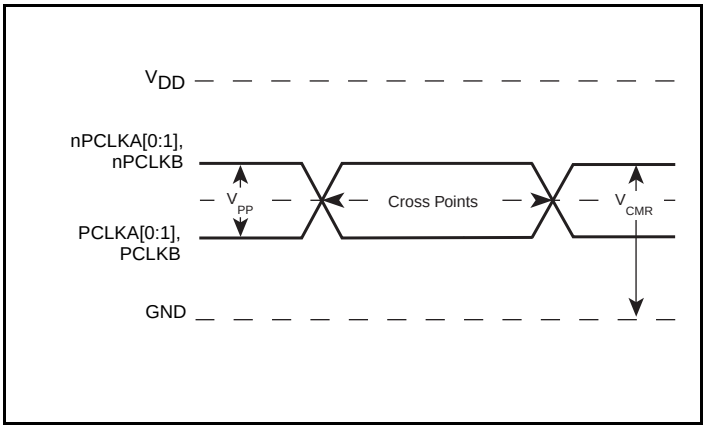
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

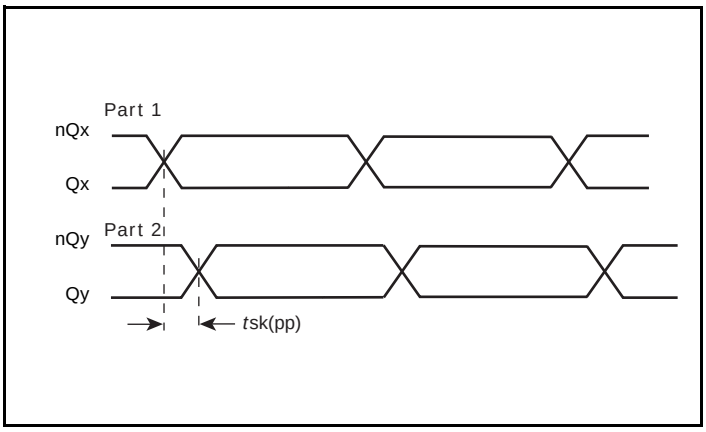
Parameter Measurement Information



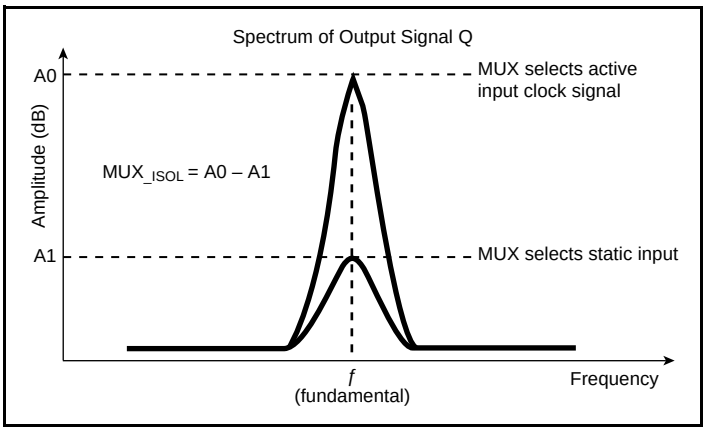
LVDS Output Load AC Test Circuit



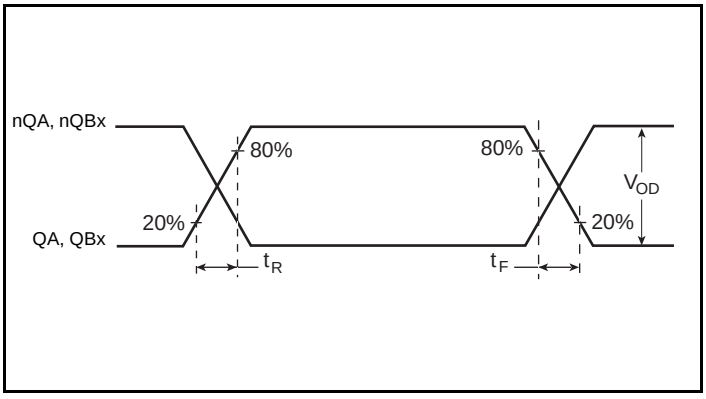
Differential Input Level



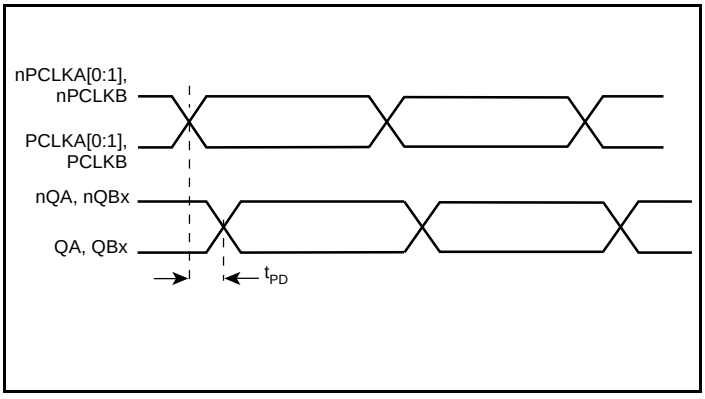
Part-to-Part Skew



MUX Isolation

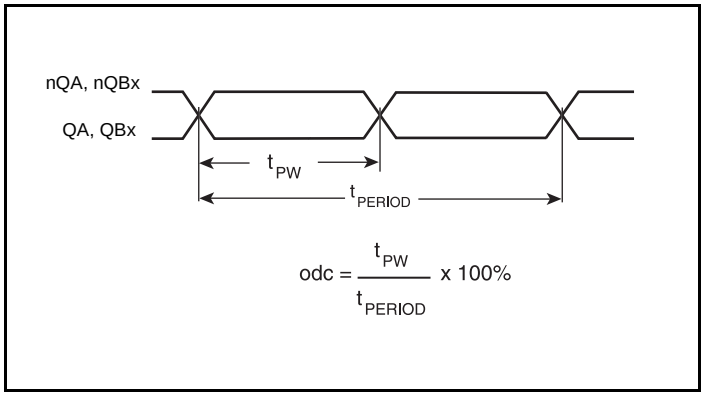


Output Rise/Fall Time

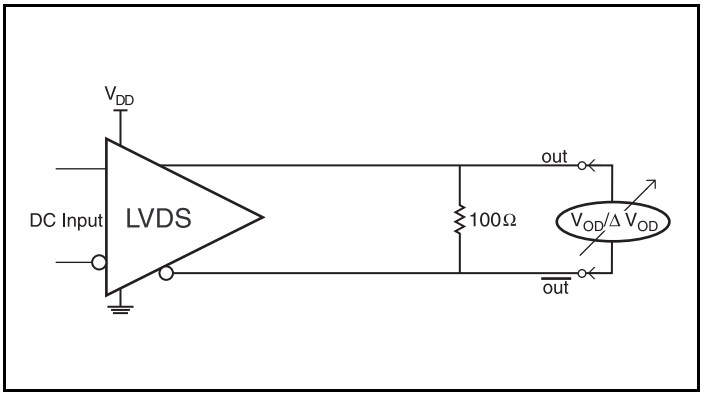


Propagation Delay

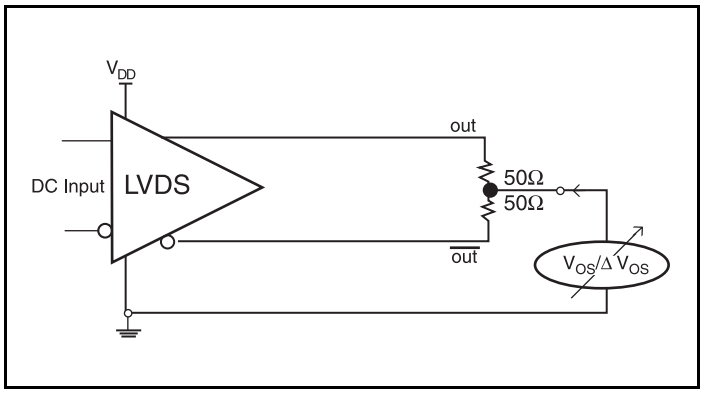
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing.

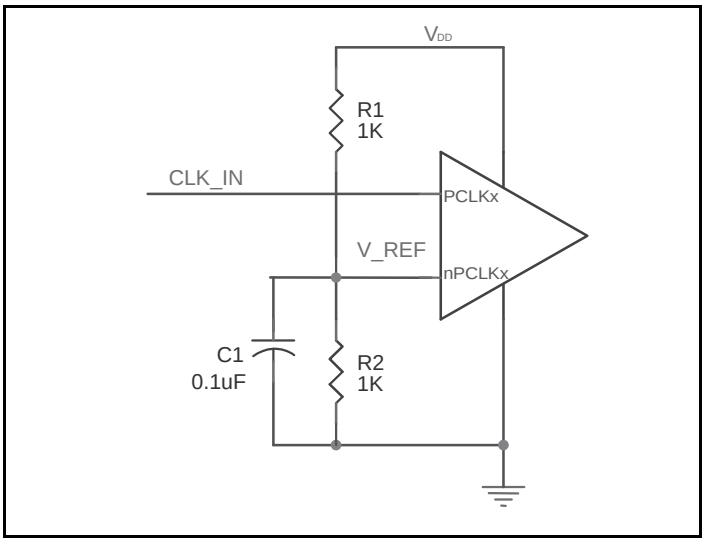


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs

PCLK/nPCLK Inputs:

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

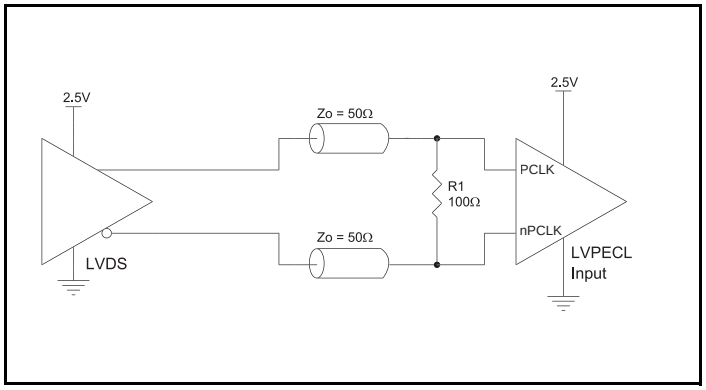


Figure 2A. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

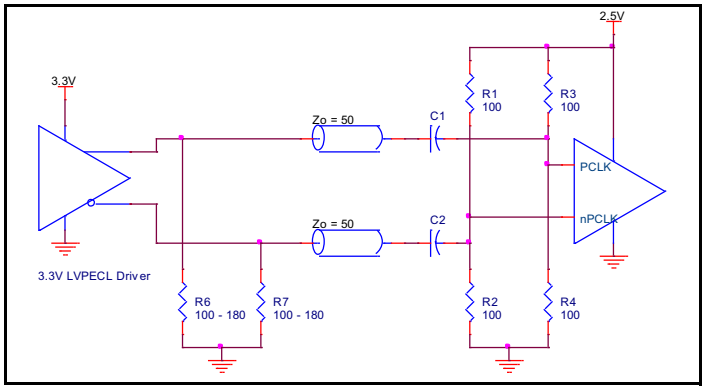


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

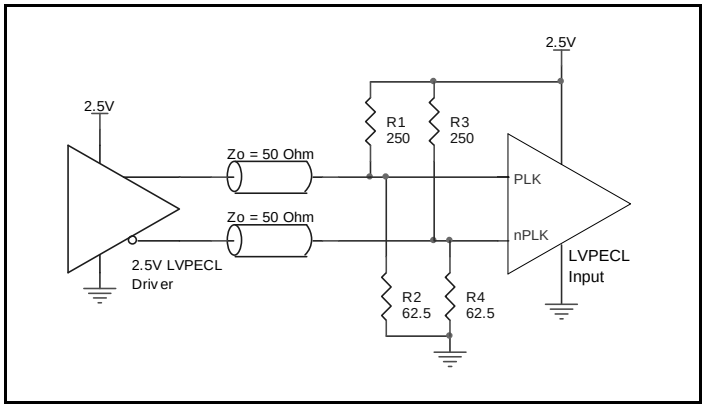
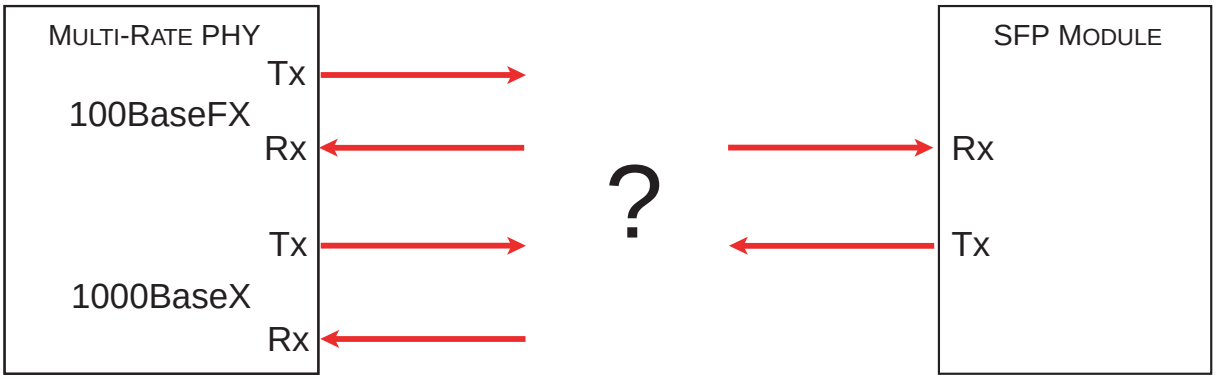


Figure 2C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

A Typical Application for the 855S54

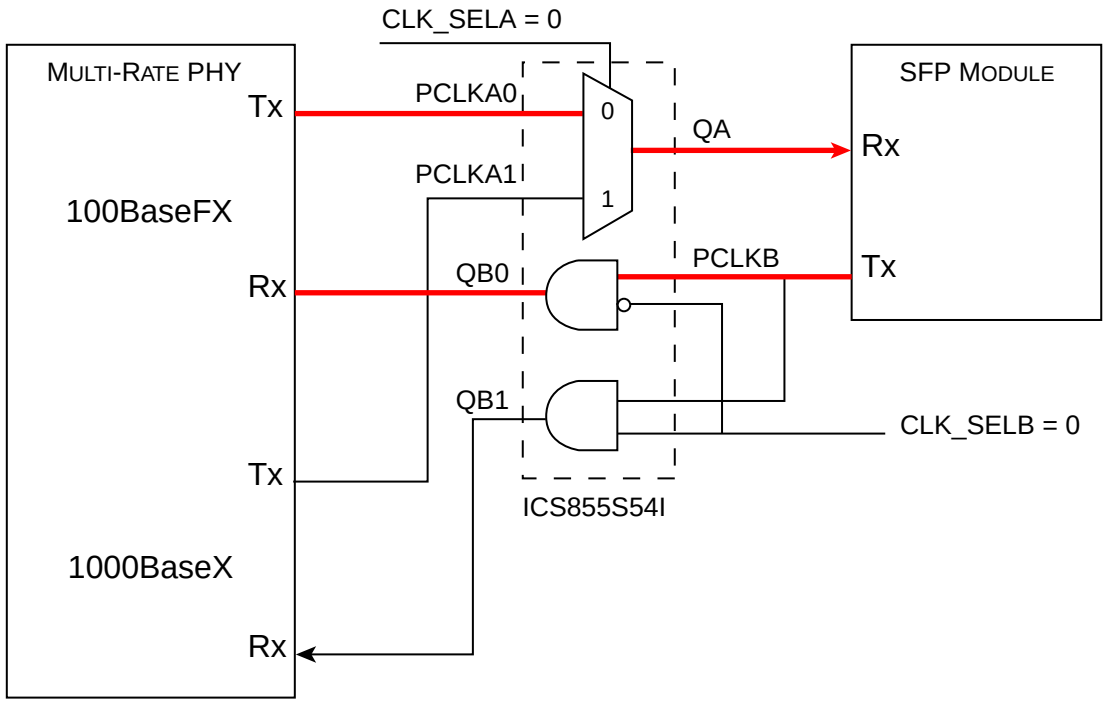
Used to connect a multi-rate PHY with the Tx/Rx pins of an SFP Module.

Problem Addressed: How to map the 2 Tx/Rx pairs of the multi-rate PHY to the single Tx/Rx pair on the SFP Module.



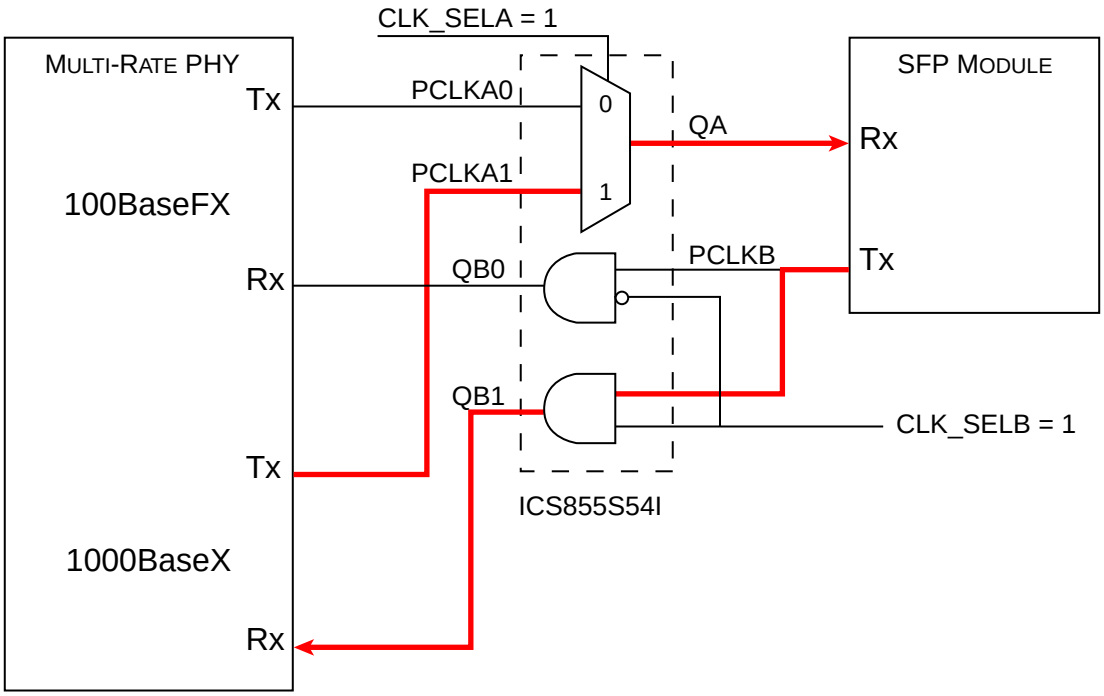
Mode 1, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing. Bold red lines are active connections highlighting the signal path.



Mode 2, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing. Bold red lines are active connections highlighting the signal path.



VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

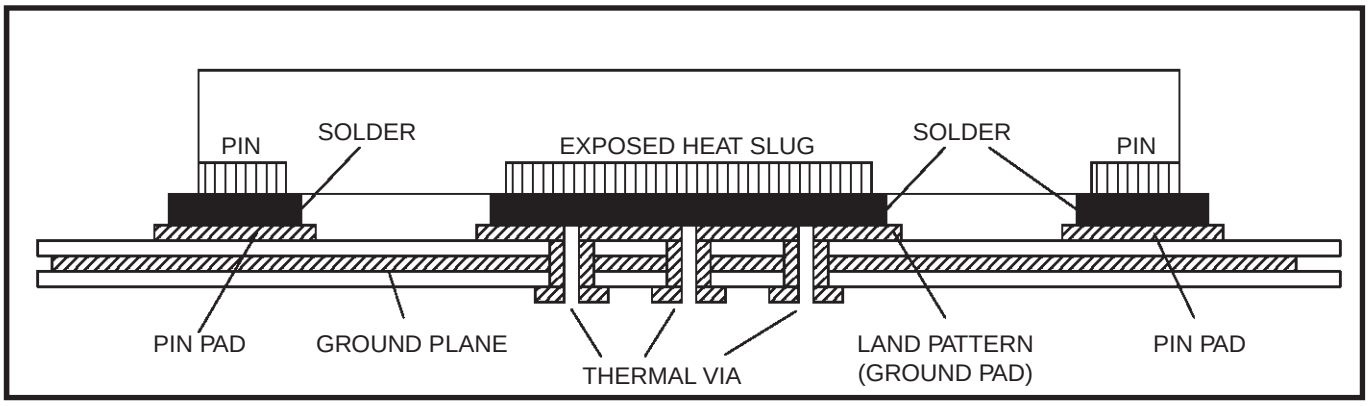


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

2.5V LVDS Driver Termination

Figure 4 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

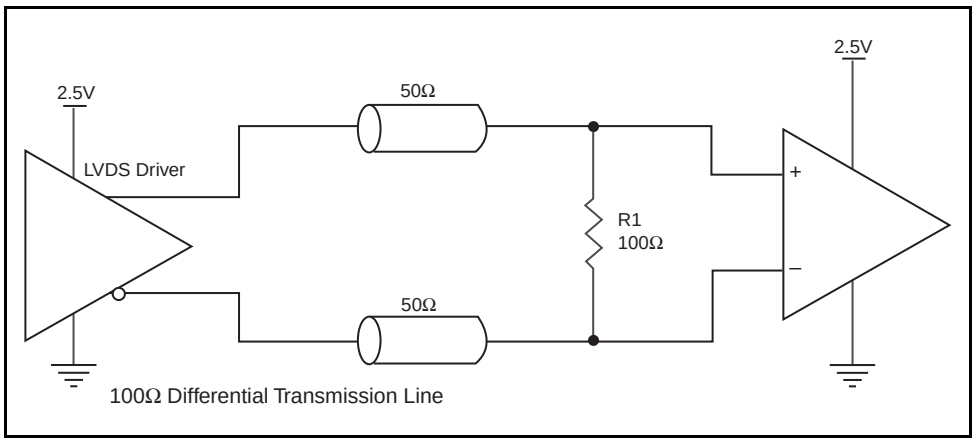


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 855S54.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 855S54 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 2.625V * 100mA = **262.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.266W * 74.7°C/W = 104.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 855S54 is: 299

This device is pin and function compatible and a suggested replacement for 855S54.

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
855S54AKILF	554A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
855S54AKILFT	554A	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Revision Date	Description of Change
September 19, 2017	Updated the package outline drawings; however, no mechanical changes Completed other minor improvements
February 10, 2016	General Description - deleted HiperClocks logo. Ordering Information Table - deleted count for Tape & Reel. Deleted “ICS” prefix and “I” suffix in the part number throughout the datasheet.

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www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

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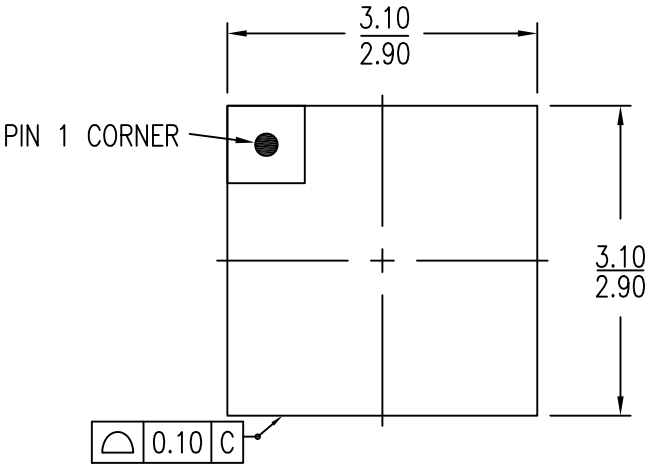
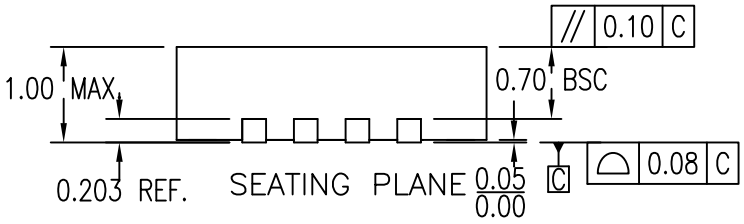
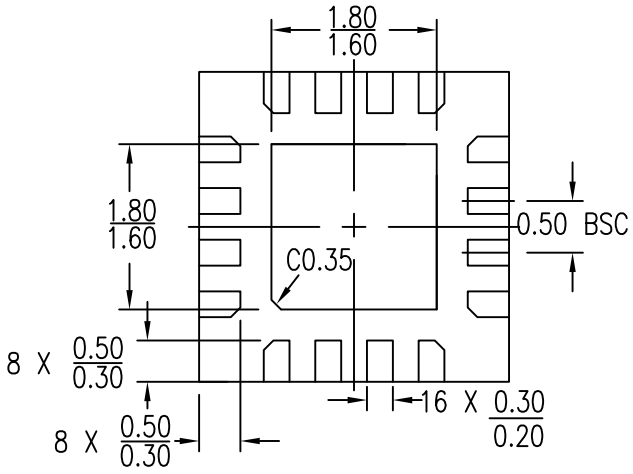


TOP VIEW



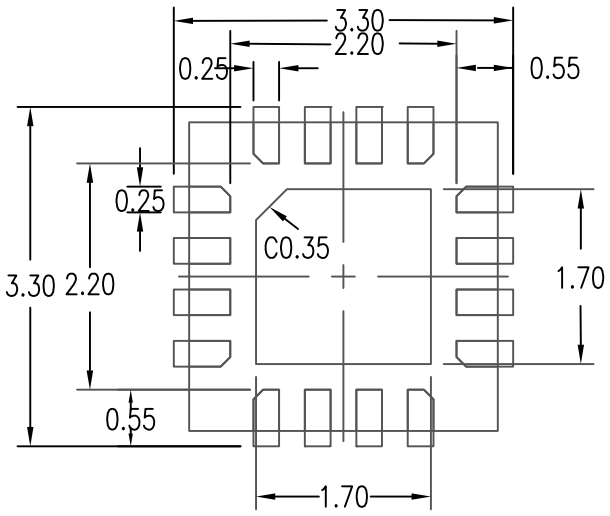
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Aug 15, 2017	Rev 03	Update Epad Range
Jul 28, 2017	Rev 02	New format