

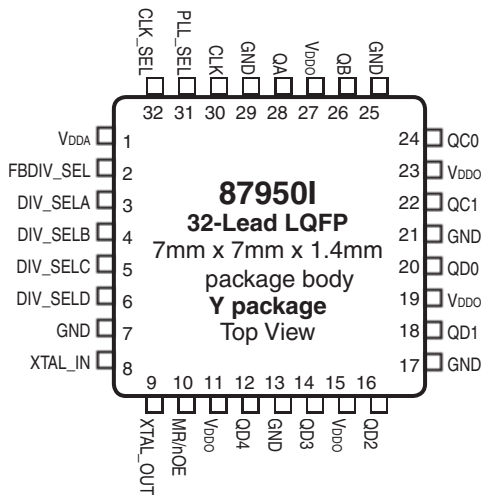
## GENERAL DESCRIPTION

The 87950I is a low voltage, low skew 1-9 LVCMOS/LVTTTL Clock Generator. With output frequencies up to 250MHz the 87950I is targeted for high performance clock applications. Along with a fully integrated PLL the 87950I contains frequency configurable outputs.

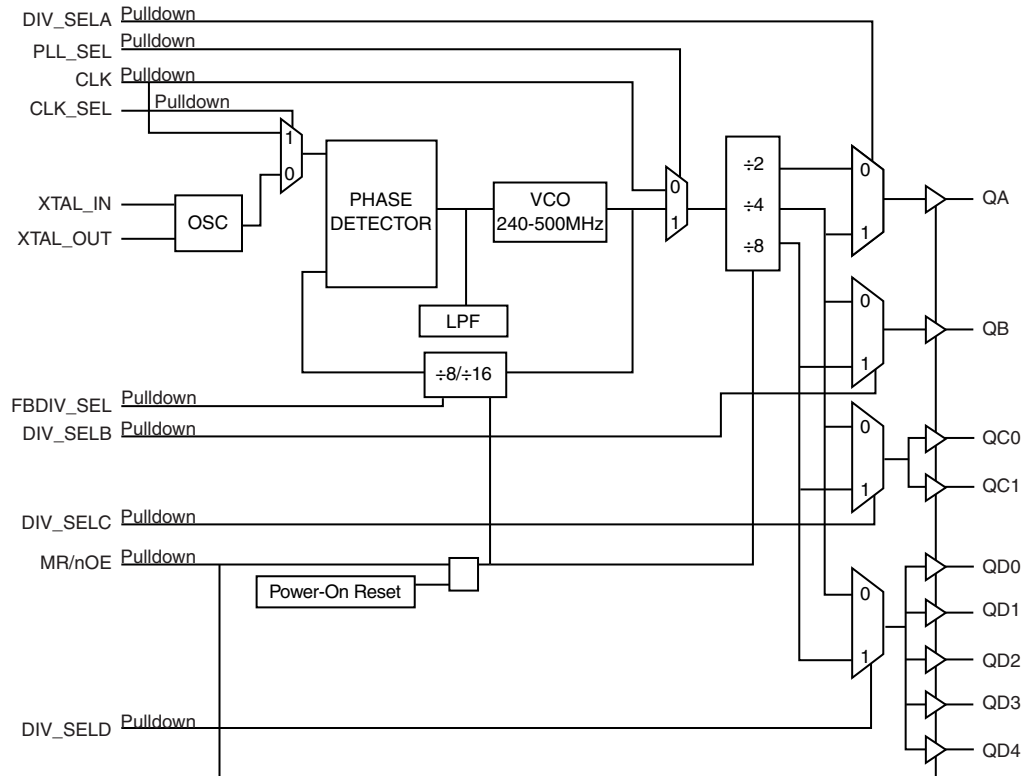
## FEATURES

- Fully integrated PLL
- 9 single ended 3.3V LVCMOS/LVTTTL outputs
- Selectable CLK or single ended crystal inputs
- Maximum output frequency: 250MHz
- Maximum VCO range: 240MHz to 500MHz
- Cycle-to-cycle jitter:  $\pm 100$  (typical)
- Output skew: 375ps (maximum) all outputs @ same frequency
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 87973i

## PIN ASSIGNMENT



## BLOCK DIAGRAM



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2	FBDIV_SEL	Input	Pulldown	Selects divide value for Bank feedback output as described in Table 3E. LVCMOS / LVTTTL interface levels.
3	DIV_SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTTL interface levels.
4	DIV_SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTTL interface levels.
5	DIV_SELC	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3D. LVCMOS / LVTTTL interface levels.
6	DIV_SELD	Input	Pulldown	Selects divide value for Bank D outputs as described in Table 3D. LVCMOS / LVTTTL interface levels.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground.
8, 9	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
10	MR/nOE	Input	Pulldown	Active High Master Reset. Active Low Output Enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
11, 15, 19, 23, 27	V <sub>DDO</sub>	Power		Output supply pins.
12, 14, 16, 18, 20	QD4, QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.
22, 24	QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.
26	QB	Output		Bank B clock output. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.
28	QA	Output		Bank A clock output. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.
30	CLK	Input	Pulldown	LVCMOS / LVTTTL phase detector reference clock input.
31	PLL_SEL	Input	Pulldown	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTTL interface levels.
32	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK. When LOW, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTTL interface levels.

NOTE: refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDA</sub> , V <sub>DDO</sub> = 3.47V		25		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

**TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE**

Inputs	Outputs			
MR/nOE	QA	QB	QC0, QC1	QD0:QD4
1	HiZ	HiZ	HiZ	HiZ
0	Enabled	Enabled	Enabled	Enabled

**TABLE 3B. OPERATING MODE FUNCTION TABLE**

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

**TABLE 3C. PLL INPUT FUNCTION TABLE**

Inputs	
CLK_SEL	PLL Input
0	XTAL Oscillator
1	CLK

**TABLE 3D. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE FOR FBDIV-SEL**

Inputs	
FBDIV_SEL	Function
1	÷8
0	÷16

TABLE 3E. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

Inputs				Outputs			
DIV_SEL A	DIV_SEL B	DIV_SEL C	DIV_SEL D	QA	QB	QCx	QDx
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

TABLE 3F. INPUT REFERENCE VS. OUTPUT FREQUENCY RELATIONSHIP

Inputs				Outputs							
DIV_SEL A	DIV_SEL B	DIV_SEL C	DIV_SEL D	FBDIV_SEL = 1				FBDIV_SEL = 0			
				QA	QB	QCx	QDx	QA	QB	QCx	QDx
0	0	0	0	4x	2x	2x	2x	8x	4x	4x	4x
0	0	0	1	4x	2x	2x	x	8x	4x	4x	2x
0	0	1	0	4x	2x	x	2x	8x	4x	2x	4x
0	0	1	1	4x	2x	x	x	8x	4x	2x	2x
0	1	0	0	4x	x	2x	2x	8x	2x	4x	4x
0	1	0	1	4x	x	2x	x	8x	2x	4x	2x
0	1	1	0	4x	x	x	2x	8x	2x	2x	4x
0	1	1	1	4x	x	x	x	8x	2x	2x	2x
1	0	0	0	2x	2x	2x	2x	4x	4x	4x	4x
1	0	0	1	2x	2x	2x	x	4x	4x	4x	2x
1	0	1	0	2x	2x	x	2x	4x	4x	2x	4x
1	0	1	1	2x	2x	x	x	4x	4x	2x	2x
1	1	0	0	2x	x	2x	2x	4x	2x	4x	4x
1	1	0	1	2x	x	2x	x	4x	2x	4x	2x
1	1	1	0	2x	x	x	2x	4x	2x	2x	4x
1	1	1	1	2x	x	x	x	4x	2x	2x	2x

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DDA} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	42.1°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DDA}$	Analog Supply Current				15	mA
$I_{DDO}$	Output Supply Current				115	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IN}$	Input Current	$V_{DDA} = V_{IN} = 3.465V$			$\pm 120$	$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1		2.6			V
$V_{OL}$	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50 $\Omega$  to  $V_{DDO}/2$ .

**TABLE 5. CRYSTAL CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

**TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Reference Frequency; NOTE 1		15		62.5	MHz

NOTE 1: Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the CLK input.

**TABLE 7. AC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	$\pm 2$			250	MHz
		$\pm 4$			125	MHz
		$\pm 8$			62.5	MHz
$f_{VCO}$	PLL VCO Lock Range		240		500	MHz
$\tau_{sk(o)}$	Output Skew; NOTE 1, 4	Same Frequency			375	ps
		Different Frequency	$QA f_{MAX} < 150MHz$		500	ps
			$QA f_{MAX} > 150MHz$		750	ps
$\tau_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2, 4			$\pm 100$		ps
$t_L$	PLL Lock Time; NOTE 4				10	mS
$t_R / t_F$	Output Rise/Fall Time	0.8V to 2V	0.1		1	ns
$t_{PW}$	Output Pulse Width; NOTE 3		$t_{PERIOD}/2 - 1000$		$t_{PERIOD}/2 + 1000$	ps
$t_{PZL}, t_{PZH}$	Output Enable Time				6	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time				7	ns

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

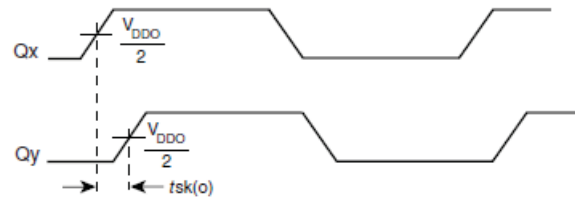
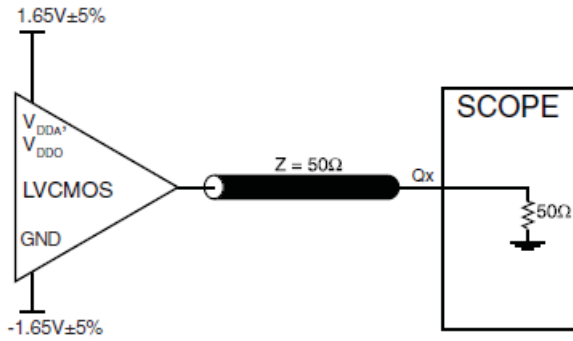
Measured at  $V_{DDO}/2$ .

NOTE 2: Jitter performance using Xtal inputs.

NOTE 3: Measured using CLK.

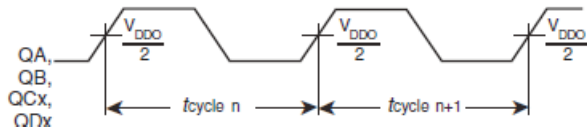
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

## PARAMETER MEASUREMENT INFORMATION



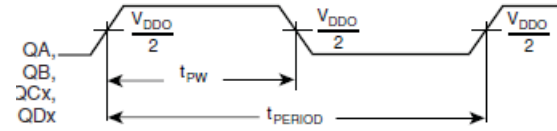
### 3.3V OUTPUT LOAD AC TEST CIRCUIT

### OUTPUT SKEW



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

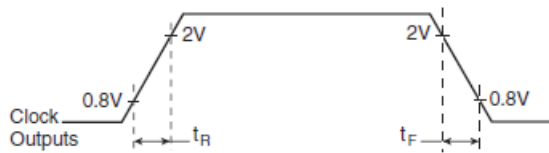
1000 Cycles



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

### CYCLE-TO-CYCLE JITTER

### OUTPUT PULSE WIDTH/PERIOD



### OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 87950I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DDO}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

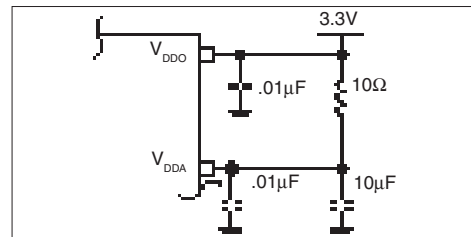


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The 87950I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

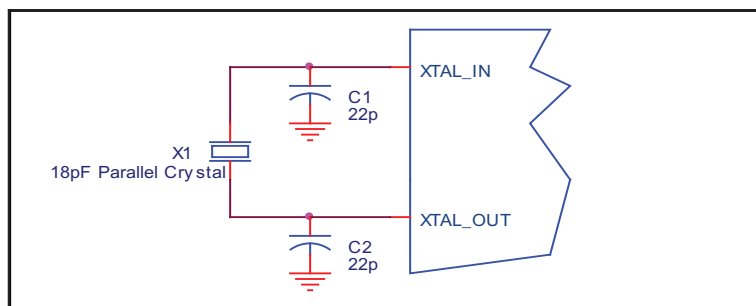


FIGURE 2. CRYSTAL INPUT INTERFACE



## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 87950I is: 2674

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

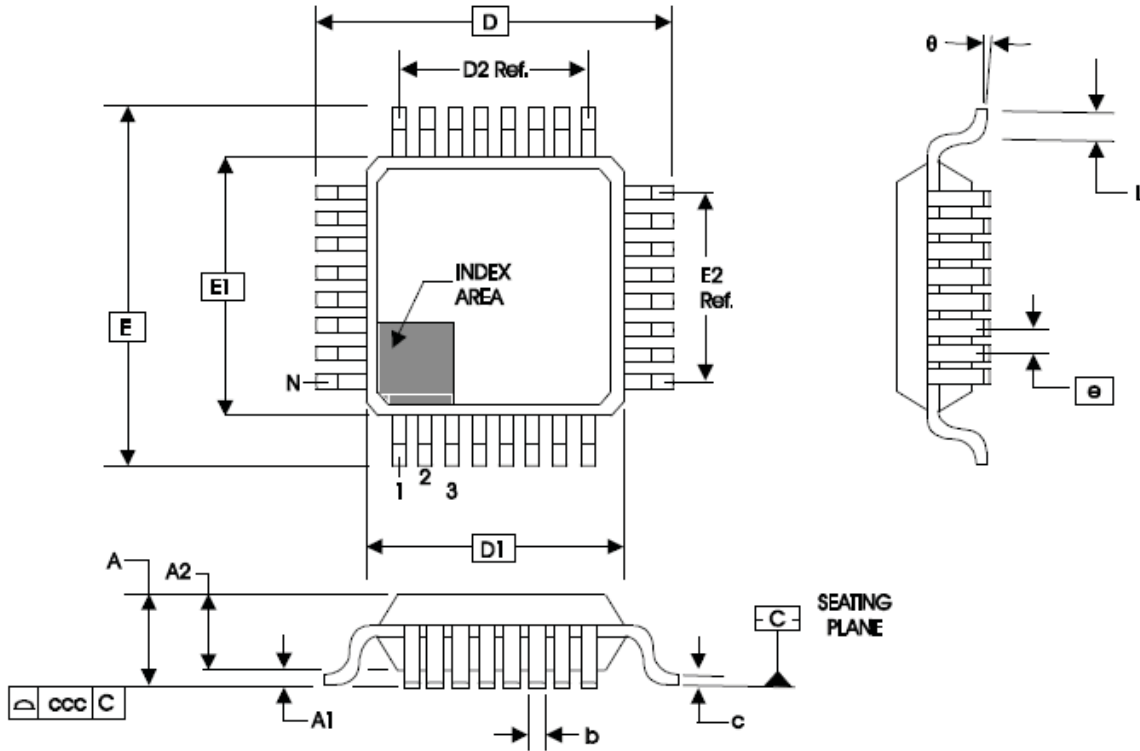


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

**TABLE 10. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87950BYILF	ICS87950BYIL	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
87950BYILFT	ICS87950BYIL	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T5 T10	1	Features Section - added Lead-Free bullet.	6/14/05
		5	Crystal Characteristics Table - added Drive Level.	
		11	Ordering Information Table - added Lead-Free part number and note. Changed XTAL1/2 naming convention to XTAL_IN/_OUT throughout the data-sheet.	
B	T10	11	Ordering Information - Added Lead-Free Marking.	9/8/08
C	T10	11	Updated datasheet's header/footer with IDT from ICS.	7/16/10
		13	Removed ICS prefix from Part/Order Number column. Added Contact Page.	
C	T10	11	Ordering Information - removed leaded devices, PDN CQ-13-02 Updated data sheet format	2/18/15
C		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05.	11/6/15



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