Overview
The 8A34044 Four-Channel Universal Frequency Translator is a highly integrated timing device with four Digital PLL (DPLL) and four Digitally Controlled Oscillator (DCO) channels. The DPLLs can lock to external references or operate in free run, and can be configured as DCOs. Each of the DCOs can be synchronized by any of the DPLLs or they can operate in free run. The DCOs can alternatively be controlled by an external algorithm for Optical Transport Network (OTN) applications.

Typical Applications
- Core and access IP switches / routers
- Synchronous Ethernet equipment
- 10Gb, 40Gb, and 100Gb Ethernet interfaces
- Wireless infrastructure for 4.5G and 5G network equipment
- OTN muxponders and line cards

Features
- Close-in phase noise complies with Common Public Radio Interface (CPRI) frequency synchronization requirements
- Supports all ITU-T G.709 frequencies
- Meets OTN jitter and wander requirements per ITU-T G.8251
- Four independent timing channels
  - Each can act as a frequency synthesizer, jitter attenuator, Digitally Controlled Oscillator (DCO), or Digital Phase Lock Loop (DPLL)
  - DPLL Digital Loop Filters (DLFs) are programmable with cut-off frequencies from 17Hz to 22kHz
  - Generates output frequencies that are independent of input frequencies via a Fractional Output Divider (FOD)
  - Each FOD supports output phase tuning with 50ps resolution
- Four Satellite DCO channels
  - Each can act as a frequency translator connected to either DPLL channel or as an independent frequency synthesizer
  - Generates output frequencies that are independent of input frequencies via a Fractional Output Divider (FOD)
  - Each FOD supports output phase tuning with 50ps resolution
- 12 differential / 24 LVCMOS outputs
  - Frequencies from 0.5Hz to 1GHz (250MHz for LVCMOS)
  - Jitter below 150fs RMS (10kHz to 20MHz)
  - Supports LVCMOS, LVDS, LVPECL, HCSL, CML, SSTL, and HSTL output modes
  - Differential output swing is selectable: 400mV / 650mV / 800mV / 910mV
  - Independent output voltages of 3.3V, 2.5V, or 1.8V
  - LVCMOS additionally supports 1.5V or 1.2V
  - The clock phase of each output is individually programmable in 1ns to 2ns steps with a total range of ±180°
- 4 differential / 8 single-ended clock inputs
  - Supports frequencies from 1kHz to 1GHz
  - Any input can be mapped to any or all of the timing channels
  - Redundant inputs frequency independent of each other
  - Any input can be designated as external frame/sync pulse of EPPS (even pulse per second), 1PPS (Pulse per Second), 5PPS, 10PPS, 50Hz, 1kHz, 2kHz, 4kHz, and 8kHz associated with a selectable reference clock input
  - Per-input programmable phase offset of up to ±1.638μs in 50ps steps
- Reference monitors qualify/disqualify references depending on LOS, activity, frequency monitoring, and/or LOS input pins
  - Loss of Signal (LOS) input pins (via GPIOs) can be assigned to any input clock reference
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive / non-revertive, and other programmable settings
- System APLL operates from fundamental-mode crystal: 25MHz to 54MHz or from a crystal oscillator
- System DPLL accepts an XO, TCXO, or OCXO operating at virtually any frequency from 1MHz to 150MHz
- DPLLs can be configured as DCOs to synthesize clocks under the control of an external algorithm
  - DCOs generate with frequency resolution less than $1.11 \times 10^{-16}$
- Supports 1MHz I²C or 50MHz SPI serial processor ports
- Can configure itself automatically after reset via:
  - Internal Customer-programmable One-Time Programmable (OTP) memory with up to 16 different configurations
  - Standard external I²C EEPROM if serial port in I²C mode
- 1149.1 JTAG Boundary Scan
- 10 x 10 mm 72-QFN package

©2019 Integrated Device Technology, Inc

June 17, 2019
Description

The 8A34044 Four-Channel Universal Frequency Translator is a highly integrated timing device with four Digital PLL (DPLL) channels and four Digitally Controlled Oscillator (DCO) channels. The DPLLs can lock to external references or operate in free run, and can be configured as DCOs. Each of the DCOs can be synchronized by any of the DPLLs or they can operate in free run. The DCOs can alternatively be controlled by an external algorithm for Optical Transport Network (OTN) applications.

The 8A34044 supports precise control of input-to-input, input-to-output, and output-to-output phase skew. The device outputs low-jitter clocks that can directly synchronize interfaces such as 100GBASE-R, 40GBASE-R, 10GBASE-R, and 10GBASE-W and lower-rate Ethernet interfaces, as well as SONET/SDH and PDH interfaces.
The internal System APLL must be supplied with a low phase noise reference clock with frequency between 25MHz and 54MHz. The output of the System APLL is used for clock synthesis by all of the Fractional Output Dividers (FODs) in the device. The System APLL reference can come from an external crystal oscillator connected to the OSCI pin or from an internal oscillator that uses a crystal connected between the OSCI and OSCO pins.

The System DPLL generates an internal system clock that is used by the reference monitors and other digital circuitry in the device. If the reference provided to the System APLL meets the stability and accuracy requirements of the intended application then the System DPLL can free run and a System DPLL reference is not required. Alternatively, the System DPLL can be locked to an external reference that meets the stability and accuracy requirements of the intended application. The System DPLL can accept a reference from the XO_DPLL pin or via the reference selection mux.

The frequency accuracy/stability of the internal system clock determines the frequency accuracy/stability of the DPLLs in Free-Run mode and in Holdover mode, and also affects the wander generation of the DPLLs in Locked and DCO modes. When provided with a suitably stable and accurate system clock, the DPLLs meet the frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of ITU-T G.8262 synchronous Ethernet Equipment Clock (EEC) options 1 and 2.

The 8A34044 accepts up to four differential reference inputs and up to eight single-ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH, PDH frequencies, and any input frequency from 1kHz to 1GHz (250MHz in single-ended mode). The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all the DPLLs. The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities, locking allowances, reference monitors, revertive and non-revertive settings, and LOS inputs.

The 8A34044 provides four independent Digital Phase Lock Loops (DPLLs) consisting of a Phase Frequency Detector (PFD), a Low Pass Filter (LPF), and a Digitally Controlled Oscillator (DCO). The DPLL architecture allows external processors to access the control loop at several points to monitor and control the loop. A processor can directly control the DCOs; and it can implement a proprietary filter and control algorithm to replace the internal LPF.

The 8A34044 can accept a clock reference and an associated frame pulse or sync signal as a pair. The DPLLs can lock to the clock reference and align the sync and clock outputs with the paired sync/frame input. The device allows any of the reference inputs to be configured as sync inputs that can be associated with any of the other reference inputs. The input sync signals can have a frequency of 1PPS (Pulse per Second), EPPS (even pulse per second), 5PPS, 10PPS, 50Hz, 100Hz, 1kHz, 2kHz, 4kHz, and 8kHz. This feature enables any DPLL to phase align its frame sync and clock outputs with a sync input without the need to use a low bandwidth setting to lock directly to the sync input.

The DPLLs support four primary operating modes: Free-Run, Locked, Holdover, and DCO. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth, and the long-term output frequency accuracy is the same as the long-term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO mode, the DPLL control loop is opened and the DCO can be controlled by a PTP clock recovery servo running on an external processor to synthesize PTP clocks.

The DPLLs can be configured with a range of selectable filtering bandwidths from 17Hz to 22kHz for use in jitter attenuation and rate conversion applications.

In addition, there are four Satellite channels that can operate either as independent frequency synthesizers, as DCOs, or as frequency translators. In synthesizer mode, a channel uses a Fractional Output Divider (FOD) clocked from the System APLL to generate any desired output frequency. In DCO mode, the channel can be controlled by an external algorithm via serial port to dynamically adjust the output clock frequency. In frequency translation mode, the FOD will receive frequency-tracking information from any DPLL channel, tracking the input that DPLL channel is locked to, but with an output frequency that is a fractional ratio to the DPLL it is tracking.

All of the channels within the 8A34044 derive their output frequencies from the same System APLL clock, and therefore, the control words used to tune the DCOs are interchangeable.

The 8A34044 generates up to 12 differential output clocks at any frequency from 0.5Hz to 1GHz. The differential outputs can support LVPECL, LVDS, HCSL, and CML. It generates up to 24 single-ended clocks with frequencies from 0.5Hz to 250MHz. LVCMOS output supports 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. Each output stage can be independently configured.
Clocks generated by the 8A34044 have jitter below 150fs RMS (10kHz to 20MHz), and therefore are suitable for serial 100GBASE-R, 40GBASE-R, and lower rate interfaces.

All control and status registers are accessed through the I²C / SPI slave microprocessor interface. The SPI interface mode supports high clock rates (up to 50MHz). For configuring the DPLLs, the 8A34044 has an internal customer-programmable OTP memory with up to 16 different configurations. If the serial port is configured in I²C mode, then the 8A34044 can become master on this I²C bus and read configuration data from a standard I²C EEPROM that shares the I²C bus. If the serial port is configured in SPI mode then this capability is unavailable.
## Contents

Overview ........................................................................................................................................................................... 1  
Typical Applications................................................................................................................................................................ 1  
Features .................................................................................................................................................................................. 1  
Block Diagram ...................................................................................................................................................................... 2  
Description ........................................................................................................................................................................... 2  
Pin Assignment ...................................................................................................................................................................... 10  
Pin Descriptions and Pin Characteristics .............................................................................................................................. 10  
Overview of the 8A3xxxx Family ........................................................................................................................................ 15  
Functional Description ........................................................................................................................................................... 15  
Basic Functional Blocks of the 8A34044 .............................................................................................................................. 16  
Crystal Input (OSCI / OSCO) .................................................................................................................................................. 16  
   Frequency Representation in 8A34044 ................................................................................................................................. 16  
System Analog PLL (APLL) ..................................................................................................................................................... 16  
Input Stage ............................................................................................................................................................................... 17  
Reference Monitoring ............................................................................................................................................................. 19  
   Loss of Signal (LOS) Monitoring ........................................................................................................................................ 19  
   Activity ................................................................................................................................................................................... 20  
   Timer ...................................................................................................................................................................................... 21  
   Frequency Offset Monitoring ............................................................................................................................................... 21  
Advanced Input Clock Qualification ...................................................................................................................................... 22  
   Input Clock Qualification ..................................................................................................................................................... 22  
   Clock Reference Disqualifier through GPIO ......................................................................................................................... 22  
Frame Pulse Operation ............................................................................................................................................................ 22  
Sync Pulse Operation ............................................................................................................................................................. 23  
Crystal Oscillator Input (XO_DPLL) ........................................................................................................................................ 24  
Digital Phase Locked Loop (DPLL) ........................................................................................................................................ 24  
   Free-Run Mode .................................................................................................................................................................... 26  
   Locked Mode ......................................................................................................................................................................... 26  
   Holdover Mode ..................................................................................................................................................................... 26  
   Manual Holdover Mode ....................................................................................................................................................... 26  
   External Feedback ............................................................................................................................................................ 27  
DPLL Input Clock Qualification and Selection .......................................................................................................................... 27  
   Automatic Input Clock Selection ......................................................................................................................................... 28  
   Manual Input Clock Selection via Register or GPIO ................................................................................................................ 28  
   Slave or GPIO Slave Selection .............................................................................................................................................. 28  
DPLL Switchover Management ................................................................................................................................................ 28  
   Revertive and Non-Revertive Switching ............................................................................................................................... 28  
   Hitless Reference Switching ............................................................................................................................................... 28  
   Phase Slope Limiting .......................................................................................................................................................... 29  
   DPLL Frequency Offset Limit Setting ................................................................................................................................. 29  
DPLL Fast Lock Operation .................................................................................................................................................... 29  
Satellite Channel .................................................................................................................................................................... 30  
Steerable Fractional Output Divider (FOD) ............................................................................................................................ 30  
FOD Multiplexing and Output Stages .................................................................................................................................. 31  
   Integer Output Divider ......................................................................................................................................................... 32  
   Output Duty Cycle Adjustment ............................................................................................................................................ 33  
   Output Coarse Phase Adjustment ....................................................................................................................................... 33  
   Output Buffer ....................................................................................................................................................................... 34
Applications Information ..................................................................................................................................................................................... 79
Recommendations for Unused Input and Output Pins........................................................................................................................................ 79
   Inputs ................................................................................................................................................................................................. 79
   Outputs .............................................................................................................................................................................................. 79
   Power Connections ........................................................................................................................................................................... 79
Clock Input Interface ................................................................................................................................................................................... 79
Overdriving the XTAL Interface ................................................................................................................................................................. 80
Wiring the Differential Input to Accept Single-Ended Levels ...................................................................................................................... 81
Differential Output Termination ................................................................................................................................................................. 81
Crystal Recommendation ............................................................................................................................................................................ 81
External I2C Serial EEPROM Recommendation ........................................................................................................................................ 82
Schematic and Layout Information .............................................................................................................................................................. 82
Power Considerations .................................................................................................................................................................................. 82
QFN EPAD Thermal Release Path ............................................................................................................................................................. 83
Thermal Characteristics ................................................................................................................................................................................ 83
Package Outline Drawings ............................................................................................................................................................................. 84
Marking Diagram ................................................................................................................................................................................................ 84
Ordering Information .................................................................................................................................................................................. 84
Product Identification .................................................................................................................................................................................. 85
Glossary ............................................................................................................................................................................................................. 86
Revision History ....................................................................................................................................................................................... 87
List of Figures

Figure 1. Block Diagram .................................................................................................................. 2
Figure 2. Pin Assignments for 10 × 10 mm 72-QFN Package .......................................................... 10
Figure 3. Single PLL Channel ......................................................................................................... 15
Figure 4. System Analog PLL Channel .......................................................................................... 16
Figure 5. Input Stage Configured as Differential Only ................................................................. 17
Figure 6. Input Stage Configured as Dual Single-Ended ............................................................... 18
Figure 7. Input Stage Configured as Differential Plus Single-Ended ........................................... 19
Figure 8. Frame Pulse Operation ................................................................................................. 23
Figure 9. Sync Pulse Operation .................................................................................................... 23
Figure 10. DPLL Channel ............................................................................................................. 24
Figure 11. DPLL Automatic State Machine .................................................................................. 25
Figure 12. External Feedback ........................................................................................................ 27
Figure 13. Satellite Channel Block Diagram ................................................................................ 30
Figure 14. Steerable Fractional Divider Block ............................................................................. 30
Figure 15. Single Output Stage ..................................................................................................... 32
Figure 16. Dual Output Stage ........................................................................................................ 32
Figure 17. Power-Up Reset Sequencing ........................................................................................ 41
Figure 18. Register Addressing Modes via Serial Port .................................................................. 44
Figure 19. I2C Slave Sequencing .................................................................................................. 45
Figure 20. I2C Slave Timing Diagram .......................................................................................... 46
Figure 21. I2C Master Sequencing ............................................................................................... 47
Figure 22. SPI Sequencing ........................................................................................................... 48
Figure 23. SPI Timing Diagram .................................................................................................... 50
Figure 24. Free-Running Synthesizer Operation ......................................................................... 52
Figure 25. Clock Generator Operation ........................................................................................ 52
Figure 26. Synthesizer Disciplined with Oscillator Operation ..................................................... 53
Figure 27. Jitter Attenuator Operation .......................................................................................... 53
Figure 28. Jitter Attenuator Operation with External Digital Loop Filter ....................................... 54
Figure 29. Jitter Attenuator Disciplined with Oscillator Operation .............................................. 54
Figure 30. External DCO Control via Frequency Control Word ................................................... 55
Figure 31. External DCO Control via Phase Control Word .......................................................... 56
Figure 32. Phase Control in Closed Loop Operation ....................................................................... 57
Figure 33. Combo Mode ............................................................................................................... 58
Figure 34. Input-Output Delay ..................................................................................................... 77
Figure 35. 156.25MHz Output Phase Noise ................................................................................ 78
Figure 36. 1.8V LVCMOS Driver to XTAL Input Interface .......................................................... 80
Figure 37. LVCMOS Driver to XTAL Input Interface ..................................................................... 80
Figure 38. LVPECL Driver to XTAL Input Interface ....................................................................... 81
Figure 39. Standard LVDS Termination ....................................................................................... 81
Figure 40. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing Not to Scale) .................................................................................. 83

©2019 Integrated Device Technology, Inc

June 17, 2019
List of Tables

| Table 1. | Pin Descriptions | 10 |
| Table 2. | Pin Characteristics | 14 |
| Table 3. | Related Documentation | 15 |
| Table 4. | Input Stage Setting | 17 |
| Table 5. | Input Stages Using GPIOs as Reference Clock Inputs | 18 |
| Table 6. | Gapped Clock LOS Settings | 20 |
| Table 7. | Activity Limit | 20 |
| Table 8. | Disqualification Timer | 21 |
| Table 9. | Qualification Timer | 21 |
| Table 10. | Frequency Offset Limits | 21 |
| Table 11. | DPLL Bandwidth | 26 |
| Table 12. | DPLL Reference Mode | 27 |
| Table 13. | Some Key DPLL Phase-Slope Limits Supported | 29 |
| Table 14. | FOD to Output Stage to Output Pin Mappings | 31 |
| Table 15. | FOD to Output Stage to Output Pin Mappings | 31 |
| Table 16. | Output Duty Cycle Examples | 33 |
| Table 17. | Configurable Output Mode Options | 34 |
| Table 18. | Alarm Indications | 37 |
| Table 19. | GPIO Pin Usage at Start-Up | 38 |
| Table 20. | Serial Port Pin to Function Mapping | 44 |
| Table 21. | I2C Slave Timing | 46 |
| Table 22. | SPI Timing | 50 |
| Table 23. | JTAG Signal Mapping | 51 |
| Table 24. | Abbreviated Signal Names and the Detailed Signal Names Referenced by Them | 59 |
| Table 25. | Absolute Maximum Ratings | 60 |
| Table 26. | Recommended Operating Conditions | 60 |
| Table 27. | Power Supply DC Characteristics | 61 |
| Table 28. | Output Supply DC Characteristics (Output Configured as Differential) | 64 |
| Table 29. | Output Supply Current (Output Configured as LVCMOS) | 64 |
| Table 30. | LVCMOS/LVTTL DC Characteristics | 65 |
| Table 31. | Differential Input DC Characteristics | 66 |
| Table 32. | Differential Output DC Characteristics ($V_{DDO,Qx} = 3.3V+5\%$, $V_{SS} = 0V$, $T_A = -40\degree C$ to $85\degree C$) | 67 |
| Table 33. | Differential Output DC Characteristics ($V_{DDO,Qx} = 2.5V+5\%$, $V_{SS} = 0V$, $T_A = -40\degree C$ to $85\degree C$) | 68 |
| Table 34. | Differential Output DC Characteristics ($V_{DDO,Qx} = 1.8V+5\%$, $V_{SS} = 0V$, $T_A = -40\degree C$ to $85\degree C$) | 69 |
| Table 35. | LVCMOS Clock Output DC Characteristics | 70 |
| Table 36. | Input Frequency Characteristics | 71 |
| Table 37. | Crystal Characteristics | 71 |
| Table 38. | AC Characteristics | 72 |
| Table 39. | Recommended Tuning Capacitors for Crystal Input | 82 |
| Table 40. | Thermal Characteristics for 72-QFN Package | 83 |
| Table 41. | Pin 1 Orientation in Tape and Reel Packaging | 85 |
| Table 42. | Product Identification | 85 |
Pin Assignment

Figure 2. Pin Assignments for 10 × 10 mm 72-QFN Package[1]

Table 1. Pin Descriptions[1]

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OSCO</td>
<td>Output</td>
<td>Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to the OSCI pin, this pin should be left unconnected.</td>
</tr>
<tr>
<td>2</td>
<td>OSCI</td>
<td>Input</td>
<td>Crystal Input. Accepts a reference from a clock oscillator or a fundamental mode parallel-resonant crystal (see Table 36 and Table 37).</td>
</tr>
</tbody>
</table>

[1] Note that indexed signals (e.g. GPIO[5]) are not necessarily numbered sequentially. Some indexes may be skipped. This is to maintain software compatibility with other members of the family of devices.
<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>( V_{DDA_PDCP_XTAL} )</td>
<td>Power</td>
<td>Analog power supply voltage for System Analog PLL’s phase detector and charge pump, as well as the oscillator circuit associated with OSCI / OSCO pins. 2.5V or 3.3V operation supported.[^{[b]}]</td>
</tr>
<tr>
<td>4</td>
<td>( V_{DDA_FB} )</td>
<td>Power</td>
<td>Analog power supply voltage for System Analog PLL’s feedback divider, 1.8V required.</td>
</tr>
<tr>
<td>5</td>
<td>( nMR )</td>
<td>Input</td>
<td>Pull-up Master Reset input (see Device Initial Configuration).</td>
</tr>
<tr>
<td>6</td>
<td>( V_{DD_CLK} )</td>
<td>Power</td>
<td>Power supply for input clock buffers and dividers. Supports 1.8V, 2.5V or 3.3V as appropriate for the input clock swing (see Input Stage)</td>
</tr>
<tr>
<td>7</td>
<td>( XO_DPLL )</td>
<td>Input</td>
<td>Single-ended crystal oscillator input for System Digital PLL (see Crystal Oscillator Input (XO_DPLL)).</td>
</tr>
<tr>
<td>8</td>
<td>( CLK0 )</td>
<td>Input</td>
<td>Pull-down Positive input for differential input Clock 0 or single-ended input for Clock 0 (see Input Stage).</td>
</tr>
<tr>
<td>9</td>
<td>( nCLK0 )</td>
<td>Input</td>
<td>Pull-up Negative input for differential input Clock 0 or single-ended input for Clock 8 (see Input Stage).</td>
</tr>
<tr>
<td>10</td>
<td>( CLK1 )</td>
<td>Input</td>
<td>Pull-down Positive input for differential input Clock 1 or single-ended input for Clock 1 (see Input Stage).</td>
</tr>
<tr>
<td>11</td>
<td>( nCLK1 )</td>
<td>Input</td>
<td>Pull-up Negative input for differential input Clock 1 or single-ended input for Clock 9 (see Input Stage).</td>
</tr>
<tr>
<td>12</td>
<td>( CLK2 )</td>
<td>Input</td>
<td>Pull-down Positive input for differential input Clock 2 or single-ended input for Clock 2 (see Input Stage).</td>
</tr>
<tr>
<td>13</td>
<td>( nCLK2 )</td>
<td>Input</td>
<td>Pull-up Negative input for differential input Clock 2 or single-ended input for Clock 10 (see Input Stage).</td>
</tr>
<tr>
<td>14</td>
<td>( CLK3 )</td>
<td>Input</td>
<td>Pull-down Positive input for differential input Clock 3 or single-ended input for Clock 3 (see Input Stage).</td>
</tr>
<tr>
<td>15</td>
<td>( nCLK3 )</td>
<td>Input</td>
<td>Pull-up Negative input for differential input Clock 3 or single-ended input for Clock 11 (see Input Stage).</td>
</tr>
<tr>
<td>16</td>
<td>( V_{DD_DIG} )</td>
<td>Power</td>
<td>Power Supply for digital logic. 1.2V or 1.8V supported.</td>
</tr>
<tr>
<td>17</td>
<td>( nc )</td>
<td></td>
<td>Unused. Do not connect.</td>
</tr>
<tr>
<td>18</td>
<td>( nc )</td>
<td></td>
<td>Unused. Do not connect.</td>
</tr>
<tr>
<td>19</td>
<td>( SCLK )</td>
<td>I/O</td>
<td>Pull-up Serial port clock input. Used in both SPI and I(^2)C modes as the clock. May also be used when device boots as I(^2)C Clock Output for I(^2)C Master Operation (see I(^2)C Master). External pull-up recommended in I(^2)C mode.</td>
</tr>
<tr>
<td>20</td>
<td>( SDIO )</td>
<td>I/O</td>
<td>Pull-up Serial port bi-directional data pin. Used as a bi-directional data pin in I(^2)C and 3-wire SPI modes. Used as Serial Data Output pin in 4-wire SPI mode. May also be used when device boots as I(^2)C Bi-directional Data for I(^2)C Master Operation (see I(^2)C Master). External pull-up recommended in I(^2)C mode.</td>
</tr>
<tr>
<td>21</td>
<td>( SDI_A1 )</td>
<td>Input</td>
<td>Pull-up Serial port input. Used as Serial Data In in 4-wire SPI mode and optionally as an Address Bit 1 select input in I(^2)C mode. Unused in 3-wire SPI mode.</td>
</tr>
<tr>
<td>22</td>
<td>( CS_A0 )</td>
<td>Input</td>
<td>Pull-up Serial port input. Used as a Chip Select input in SPI mode and optionally as an Address Bit 0 select input in I(^2)C mode.</td>
</tr>
<tr>
<td>23</td>
<td>( FILTER )</td>
<td>Analog</td>
<td>Reference capacitor for System Analog PLL Loop Filter. Requires a 2.2nF capacitor to ground.</td>
</tr>
</tbody>
</table>

\[^{[a]}\] Table 1: Pin Descriptions (Cont.)
Table 1. Pin Descriptions[^a] (Cont.)

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>$V_{DDA_LC_BG}$</td>
<td>Power</td>
<td>Analog power supply voltage for System Analog PLL’s LC Resonator and bandgap regulator, 3.3V or 2.5V supported[^b]</td>
</tr>
<tr>
<td>25</td>
<td>nTEST</td>
<td>Input</td>
<td>Pull-up</td>
</tr>
<tr>
<td>26</td>
<td>GPIO[3]</td>
<td>I/O</td>
<td>Pull-up[^c]</td>
</tr>
<tr>
<td>27</td>
<td>nQ11</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Q11</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>$V_{DDO_Q11}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>$V_{DD_DIA_FOD_B}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>$V_{DDO_Q7}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Q7</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>nQ7</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>GPIO[9]</td>
<td>I/O</td>
<td>Pull-up[^c]</td>
</tr>
<tr>
<td>35</td>
<td>nQ6</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>Q6</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>$V_{DDO_Q6}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>$V_{DDO_Q5}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>Q5</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>nQ5</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>$V_{DDO_Q4}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>Q4</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>nQ4</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>$V_{DDO_Q10}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>Q10</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>nQ10</td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>GPIO[2]</td>
<td>I/O</td>
<td>Pull-up[^c]</td>
</tr>
<tr>
<td>48</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>GPIO[1]</td>
<td>I/O</td>
<td>Pull-up[^c]</td>
</tr>
<tr>
<td>50</td>
<td>nQ9</td>
<td>Output</td>
<td></td>
</tr>
</tbody>
</table>
Table 1. Pin Descriptions[a] (Cont.)

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>51</td>
<td>Q9</td>
<td>Output</td>
<td>Q9 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>52</td>
<td>VDDO_Q9</td>
<td>Power</td>
<td>Power supply for Q9/nQ9 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>53</td>
<td>nQ3</td>
<td>Output</td>
<td>Q3 clock negative output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>54</td>
<td>Q3</td>
<td>Output</td>
<td>Q3 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>55</td>
<td>VDDO_Q3</td>
<td>Power</td>
<td>Power supply for Q3/nQ3 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>56</td>
<td>GPIO[5]</td>
<td>I/O</td>
<td>General Purpose Input / Output 5 (see General Purpose Input/Outputs (GPIOs)).</td>
</tr>
<tr>
<td>57</td>
<td>nQ2</td>
<td>Output</td>
<td>Q2 clock negative output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>58</td>
<td>Q2</td>
<td>Output</td>
<td>Q2 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>59</td>
<td>VDDO_Q2</td>
<td>Power</td>
<td>Power supply for Q2/nQ2 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>60</td>
<td>VDDO_Q1</td>
<td>Power</td>
<td>Power supply for Q1/nQ1 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>61</td>
<td>Q1</td>
<td>Output</td>
<td>Q1 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>62</td>
<td>nQ1</td>
<td>Output</td>
<td>Q1 clock negative output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>63</td>
<td>GPIO[4]</td>
<td>I/O</td>
<td>General Purpose Input / Output 4 (see General Purpose Input/Outputs (GPIOs)).</td>
</tr>
<tr>
<td>64</td>
<td>nQ0</td>
<td>Output</td>
<td>Q0 clock negative output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>65</td>
<td>Q0</td>
<td>Output</td>
<td>Q0 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>66</td>
<td>VDDO_Q0</td>
<td>Power</td>
<td>Power supply for Q0/nQ0 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>67</td>
<td>VDD_A</td>
<td>Power</td>
<td>Power supply for FOD control logic for FOD_0, FOD_1, FOD_4, and FOD_5. Also powers FOD_0, FOD_1, and FOD_4. 1.8V supply required.</td>
</tr>
<tr>
<td>68</td>
<td>VDDO_Q8</td>
<td>Power</td>
<td>Power supply for Q8/nQ8 output buffers. For voltages supported, see FOD Multiplexing and Output Stages.</td>
</tr>
<tr>
<td>69</td>
<td>Q8</td>
<td>Output</td>
<td>Q8 clock positive output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>70</td>
<td>nQ8</td>
<td>Output</td>
<td>Q8 clock negative output (see FOD Multiplexing and Output Stages).</td>
</tr>
<tr>
<td>71</td>
<td>GPIO[0]</td>
<td>I/O</td>
<td>General Purpose Input / Output 0 (see General Purpose Input/Outputs (GPIOs)).</td>
</tr>
<tr>
<td>72</td>
<td>C_REG_XTAL</td>
<td>Power</td>
<td>Filter capacitor for voltage regulator for oscillator circuit associated with OSCI / OSCO pins. Requires a 10μF filter capacitor to ground.</td>
</tr>
<tr>
<td>ePAD</td>
<td>VSS</td>
<td>Power</td>
<td>Device ePAD must be connected to Ground.</td>
</tr>
</tbody>
</table>

[a] Pull-up and Pull-down refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

[b] VDDA_PDCP_XTAL and VDDA_LC_BG can be driven with either 2.5V or 3.3V, however both must use the same voltage level. Register programming is required to configure the device for either 2.5V or 3.3V operation. For more information, see the 8A3xxxx Family Programming Guide.

[c] GPIO pins may be configured via EEPROM and/or OTP with a pull-up or a pull-down. Pull-up is the default configuration.
### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C\text{IN}</td>
<td>Input Capacitance</td>
<td>OSCI, OSCO</td>
<td>9</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>XO_DPLL</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All Other pins</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R\text{PULLUP}</td>
<td>Input Pull-up Resistor</td>
<td>nCLK[3:0]</td>
<td>50</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R\text{PULLDOWN}</td>
<td>Input Pull-down Resistor</td>
<td>CLK[3:0]</td>
<td>50</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>C\text{PD}</td>
<td>Power Dissipation Capacitance (per output pair)</td>
<td>LVCMOS</td>
<td>V\text{DDO_Q}[a] = 3.465V</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 2.625V</td>
<td>8.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 1.89V</td>
<td>8.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 1.575V</td>
<td>9.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 1.26V</td>
<td>8.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential</td>
<td>V\text{DDO_Q} = 3.465V</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 2.625V</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V\text{DDO_Q} = 1.89V</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R\text{OUT}[b]</td>
<td>Output Impedance</td>
<td>GPIO[9,5:0]</td>
<td>V\text{DD_GPIO_FOD} = 1.8V</td>
<td>32</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SDIO, SCLK</td>
<td>V\text{DD_GPIO_FOD} = 1.8V</td>
<td>38</td>
<td></td>
</tr>
</tbody>
</table>

[a] V\text{DDO_Q} denotes: V\text{DDO_Q0}, V\text{DDO_Q1}, V\text{DDO_Q2}, V\text{DDO_Q3}, V\text{DDO_Q4}, V\text{DDO_Q5}, V\text{DDO_Q6}, V\text{DDO_Q7}, V\text{DDO_Q8}, V\text{DDO_Q9}, V\text{DDO_Q10}, or V\text{DDO_Q11}

[b] Output impedance values for the Qx / nQx outputs are provided in Table 35.
Overview of the 8A3xxxx Family

The 8A3xxxx family of devices have multiple channels that can operate independently from each other, or in combination with each other (combo mode). All devices share a common channel architecture (see Figure 3) with different functional blocks within the channel being available for use in different members of the family. In addition, there are other peripheral blocks that may only be available in specific family members. The number of channels and of certain peripheral blocks (such as extra serial ports) will also vary from one device in the family to another. Across all members of the family, numbering of the functional and peripheral blocks and their associated register locations are kept consistent to enhance software compatibility and portability between members of the family.

The remaining sub-sections of this Functional Description section will describe functions within the clocking channel and peripheral functions that are available in the 8A34044 only.

Figure 3. Single PLL Channel

Functional Description

This section describes the operational modes and associated functional blocks of the 8A34044. In addition, there are several other areas of the document that describe specific functions or details that would overly burden this document. Table 3 shows related documents.

Table 3. Related Documentation

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8A34044 Datasheet (This document)</td>
<td>Contains a functional overview of the device and hardware-design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.</td>
</tr>
<tr>
<td>8A34044&lt;Dash code&gt; Datasheet Addendum</td>
<td>Indicates pre-programmed power-up / reset configurations of this specific &quot;dash code&quot; part number.</td>
</tr>
<tr>
<td>8A3xxxx Family Programming Guide (v4.8)</td>
<td>Contains detailed register descriptions and address maps for all members of the family of devices. Please ensure to use the version indicated here for this product. The functionality described in this datasheet assumes that the device is running the update revision referred to here or a later one. For individual updates to determine differences between update revisions, see Release Note documents. Note that the device may not ship from the factory with the indicated update revision included in the device. If this is the case, the indicated revision may need to be loaded from an external EEPROM or over the serial port at each device reset.</td>
</tr>
</tbody>
</table>
Basic Functional Blocks of the 8A34044

Crystal Input (OSCI / OSCO)
The 8A34044 requires a 25MHz–54MHz crystal input on the OSCI/OSCO pins at all times. This input is used to drive the System APLL, which in turn is the source for all internal clocks. For more information, see Table 36 and Crystal Recommendation.

Alternatively, the crystal input can be overdriven by a crystal oscillator. For more information, see Overdriving the XTAL Interface.

Frequency Representation in 8A34044
The format for representing a frequency in the registers of the 8A34044 is:

\[ f = \frac{M}{N} \]

where \( M \) is a 48-bit integer and \( N \) is a 16-bit integer

M/N is a fraction that allows for the creation of non-integer frequencies

For example:

133.333333MHz = \( \frac{409}{3} \) MHz

System Analog PLL (APLL)
The System Analog Phase-Lock Loop (APLL) is shown in Figure 4. This consists of a simple analog PLL circuit that takes a reference crystal input and multiplies it up to a frequency in the 13.4GHz–13.9GHz range. That high-speed signal is then used to drive the Fractional Output Divider (FOD) circuits as described in FOD Multiplexing and Output Stages. This combination of the APLL and the FOD logic results in excellent phase noise performance and a substantial amount of flexibility in frequency and phase for the 8A34044.

One user programming option involves selecting whether the crystal reference frequency is to be used directly or run through an internal frequency doubler circuit first. An additional user programming option is to select the feedback divider value from the set of integers between 122 and 560. Between these two settings, the user should select an APLL operating frequency that is within the above-stated tuning range and also does not result in FOD divider ratios where the divide-ratio fraction is very close to 1, 0, or 1/2.

Figure 4. System Analog PLL Channel

During a device reset, the APLL is configured by loading the appropriate control register fields from the internal One-Time Programmable memory or an external serial EEPROM, whichever is enabled and has valid contents. After the reset sequence has completed, the APLL can be re-configured manually over the serial port at any time.

The System APLL is considered locked when the Loop Filter control voltage is within specified limits for the configuration selected. The 8A34044 automatically calculates these limits based on other parameters specified in the device configuration. Specific user input to set locking limits is not required. A System APLL Loss-Of-Lock alarm is generated internally. This can be read from internal status registers and/or used to drive a GPIO status signal as described in GPIO Modes.
Input Stage

The 8A34044 contains multiple input stages. An input stage can be configured as one differential or dual single-ended inputs. Some of the input stages can also be configured to support one differential plus one single-ended clock. For information on how to connect various input types to the 8A34044, see Table 4 and Applications Information.

Table 4. Input Stage Setting

<table>
<thead>
<tr>
<th>Input Protocol</th>
<th>Driver V&lt;sub&gt;DD&lt;/sub&gt; Level</th>
<th>V&lt;sub&gt;DD_CLK&lt;/sub&gt;Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>3.3V</td>
</tr>
<tr>
<td>PECL</td>
<td>3.3V</td>
<td>Differential + NMOS</td>
</tr>
<tr>
<td>PECL</td>
<td>2.5V</td>
<td>Differential + PMOS</td>
</tr>
<tr>
<td>LVDS</td>
<td>N/A</td>
<td>Differential + NMOS</td>
</tr>
<tr>
<td>HCSL</td>
<td>N/A</td>
<td>Differential + PMOS</td>
</tr>
<tr>
<td>CML</td>
<td>3.3V</td>
<td>Differential + NMOS</td>
</tr>
<tr>
<td>CML</td>
<td>2.5V</td>
<td>Differential + NMOS</td>
</tr>
<tr>
<td>CML</td>
<td>1.8V</td>
<td>Differential + NMOS</td>
</tr>
<tr>
<td>CMOS</td>
<td>3.3V</td>
<td>Single-ended</td>
</tr>
<tr>
<td>CMOS</td>
<td>2.5V</td>
<td></td>
</tr>
<tr>
<td>CMOS</td>
<td>1.8V</td>
<td></td>
</tr>
</tbody>
</table>

When programmed as differential only, as shown in Figure 5, the internal signal will be referred to by the index number of the input pins (e.g., CLK0 is used to refer to the differential input pair CLK0/nCLK0). It is also necessary to select the appropriate mode, PMOS or NMOS so the input buffer will work best with the incoming signal’s voltage swing.

The 8A34044 supports input frequencies up to 1GHz for differential inputs. If the input reference clock frequency is higher than 150MHz, then it must be divided down to the internal frequency (less than or equal to 150MHz) used by the DPLL. An integer divider with a range between 2 to 15 is provided to divide the signal down to less than or equal to 150MHz. For input reference clock frequencies less than 150MHz, the internal divider can be bypassed.

The 8A34044 has the option to lock to the rising or falling edge of the input clock signal by selecting the inverted input path to the divider.

Figure 5. Input Stage Configured as Differential Only
When programmed as dual single-ended as shown in Figure 6, two independent inputs are provided to the 8A34044. The input clock originating from the positive input will be referred to by using the same index number (e.g., CLK0 is used to refer to the signal originating from CLK0). The signal originating from the negative input will be referred to by using the index + 8 (e.g., CLK8 is used to refer to the signal originating from nCLK0). Note that this numbering scheme remains the same on all 8A3xxxx family members, regardless of the number of actual input pins. This is to simplify software portability between family members. PMOS versus NMOS mode does not have any effect for single-ended inputs.

The 8A34044 supports input frequencies up to 250MHz for single-ended inputs. If the input reference clock frequency is higher than 150MHz, then it needs to be divided down to the internal frequency (less or equal to 150MHz) used by the DPLL with the dividers shown in each path. For input reference clock frequencies less than 150MHz, the internal divider can be bypassed.

The 8A34044 has the option to lock to the rising or falling edge of the input clock signal for either path independently.

Figure 6. Input Stage Configured as Dual Single-Ended

When programmed as differential plus one single-ended as shown in Figure 7, two independent inputs are provided to the 8A34044. This mode can only be used with the GPIOs and input stages shown in the following table.

Table 5. Input Stages Using GPIOs as Reference Clock Inputs

<table>
<thead>
<tr>
<th>Differential Clock Input</th>
<th>Mapped to Internal Clock</th>
<th>GPIO Input</th>
<th>Mapped to Internal Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK0 / nCLK0</td>
<td>CLK[0]</td>
<td>GPIO[0]</td>
<td>CLK[8]</td>
</tr>
<tr>
<td>CLK1 / nCLK1</td>
<td>CLK[1]</td>
<td>-</td>
<td>CLK[9]</td>
</tr>
</tbody>
</table>

Input stages not shown in this table can be used in the differential only mode or dual single-ended mode only. The differential input clock originating from the positive input will be referred to the same way as in differential only mode. The signal originating from the GPIO input will be referred to by using the index shown in the table. Note that this numbering scheme remains the same on all 8A3xxxx family members, regardless of the number of actual input pins. This is to simplify software portability between family members. PMOS versus NMOS mode does not have any effect for GPIO inputs.

The 8A34044 supports input frequencies up to 150MHz for GPIO inputs, so no division is necessary. If the input reference clock frequency from the differential input path is higher than 150MHz, then it needs to be divided down to the internal frequency (less or equal to 150MHz) used by the DPLL with the divider shown in its path. For input reference clock frequencies less than 150MHz, the internal divider may be bypassed.

The 8A34044 has the option to lock to the rising or falling edge of the input clock signal for either path individually.
In addition to the above, there are a number of other configuration bits that can be used for the input stage.

- Unused inputs can be disabled. This allows a small amount of power saving and eliminates a source of on-die noise.
- Any input can be used either as a sync or frame pulse associated with an input clock (for more information, see Frame Pulse Operation and Sync Pulse Operation).
- The frequency of each input needs to be known by the 8A34044 and so must be programmed in the registers for each active input stage.

**Reference Monitoring**

The quality of all input clocks is always monitored for:

- LOS (loss of signal)
- Activity
- Frequency

All input clocks are monitored all the time, including the active reference to ensure that it is still a valid reference. If any monitor detects a failure of the input clock, it will generate an internal alarm. An input clock with an alarm condition is not used for synchronization unless configured to allow it to be considered qualified in spite of the alarm.

For information on how these internal alarms can be signaled and monitored by outside resources, see Alarm Output Operation.

**Loss of Signal (LOS) Monitoring**

Each input clock is monitored for loss of signal (LOS). The LOS reference monitor supports normal clock operation and gapped clock operation. In normal operation, the user can specify whether the alarm condition should be tight to the expected clock period or loose. Tight monitoring will give minimum response time for loss of the input clock, but may result in false alarms due to normal clock jitter or wander. The loose threshold will take longer to detect an alarm condition but is unlikely to give false alarms. For clocks greater than 500kHz, both loose and tight specifications check for the clock edge being outside ±20ns of the expected position to declare an alarm. For clocks less than or equal to 500kHz, loose threshold is set at ±25% of the nominal edge position and tight is set to ±1%.
In gapped clock operation, LOS is declared if the clock reference misses consecutive clock cycles. It is cleared once an active clock edge is detected. The number of consecutive clocks that are missed to declare LOS is programmable according to Table 6. A setting of 01 is equivalent to a normal clock monitor.

**Table 6. Gapped Clock LOS Settings**

<table>
<thead>
<tr>
<th>LOS[1:0]</th>
<th>Number of Consecutive Clocks Missed to Declare LOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Gapped Clock Monitoring Disabled (default)</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>5</td>
</tr>
</tbody>
</table>

There is a status register for LOS. LOS failure alarm will be set as described above. What actions are taken in the event of an alarm can be configured via registers. The LOS failure can cause a specific alarm on a GPIO and/or be used as one input to an Alert (aggregated alarm) output via GPIO if so configured.

**Activity**

All input reference clocks higher than 1kHz can be monitored for activity. Activity monitoring can quickly determine if a clock is within the frequency limits shown in Table 7. The method used by this monitor is not as precise as the Frequency Offset Monitor, but results are available much more quickly.

**Table 7. Activity Limit**

<table>
<thead>
<tr>
<th>Activity_Limit[2:0]</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>±1000ppm</td>
</tr>
<tr>
<td>001</td>
<td>±260ppm</td>
</tr>
<tr>
<td>010</td>
<td>±130ppm</td>
</tr>
<tr>
<td>011</td>
<td>±83ppm</td>
</tr>
<tr>
<td>100</td>
<td>±65ppm</td>
</tr>
<tr>
<td>101</td>
<td>±52ppm</td>
</tr>
<tr>
<td>110</td>
<td>±18ppm</td>
</tr>
<tr>
<td>111</td>
<td>±12ppm</td>
</tr>
</tbody>
</table>

An activity failure alarm will be set if the input frequency has drifted outside the range set by the programmable range for longer than 1.25ms. What actions are taken in the event of an alarm can be configured via registers. The Activity failure can cause a specific alarm on a GPIO and/or be used as one input to an Alert (aggregated alarm) output via GPIO if so configured.
There is a timer associated with the activity qualification and disqualification of each input reference. After an activity or LOS alarm is detected, then the timer starts. If the Activity or LOS alarm remains active for the full duration of the timer, then the reference disqualification alarm will be set to high. Register bits can be used to configure whether or not either the alarm is allowed to affect the disqualification decision or not. The disqualification timer can be selected according to Table 8.

Table 8. Disqualification Timer

<table>
<thead>
<tr>
<th>CLKn_Disqualification Timer[1:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>2.5s (default)</td>
</tr>
<tr>
<td>01</td>
<td>1.25ms</td>
</tr>
<tr>
<td>10</td>
<td>25ms</td>
</tr>
<tr>
<td>11</td>
<td>50ms</td>
</tr>
</tbody>
</table>

After a reference is disqualified, once it returns (all alarms now clear), then a qualification timer is started. If the alarms remain cleared for the full duration selected, then the input is qualified for use again. Qualification timer settings are shown in Table 9.

Table 9. Qualification Timer

<table>
<thead>
<tr>
<th>CLKn_Qualification Timer[1:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>4 times the Disqualification timer</td>
</tr>
<tr>
<td>01</td>
<td>2 times the Disqualification timer</td>
</tr>
<tr>
<td>10</td>
<td>8 times the Disqualification timer</td>
</tr>
<tr>
<td>11</td>
<td>16 times the Disqualification timer</td>
</tr>
</tbody>
</table>

Frequency Offset Monitoring

Each input reference is monitored for frequency offset failures. The device measures the input frequency and an alarm is raised if the input frequency exceeds the rejection range limit set as per Table 10. To avoid having the alarm toggling in case an input clock frequency is on the edge of the frequency range, a separate, narrower acceptance range must be met before the alarm will clear. The acceptance ranges are also listed in Table 10.

Table 10. Frequency Offset Limits

<table>
<thead>
<tr>
<th>Frequency_Offset_Limit[2:0]</th>
<th>Acceptance Range</th>
<th>Rejection Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>±9.2 ppm</td>
<td>±12 ppm</td>
<td>Stratum 3, Stratum 3E, G.8262 option 2</td>
</tr>
<tr>
<td>001</td>
<td>±13.8 ppm</td>
<td>±18 ppm</td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>±24.5 ppm</td>
<td>±32 ppm</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>±36.6 ppm</td>
<td>±47.5 ppm</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>±40 ppm</td>
<td>±52 ppm</td>
<td>SONET Minimum clock. G.813 option 2</td>
</tr>
<tr>
<td>101</td>
<td>±52 ppm</td>
<td>±67.5 ppm</td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>±64 ppm</td>
<td>±83 ppm</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>±100 ppm</td>
<td>±130 ppm</td>
<td></td>
</tr>
</tbody>
</table>
Advanced Input Clock Qualification

In addition to the Input Clock Selection and Qualification functions mentioned earlier, the following modes are also available.

Input Clock Qualification

For each DPLL the following conditions must be met for the input clock to be valid; otherwise, it is invalid:

- No reference monitor alarms are asserted for that input clock (unless register settings allow the alarms not to affect the decision)
- GPIO used to disqualify that input reference clock is not asserted

Clock Reference Disqualifier through GPIO

GPIO pins can be used to disqualify any input reference clock. If a GPIO is programmed to disqualify a particular input clock, then if that pin is asserted, the corresponding input reference clock will not be available for the DPLL to lock to. For example, a GPIO can be configured as an input to the 8A34044 and connected to a Loss of Signal (LOS) output coming from a PHY device that is providing a recovered clock to one of the DPLLs. If the LOS from the PHY is active, then the DPLL will disqualify that input clock and it will not be available to be locked to. If the disqualified input was the active input for the DPLL, then a switchover process will be triggered if any other valid inputs are available.

Frame Pulse Operation

In frame pulse operation, two clock signals are working together to signal alignment to a remote receiver. A higher frequency clock is providing a phase aligned reference. A second clock signal (frame signal) is running at a lower, but integer-related rate to the higher frequency clock. The active edge of the frame pulse indicates that the next rising edge of the associated higher frequency clock is to be used as an alignment edge. The 8A34044 supports either rising or falling edges on a frame pulse. The frame signal is usually implemented as a pulse rather than a square wave clock.

Any input clock and any output clock can be used as frame signal input and output respectively. This is accomplished by configuring the appropriate bits in control registers. An EPPS (even pulse per second), 1PPS, 5PPS, 10PPS, 50Hz, 100Hz, 1kHz, 2kHz, 4kHz, or 8kHz frame input signal can be used with an associated input clock to align a frame output signal and align associated output and frame clock. The frame pulse does not require any specific duty cycle but should have a pulse width of at least 10nsec.

The maximum frequency for the associated input clock is 150MHz, and it can be associated with any supported frame pulse frequency for the frame signal input as long as the integer frequency relationship is maintained. The frame output frequencies are independent of the frame input frequencies; however, the output associated clock and output frame signal must have an integer relationship in order to be aligned.

The frame pulse and clock output coming out of the same DPLL are aligned with the first rising edge of the input clock which follows the input frame pulse used by the same DPLL. The 8A34044 allows several different pulse widths to be selected (see Table 16).

When the frame input signal is enabled to synchronize the frame output signal, the output will be adjusted to align itself with the DPLLS selected input clock (associated with the input frame signal) within the input-output alignment limits indicated in AC Electrical Characteristics.

By default, the rising edge of the frame input signal identifies the rising edge of the DPLL’s selected input clock. The falling edge of the frame input signal can be used to identify the rising edge of the DPLL’s selected input clock by setting the frame pulse configuration register.

An example of the frame pulse operation is provided in Figure 8.
In Figure 8, CLKx is the associated input clock and CLKy is the frame pulse, and they are both input to DPLLn. Qx is the output clock that is locked to CLKx, and Qy is the output frame pulse output of DPLLn.

**Sync Pulse Operation**

A sync pulse scenario occurs similarly to a frame pulse scenario, except that it is the rising edge of the sync signal that is used as the alignment edge rather than an edge of the associated clock.

Any input clock and any output clock can be used as sync signal input and output respectively, which is done by configuring the appropriate bits in control registers. An EPPS (even pulse per second), 1PPS, 5PPS, 10PPS, 50Hz, 100Hz, 1kHz, 2kHz, 4kHz, or 8kHz sync input signal can be used with an associated input clock to align a sync output signal and output clocks. The sync pulse does not require any specific duty cycle but should have a pulse width of at least 10nsec.

The maximum frequency for the associated input clock is 1GHz, and it can be associated with any supported frequency for the sync signal input as long as it is an integer multiple of the sync signal frequency. The sync output frequencies should be an integer relationship of the sync input frequencies.

By default, the sync pulse and clocks output coming out of the same DPLL are aligned with the first rising edge of the sync pulse used by the same DPLL. The falling edge of the sync input signal can be used by setting the frame pulse configuration register.

An example of the sync pulse operation is provided in Figure 9.

In Figure 9, CLKx is the associated input clock and CLKy is the sync pulse, and they are both input to DPLLn. Qx is the output clock that is locked to CLKx, and Qy is the output sync pulse output of DPLLn.
Crystal Oscillator Input (XO_DPLL)

There is one additional reference clock input that is available: XO_DPLL. This is a single-ended (LVCMOS) input that is intended to be used to provide a stable frequency reference, such as an XO, TCXO or OCXO to the System DPLL. This input is not required in all cases. The crystal oscillator should be chosen accordingly to meet different applications and standard requirements (see application note, AN-807 Recommended Crystal Oscillators for NetSynchro WAN PLL).

Please note that there is no reference monitoring function on the XO_DPLL input. Failures of this input cannot be detected directly. Since the XO_DPLL input is usually used to drive the SysDPLL which in turn provides a reference clock to the reference monitors for all other input clocks, a simultaneous failure of all monitored input clocks could be inferred to be a failure of the XO_DPLL input in that case.

Digital Phase Locked Loop (DPLL)

All DPLLs and the system DPLL within the 8A34044 are exactly the same. The only difference with the System DPLL channel is that it is not connected directly to any output stages. One channel of the DPLL is shown in Figure 10.

Figure 10. DPLL Channel

The DPLL operating mode operation can be set to automatic, forced locked, forced free-run, and forced holdover. The operating mode can be controlled by setting the appropriated bits in the DPLL mode register. When the DPLL is set to automatic then an internal state machine will control the states automatically. The automatic state machine is displayed in Figure 11.
In Figure 11, the changes of state are based on the following:

1. Reset, the device enters Free-Run State.
2. Once an input clock is qualified and it is selected: enter the LockAcq State.
3. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Free-Run State.
4. DPLL switches to another qualified clock: remain in LockAcq State.
5. The DPLL locks to the selected input clock: enter Locked State.
6. The DPLL selected input clock is disqualified AND No qualified input clock is available: enter Holdover State.
7. A qualified input clock is now available: enter LockRec State.
8. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Holdover State.
9. The DPLL switches to another qualified clock: enter LockRec State.
10. The DPLL locks to the selected input clock: go to Locked State.
11. The DPLL switches to another qualified clock: remain in LockRec State

In items 4, 9, and 11, the DPLL switches to another qualified clock due to the selected input clock being disqualified, or the device is set to revertive mode and a qualified input clock with a higher priority becomes valid, or the device is set to Forced selection to another input clock.
**Free-Run Mode**

In Free-Run mode, the DPLL synthesizes clocks based on the system clock (crystal oscillator) and has no influence from a current or a previous input clock.

Combo mode can be used with Free-Run mode. In this case, the input clock of the combo master affects the combo slave’s free-Run frequency. For more information, see **Combo Mode**.

**Locked Mode**

In Locked mode, the DPLL is synchronized to an input clock. The frequency and phase of the output clock track the DPLL selected input clock. The bandwidth (BW) and damping factor are programmable and are used by the DPLL when locked to an input reference. The following table includes some common bandwidth settings and their associated applications.

**Table 11. DPLL Bandwidth**

<table>
<thead>
<tr>
<th>DPLL Bandwidth</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25Hz</td>
<td>Jitter attenuators and Clock generators (General)</td>
</tr>
<tr>
<td>100Hz</td>
<td>G.8251 (OTN 1G)</td>
</tr>
<tr>
<td>300Hz</td>
<td>G.8251 (OTN)</td>
</tr>
<tr>
<td>1kHz</td>
<td>Jitter attenuators and Clock generators (100G)</td>
</tr>
<tr>
<td>10kHz</td>
<td>Jitter attenuators and Clock generators (10G)</td>
</tr>
<tr>
<td>12kHz</td>
<td>Jitter attenuators and Clock generators (1G/SONET/SDH)</td>
</tr>
</tbody>
</table>

**Holdover Mode**

If all the input clocks for a particular DPLL become invalid, then the DPLL will enter holdover state.

In holdover mode, the DPLL uses stored frequency data acquired in Locked mode to control its output clocks. There are several programmable modes for the frequency offset acquisition method; it can use the frequency offset just before it entered holdover state (simple holdover), or a previously stored post-filtered frequency offset (advanced holdover).

For the advanced holdover mode, the holdover value can be post filtered and is stored in two registers at a programmable rate while the DPLL is in locked state. When the DPLL enters the advanced holdover mode, the oldest register value is restored into the integrator inside the DPLL. The rate at which the holdover registers are updated is programmable between 0s and 63s in steps of 1s.

**Note:** To establish an accurate holdover value for the advanced holdover mode, a stable estimate of the average input reference frequency is necessary before entering holdover. Therefore, the DPLL must have been in the locked state for a period that is based on the holdover settings (e.g., the lower the bandwidth setting for the holdover filter, the longer it takes to acquire the accurate holdover value).

The DPLL can also be forced into the holdover mode. If the forced holdover mode is used, then the DPLL will stay in holdover even if there are valid references available for the DPLL to lock to.

**Manual Holdover Mode**

In Manual Holdover mode, the DPLL state machine is forced into the Holdover state but the frequency offset is set by the DPLL manual holdover value register bits under user control.
External Feedback

The 8A34044 supports the use of an external feedback path, where one of the channel’s output clocks is externally connected to one of the reference clock inputs as shown in Figure 12. External feedback automatically maintains tight alignment of the output phase with the reference input phase. This alignment is done by dynamically compensating for changes in PCB trace delay and external buffer propagation delay caused by changes in temperature and voltage. Use of the external feedback path is referred to as a zero delay phase locked loop (ZDPLL), where output frequencies are different to the reference clock input, or a zero delay buffer (ZDB), where all output frequencies are the same as the reference clock input.

Figure 12. External Feedback

For both ZDPLL and ZDB, the frequency of the external feedback clock must be the same as the reference clock input. For this reason, all of the reference clock inputs must be the same frequency when using automatic reference switching. Otherwise, the external feedback clock must be reconfigured to match the new input reference clock frequency prior to manually switching to the new reference.

For more information about this feature, see EXT_FB_EN and EXT_FB_REF_SELECT in the 8A3xxx Family Programming Guide.

DPLL Input Clock Qualification and Selection

Any Digital PLL (DPLL) can use any of the inputs as its reference. Several options exist to control how the DPLL selects which input to use at any moment in time. Whether a particular input is qualified for use at any time is based on the reference monitors. The DPLL_REF_MODE registers allow the DPLL to be set in any of the modes shown in Table 12. There is an independent reference selection process for each DPLL.

Table 12. DPLL Reference Mode

<table>
<thead>
<tr>
<th>DPLL_ref_mode[3:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Automatic input clock selection</td>
</tr>
<tr>
<td>0001</td>
<td>Manual input clock selection</td>
</tr>
<tr>
<td>0010</td>
<td>GPIO</td>
</tr>
<tr>
<td>0011</td>
<td>Slave</td>
</tr>
<tr>
<td>0100</td>
<td>GPIO_Slave</td>
</tr>
<tr>
<td>0101–1111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Automatic Input Clock Selection

If automatic input clock selection is used then the input clock selection is determined by the input clock being valid, the priority of each input clock, and the input clock configuration.

Each input can be enabled or disabled by setting register bits. If the input is enabled and reference monitors declare that input valid, then that input is qualified to be used by the DPLL. Within all the qualified inputs, the one with the highest priority is selected by the DPLL. The input clock priority is set by setting the appropriate bits in the DPLL_REF_PRIORITY registers. If a user wanted to designate several inputs as having the same priority, then an additional table allows several outputs to be placed in a group of equal priority.

Manual Input Clock Selection via Register or GPIO

If manual input clock selection is chosen then the DPLL will lock to the input clock indicated by register bits or by selected GPIO pins. The results of input reference monitoring do not affect the clock selection in manual selection mode. If the DPLL is locked to an input clock that becomes invalid, then the DPLL will go into holdover mode even in the case where there are other input clocks that are valid.

Slave or GPIO Slave Selection

This mode of clock selection is used when the 8A34044 is acting as an inactive, redundant clock source to another timing device. The other device is the master and this device is the slave. When Slave mode is selected via registers, a specific input (from the master timing device) is also indicated. That input and only that input is used in this mode. GPIO Slave mode involves the same configuration settings as if the part were a master, but a GPIO input is used to tell this device that it is now the slave and to switch to and monitor the designated input only.

DPLL Switchover Management

Revertive and Non-Revertive Switching

All DPLLs support revertive and non-revertive switching, with the default being non-revertive. During the reference selection process, a DPLL selects the valid reference with the highest priority then the DPLL locks to that input clock. In the case of non-revertive switching, the DPLL only switches to another, higher priority reference if the current reference becomes invalid. Non-revertive switching minimizes the amount of reference switches and therefore is the recommended mode.

If revertive switching is enabled and a higher priority clock becomes valid, then the DPLL will switch to that higher priority input clock unless that clock is designated as part of the same group (i.e., should be considered of equal priority).

Hitless Reference Switching

All DPLLs support Hitless Reference Switching (HS). HS is intended to minimize the phase change on the output clock when switching between input sources that may have different phases. When a DPLL switches input with HS enabled, it will first go into an internal holdover state (but not assert a holdover alarm either internally or externally), then the phase offset of the newly selected input clock with respect to the previous clock will be measured. The device then automatically compensates for the measured phase offset resulting in minimal disruption to the phase of the DPLL output clock.

The HS operation for a particular DPLL is triggered if either of the following conditions occurs:
- DPLL is locked to an input clock and switches to a different input clock
- DPLL exits from Holdover mode
- There are several additional cases where hitless reference switching can be used in synchronization applications with physical and/or packet clocks. For more information relevant to the particular application, please contact IDT.

For the two conditions, the maximum phase transient on the DPLL output clock with HS on is indicated in Table 38. Hitless reference switching can be enabled or disabled through register settings.

For 1PPS input clocks, if they have up to 100μs of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock with HS on is indicated in Table 38. If they have between 100μs and 0.5s of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock will be larger.
Phase Slope Limiting

Phase Slope Limiting (PSL) can be enabled and independently programmed for each of the DPLLS. PSL is particularly useful in the initial locking to an input or during switchover between clock inputs. If PSL is enabled then the rate of change of phase of the output clock is limited by the DPLL. The PSL settings for the device are very flexible, allowing any slope from 1ns/s to 65.536μs/s with a granularity of 1ns/s, including the values needed to meet Telecom standards as displayed in Table 13.

Table 13. Some Key DPLL Phase-Slope Limits Supported

<table>
<thead>
<tr>
<th>DPLL PSL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unlimited</td>
<td>Limited by DPLL loop bandwidth setting</td>
</tr>
<tr>
<td>61 μs/s</td>
<td>Telcordia GR-1244 ST3</td>
</tr>
<tr>
<td>7.5 μs/s</td>
<td>G.8262 EEC option 1, G.813 SEC option 1</td>
</tr>
<tr>
<td>885 ns/s</td>
<td>Telcordia GR-1244 ST2, ST3E, and ST3 (objective)</td>
</tr>
</tbody>
</table>

DPLL Frequency Offset Limit Setting

Each DPLL has an independent setting to limit its maximum frequency range. This setting is used in conjunction with the advanced reference monitoring to provide pull-in / hold-in limit enforcement as required in many telecom standards. It will also limit the frequency deviation during locking, during holdover, and while performing switchovers. This limit must be set wide enough to cover the expected frequency range of the input when locking.

DPLL Fast Lock Operation

Each DPLL also supports a Fast Lock function. There are four options the user can choose from to perform the fast lock:

- Frequency Snap
- Phase Snap
- Open-loop phase pull-in (mutually exclusive with Phase Snap)
- Wide Acquisition Bandwidth

Any of the options can be independently enabled or disabled, and selected to be applied when the DPLL is in either the LOCKACQ state or the LOCKREC state. Although the options are mutually exclusive, the order of precedence is as listed (with frequency snap being the highest).

The frequency and phase snap options are recommended for locking to mid-kHz-range input clocks or lower. For frequency snap, the 8A34044 will measure the input clock from the current DPLL operating frequency, determine an approximate frequency offset, and digitally write that directly to the steerable FOD block, causing the output frequency to snap directly to the correct output frequency. The frequency snap can be optionally limited using a Frequency Slope Limit (FSL). For the phase snap and the open loop phase pull-in options, the measurement is used to determine the phase offset. With phase snap, the phase is snapped to the correct value; with open loop pull-in, the DPLL’s PFD and LPF are temporarily isolated to allow for an unfiltered phase pull-in to the correct value. The combination of these methods will achieve lock very quickly, but there may be severe disruptions on the output clock while locking occurs; mainly due to the frequency/phase snaps.

The wide acquisition bandwidth option uses the DPLL in a normal operating mode, but with temporary relaxation of items like DPLL loop bandwidth, phase slope limits (PSL), or damping factor until lock is achieved. At that point, the normal DPLL limits are resumed. The user can control what limits are to be applied. In addition, for LOCKACQ state only, the DPLL’s bandwidth may be temporarily opened to its maximum for a short duration of time (in ms), with the temporary phase slope limit still being applied. This pre-acquisition option is applied before the wide acquisition bandwidth option. These methods are recommended for higher frequency signals since it results in fewer perturbations on the output clock. It also allows the user to trade-off the level of changes on the clock during the locking process versus the speed of locking.
Satellite Channel

A satellite channel has simplified functionality in the 8A34044. It does not support locking to input references, and therefore, does not have a DPLL state machine or associated switchover management logic. It has the same steerable fractional output divider and output stage, and can be steered by other channels or external inputs as the DPLL channels (see Figure 13). As a result, a satellite channel can be used independently as a Frequency Synthesizer or Clock Generator, with external input (using Write Frequency and Write Phase modes) as a Digitally-Controlled Oscillator (DCO), and in conjunction with a DPLL channel as additional outputs, including frequency translation capability.

Figure 13. Satellite Channel Block Diagram

Steerable Fractional Output Divider (FOD)

The 8A34044 has multiple Steerable Fractional Divider blocks as shown in Figure 14. Each block receives a high-frequency, low-jitter clock from the System Analog PLL (APLL). It then divides that by a fixed-point (non-integer) divide ratio to produce a low-jitter output clock that is passed to the output stage(s) for further division and/or adjustment and also to the DPLL feedback dividers. The FOD output will be in the frequency range of 500MHz to 1GHz, and is independent of the output frequencies from any other FOD and from the System APLL.

Figure 14. Steerable Fractional Divider Block
The output frequency is determined by dividing the APLL frequency \( f_{\text{APLL}} \) by the Fractional Divider. Since \( f_{\text{APLL}} \) is between 13.4GHz and 13.9GHz and the FOD output \( f_{\text{FOD}} \) is between 500MHz and 1GHz, there is a limited range of valid FOD divide ratios (from 13.4 to 27.8). The Fractional Divider involves two unsigned integer values, representing the integer (INT) and fraction (FRAC) portion of the divide ratio. The fraction portion is an integer representing the 43-bit numerator of a fraction, where the denominator of that fraction is fixed at \( 2^{43} \).

IDT’s Timing Commander Software can be used to determine if a particular output frequency can be represented accurately, and if not, the magnitude of the inaccuracy. If additional information is required, please contact IDT directly.

The equation for the FOD output frequency is as follows.

\[
 f_{\text{FOD}} = \frac{f_{\text{APLL}}}{(\text{INT} + \frac{\text{FRAC}}{2^{43}})}
\]

**Note:** Fractions that approach 0, 1, or 1/2 can result in increased phase noise on the output signal due to integer-boundary spurs. It is recommended that APLL frequency and FOD divider settings be coordinated to avoid such fractions.

Fine adjustments in the phase of the FOD output may also be made. A phase adjustment is performed by increasing or decreasing the frequency of operation of the FOD for a period of time. This results in the clock edges of the FOD output clock being advanced (increased FOD output frequency will move edges to the left as seen on an oscilloscope relative to some fixed reference point) or delayed (decreased FOD output frequency moves edges to the right) by some amount. The user writes a signed integer value to the fine adjust register of the FOD over the serial port. This value represents the number of picoseconds the clock edges are to be advanced (negative value) or delayed (positive value). The user can also specify a rate of phase change as Fast, Medium, or Slow. A Fast setting will apply a larger frequency change for a shorter period of time, whereas a Slow setting will apply a smaller frequency change for a longer period. Medium will choose an intermediate frequency and duration. This setting is used to accommodate devices on the output clocks that may not be able to track a fast phase change. Any number of phase changes may be applied, so the range of phase change is effectively infinite.

Note that this method of fine phase adjustment should only be used when the FOD is operating in an open-loop manner. If the FOD is being used as part of a closed-loop control, where the output phase is observed and used to track a reference input, the feedback loop may act to remove the phase adjustment. If the FOD is part of a closed-loop operation, then it is recommended that phase or frequency adjustment be performed via the Digital Phase Locked Loop (DPLL) logic.

### FOD Multiplexing and Output Stages

The 8A34044 has multiple output stages that are associated with the FODs and output pins as shown in the following table.

**Table 14. FOD to Output Stage to Output Pin Mappings**

<table>
<thead>
<tr>
<th>Output Stage</th>
<th>Single / Dual</th>
<th>Output Pins</th>
<th>FODs that can Drive this Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Dual</td>
<td>Q0 / nQ0, Q1 / nQ1</td>
<td>FOD_0</td>
</tr>
<tr>
<td>1</td>
<td>Dual</td>
<td>Q2 / nQ2, Q3 / nQ3</td>
<td>FOD_1</td>
</tr>
<tr>
<td>2</td>
<td>Dual</td>
<td>Q4 / nQ4, Q5 / nQ5</td>
<td>FOD_2</td>
</tr>
<tr>
<td>3</td>
<td>Dual</td>
<td>Q6 / nQ6, Q7 / nQ7</td>
<td>FOD_3</td>
</tr>
<tr>
<td>4</td>
<td>Single</td>
<td>Q8 / nQ8</td>
<td>FOD_4, FOD_5</td>
</tr>
<tr>
<td>5</td>
<td>Single</td>
<td>Q9 / nQ9</td>
<td>FOD_5</td>
</tr>
<tr>
<td>6</td>
<td>Single</td>
<td>Q10 / nQ10</td>
<td>FOD_6</td>
</tr>
<tr>
<td>7</td>
<td>Single</td>
<td>Q11 / nQ11</td>
<td>FOD_6, FOD_7</td>
</tr>
</tbody>
</table>

The single output stages are shown in Figure 15 and the dual output stages are shown in Figure 16.
Other than having two copies of each functional block fed from the same FOD, both single and dual output stages behave the same. Similarly, the two paths within the dual output stages behave the same as each other. Descriptions of each functional block are provided in the following sub-sections.

**Integer Output Divider**

The integer output divider takes a clock signal from the FOD stage ranging from 500MHz to 1GHz and divides it by a 32-bit integer value. This results in output frequencies that range from 1GHz down to less than 0.5Hz, depending on the frequency coming from the FOD. For information on which FOD can be used with which output stage / output pins, see the previous table.
Output Duty Cycle Adjustment

The 8A34044 also has a number of options for generating pulses with different duty cycles. While these are intended primarily for frame pulses or sync pulses, duty cycle adjustment options remain accessible in all modes of operation.

As described in the previous section, each output is a divided down clock from the FOD. By default, this resulting clock will be a 50/50 duty cycle clock. If a pulse, such as a frame or sync pulse, is to be derived from the resulting clock, then the high pulse width can be programmed by a 32-bit integer value, representing the number of FOD clock cycles in the high period. This value must be less than the integer output divider value. Several examples are shown in Table 16.

Table 16. Output Duty Cycle Examples

<table>
<thead>
<tr>
<th>FOD_n Frequency</th>
<th>Integer Output Divider Register Value</th>
<th>Output Frequency</th>
<th>Output Duty Cycle High Register Value[a]</th>
<th>Resulting Pulse width</th>
</tr>
</thead>
<tbody>
<tr>
<td>500MHz</td>
<td>2</td>
<td>250MHz</td>
<td>0</td>
<td>2ns (50% / 50%)[b]</td>
</tr>
<tr>
<td></td>
<td>500,000,000</td>
<td>1Hz (1PPS)</td>
<td>500</td>
<td>1µs[c]</td>
</tr>
<tr>
<td>655.36MHz</td>
<td>80</td>
<td>8.192MHz</td>
<td>0</td>
<td>61.035ns (50% / 50%)</td>
</tr>
<tr>
<td></td>
<td>81920</td>
<td>8kHz</td>
<td>80</td>
<td>122ns (1UI[d])</td>
</tr>
</tbody>
</table>

[a] Pulses are always created by this logic as high-going pulses. If a low-going pulse is desired, the nQx output pin can be used with the inverter option selected.
[b] For precision of duty cycle achieved, see Table 38.
[c] This represents the high period of a pulse.
[d] The UI method of specifying a pulse width is often used for generation of a frame pulse. A frame pulse is always associated with another regular clock, so UI = Unit Interval of the clock output associated with the frame pulse. In this example, the associated clock is the 8.192MHz clock.

Output Coarse Phase Adjustment

The 8A34044 supports two methods for adjustment of the phase of an output clock. Fine phase adjustment can be performed in the Digital Phase Locked Loop (DPLL) block, so it can only be adjusted per-channel. In addition, coarse phase adjustment can be performed in the Output Stage and so can be performed on a per-output basis. Coarse adjust will move an output edge in units of the period of the FOD clock (T_FOD). Subject to the following rules, an infinite adjustment range is possible and the clock edge can be either advanced or delayed. Note that if an output phase adjustment is needed for a signal that does not meet these rules, fine phase adjustment should be used.

Rules for application of coarse phase adjust include the following:

- Coarse phase adjust lengthens or shortens the high and/or low pulses of the output clock in units of T_FOD.
- The coarse phase adjust will not shorten the output clock period to anything less than 2 × T_FOD high + 2 × T_FOD low.
  - This means coarse adjust cannot be used if the integer divider ratio is 1, 2, 3, or 4.
- Coarse phase adjust can lengthen or shorten (subject to the above rule) the output clock period by up to 2^{32} × T_FOD high + 2^{32} × T_FOD low.
  - Such a large change in a single clock period may have serious effects on devices receiving the output clock, so the user is cautioned to consider that before applying a large adjust at one time. Multiple smaller adjustments can be performed by the user over a period of time to avoid this.
• Logic within the 8A34044 will take the positive (lengthen the period) or negative (shorten the period) adjustment value provided by the user and apply it in a single clock period to the limits listed in the preceding rules.
• For clock signals that are using 50% / 50% duty cycle, adjustments will be applied approximately equally to the high and low portions of the clock.
• For clock signals using other duty cycle selections, adjustments will only be applied to the low portion of the clock.
• The user can apply as many of these updates as desired, so the range of adjustment is unlimited.

**Output Buffer**

The output buffer structure will generate either one differential or two single-ended output signals as programmed by the user. A single output stage will have one output buffer structure and a dual stage one will have two output buffers. Each output buffer has a separate V<sub>DDO_Qx</sub> pin that will affect its output voltage swing as indicated below and in Table 32.

**Output Buffer in Differential Mode**

When used as a differential output buffer, the user can control the output voltage swing (V<sub>OVS</sub>) and common mode voltage (V<sub>CMR</sub>) of the buffer. Which V<sub>OVS</sub> and V<sub>SWING</sub> settings may be used with a particular V<sub>DDO_Qx</sub> voltage are described in Table 17. Note that V<sub>DDO_Qx</sub> options of 1.5V or 1.2V cannot be used in differential mode. The nominal voltage swing options are 410mV, 600mV, 750mV, and 900mV. The nominal voltage crossing points options are 0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, and 2.3V. For actual values under different conditions, see Table 32.

**Table 17. Configurable Output Mode Options**

<table>
<thead>
<tr>
<th>V&lt;sub&gt;DDO_Qx&lt;/sub&gt;</th>
<th>SWING Setting</th>
<th>V&lt;sub&gt;OVS&lt;/sub&gt; Options Supported&lt;sup&gt;[a]&lt;/sup&gt;</th>
<th>V&lt;sub&gt;CMR&lt;/sub&gt; Options Supported</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>00</td>
<td>410mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>600mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>750mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>900mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V, 1.7V</td>
</tr>
<tr>
<td>2.5V</td>
<td>00</td>
<td>410mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V, 1.7V</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>600mV</td>
<td>0.9V, 1.1V, 1.3V, 1.5V</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>750mV</td>
<td>0.9V, 1.1V, 1.3V</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>900mV</td>
<td>0.9V</td>
</tr>
<tr>
<td>1.8V</td>
<td>00</td>
<td>410mV</td>
<td>0.9V, 1.1V, 1.3V</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>600mV</td>
<td>0.9V</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>750mV</td>
<td>0.9V</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>900mV</td>
<td>0.9V</td>
</tr>
</tbody>
</table>

<sup>[a]</sup> Voltage swing values are approximate values. For actual swing values, see Table 32, Table 33, and Table 34.

The user can use this programmability to drive LVDS, 2.5V LVPECL, and 3.3V LVPECL receivers without AC-coupling. Most other desired receivers can be addressed with this programmable output, but many will require AC-coupling or additional terminations. For termination recommendations for some common receiver types, see the appropriate section of the Applications Information or contact IDT using the contact information on the last page of this document.
Output Buffer in Single-Ended Mode

When used as a single-ended output buffer, two copies of the same output clock are created with LVCMOS output levels. Each clock will have the same frequency, phase, voltage, and current characteristics. The only exception to this is that the user can program the clock from the nQx output pad to be inverted in phase relative to the one coming from the Qx output pin. The non-inverted setting may result in greater noise on these outputs and increased coupling to other output clocks in the device, so it should be used with caution.

In this mode of operation, the output buffer supports 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V $V_{DDO_{Qx}}$ voltages. For each output voltage, there are four impedance options that can be selected from. For actual voltage and impedance values under different conditions, see Table 35.

General Purpose Input/Outputs (GPIOs)

The GPIO signals are intended to provide a user with a flexible method to manage the control and status of the part via pins without providing dedicated pins for each possible function that may be wasted in a lot of applications. The GPIOs are fully configurable so that any GPIO can perform any function on any target logic block.

GPIO Modes

Each GPIO pin can be individually configured to operate in one of the following modes. Note that these modes are effective only once the 8A34044 has completed its reset sequence. During the reset sequence one or more of these pins can have different functions as outlined in Use of GPIO Pins at Reset:

- General Purpose Input – In this mode of operation, the GPIO pin will act as an input whose logic level will be monitored and reflected in an internal register that may be read over the serial port. This is the default mode if no other option is programmed in OTP or EEPROM.
- General Purpose Output – In this mode of operation, the GPIO pin will act as an output that is driven to the logic level specified in an internal register. That register can be written over the serial port.
- Alarm output – In this mode of operation, the GPIO pin will act as a single-purpose alarm or Alert (aggregated alarm) output. For information on when an alarm output will be asserted or released and alarm sources, see Alarm Output Operation. Note that each GPIO can be independently configured. If multiple GPIOs are configured the same way, they will all have the same output values.
  - Loss-of-Signal status – In this mode of operation, the GPIO pin will act as an active-high Loss-of-Signal output. There is an option to invert this output polarity via register programming. When the GPIO output is asserted, that indicates the selected input reference monitor is indicating an alarm condition. The related reference monitor and the associated GPIO pin are configured via registers. Configuration of the reference monitor will determine what constitutes an alarm. For more information on reference monitor configuration, see Reference Monitoring. Note that the GPIO output reflects the actual state of the alarm signal from the selected reference monitor. This is not a latched or “sticky” signal. This is different than the other alarm sources below.
  - Loss-of-Lock status – In this mode of operation, the GPIO pin will act as a Loss-of-Lock output. The related PLL channel and associated GPIO pin are configured via registers. For more information on alarm conditions, see Digital Phase Locked Loop (DPLL) and System Analog PLL (APLL). The GPIO can be programmed to show the active Loss-of-Lock status, in which case a high state on the pin will indicate that the associated DPLL or APLL is not currently locked. Alternatively, the GPIO can be programmed to flag any changes in the lock status in a “sticky” bit mode. In this mode of operation, a high state will indicate that the lock status of the associated DPLL or APLL has changed. Either the PLL has entered or left the locked state. The GPIO can be programmed to invert this polarity so that a low state indicates a status change. In either case, since this is a “sticky” status, it must be cleared by register access to the “stick” clear register to remove the alarm signal.
  - Holdover status – In this mode of operation, the GPIO pin will act as a Holdover status. The related PLL channel and associated GPIO pin are configured via registers. For more information on alarm conditions, see Digital Phase Locked Loop (DPLL). The GPIO can be programmed to show the active Holdover status, in which case a high state on the pin will indicate that the associated DPLL is currently in holdover state. Alternatively, the GPIO can be programmed to flag any changes in the holdover status in a “sticky” bit mode. In this mode of operation, a high state will indicate that the holdover status of the associated DPLL has changed. Either the PLL has entered or left the holdover state. The GPIO can be programmed to invert this polarity so that a low state indicates a status change. In either case, since this is a “sticky” status, it must be cleared by register access to the “stick” clear register to remove the alarm signal.
• Alert (aggregated alarm) status – In this mode of operation, the GPIO will act as the logical OR of all alarm indicators that are enabled to drive this output. Only “sticky” bits are available to drive the GPIO in this mode. This output will be asserted if any of the “sticky” bits are asserted and enabled to cause the Alert (aggregated alarm). To clear this output, all contributing “sticky” bits must be individually cleared. This output will be active-high to indicate one or more alarms are asserted. There is an option to invert this output polarity via register programming.

• Output Disable control – In this mode of operation, the GPIO pin will act as a control input. When the GPIO input is high, the selected output clock(s) will be disabled, then placed in high-impedance state. When the GPIO pin is low, the selected output clock(s) will be enabled and drive their outputs as configured. For information on output frequency and output levels, see System Analog PLL (APLL) and FOD Multiplexing and Output Stages. Selection of which output(s) are controlled by which GPIO(s) is configured via registers over the serial port or by OTP or EEPROM at reset. Each GPIO can be configured to control any or all outputs (or none). So all combinations can be set up from a single GPIO controlling all outputs, to all outputs responding to individual GPIO signals and any grouping in between.

• Single-ended Input Clock – In this mode of operation a single-ended input clock can be applied to certain GPIOs that map to specific input stages (see Input Stage for details, including which GPIOs map to which input references). This can be used if extra single-ended inputs are needed due to all input reference clock pins being taken-up by differential input references. This mode cannot be used if an input stage already has two single-ended input references from the CLKx/nCLKx input pins.

• Manual Clock Selection control – In this mode of operation, the GPIO pin acts as an input that will manually select between one of two inputs for a specific DPLL channel. The specific input references and the PLL channel must be preconfigured via registers. Assertion of the GPIO will select the higher priority input and de-assertion will select the lower priority input. For information on how to configure the input references for a PLL channel, see DPLL Input Clock Qualification and Selection.

• DCO Increment – In this mode of operation, the GPIO pin will act as an increment command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause an increment function on the indicated DCO. The amount of the increment and the related DCO to increment must be previously configured via registers. For more information, see Increment / Decrement Registers and Pins.

• DCO Decrement – In this mode of operation, the GPIO pin will act as a decrement command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause a decrement function on the indicated DCO. The amount of the decrement and the related DCO to decrement must be previously configured via registers. For more information, see Increment / Decrement Registers and Pins.

• Clock Disqualification Input – In this mode of operation, the GPIO pin will act as an active-high disqualification input for a preconfigured input and DPLL. This is intended to be connected to the LOS output of a PHY or other device. For more information, see DPLL Input Clock Qualification and Selection.

### GPIO Pin Configuration

The GPIO pins are all powered off a single voltage supply that only supports 1.8V operation. An internal register must be set to indicate 1.8V. This setting is a global one for all GPIOs.

In addition, each GPIO can be enabled or disabled under register control. If enabled and configured in an operating mode that makes it an output, the user can choose if the GPIO output will function as an open-drain output or a CMOS output. The open-drain output drives low but is pulled high by a pull-up resistor. There is a very weak pull-up internal to the 8A34044, but an external pull-up is strongly recommended. In CMOS mode, the output voltage will be driven actively both high and low as needed. Register control can also enable a pull-up (default) or pull-down.

### Alarm Output Operation

There are many internal status and alarm conditions within the 8A34044 that can be monitored over the serial port by polling registers. Several of these can be directed to GPIO pins as indicated in General Purpose Input/Outputs (GPIOs). In addition, one of the GPIOs can be designated as an Alert (aggregated alarm) output signal called an Alert output.
The 8A34044 provides both a “live” and a “sticky” status for each potential alarm condition. A “live” bit shows the status of that alarm signal at the moment it is read over the serial port. A “sticky” bit will assert when an alarm condition changes state and will remain asserted until the user clears it by writing to the appropriate clear bit over the serial port. When a GPIO is configured to show the status of a specific alarm, it will show the “live” or sticky status of that alarm, depending on the specific alarm, where a high output on the GPIO indicates the alarm is present. For more information, see GPIO Modes. The GPIO can be programmed to invert the alarm if desired.

The Alert (aggregated alarm) output logic only uses the “sticky” status bit for alarms. This ensures when a software routine reads the 8A34044 there will be an indication of what caused the alarm in the first place. Note that there can be multiple sticky bits asserted. Table 18 shows the alarm conditions possible within the 8A34044. Note that the reference monitor, the DPLL, and the System DPLL blocks can generate the indicated alarms.

Table 18. Alarm Indications

<table>
<thead>
<tr>
<th>Logic Block</th>
<th>Specific Alarm</th>
<th>Conditions for Live Alarm[a] to Assert</th>
<th>Conditions for Live Alarm[a] to Negate[b]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Monitoring</td>
<td>Frequency Offset Limit Exceeded</td>
<td>See Frequency Offset Monitoring</td>
<td>See Frequency Offset Monitoring</td>
</tr>
<tr>
<td></td>
<td>Loss-of-Signal</td>
<td>See Loss of Signal (LOS) Monitoring</td>
<td>See Loss of Signal (LOS) Monitoring</td>
</tr>
<tr>
<td></td>
<td>Activity Alarm</td>
<td>See Activity Monitor</td>
<td>See Activity Monitor</td>
</tr>
<tr>
<td>Digital Phase Locked Loop (DPLL)</td>
<td>Holdover</td>
<td>DPLL has entered / is in the Holdover state</td>
<td>DPLL no longer in Holdover state</td>
</tr>
<tr>
<td></td>
<td>Locked</td>
<td>DPLL has entered / is in the Locked state and System APLL is in the Locked state</td>
<td>DPLL and/or System APLL no longer in the Locked state</td>
</tr>
</tbody>
</table>

[a] “Sticky” alarm bits are set whenever the associated live alarm changes state. So there will be a new “sticky” alarm on both assertion and negation of the appropriate live alarm indication.

[b] Only the “live” status will negate by itself. The “sticky” needs to be explicitly cleared by the user.

[c] For the Digital PLL, “sticky” alarms are raised when the state machine transitions into specific states and “live” status indicates that the Digital PLL is currently in a specific state. The user can read the current state of the Digital PLL state machine from status registers over the serial port.

[d] This includes the System DPLL, as well as all Digital PLLs.

For each alarm type in each logic block that can generate them, there is a “live” status, a “sticky” status, a “sticky” clear control and a series of control bits that indicate what effects the alarm will have. When the “live” status changes state, the “sticky” status will assert. If so configured via registers, that alarm may generate an external signal via GPIO. That signal may be an individual alarm output or an Alert (aggregated alarm). Once external software responds, it is expected to read the sticky status bits to determine the source(s) of the alarm and any other status information it may need to take appropriate action. The “sticky” clear control can be used to clear any or all of the bits that contributed to the alarm output being asserted.

In addition to the above controls and status, each potential alarming logic block has its own controls and status. Each of the reference monitors has a “sticky” status bit, a “sticky” clear bit and various control bits. Each of the DPLLS and the SysDPLL have a “sticky” status bit, a “sticky” clear bit, control bits and a PLL state status field. These functions behave as described in the previous paragraph. Note that both the individual alarm “sticky” status and the logic block “sticky” status must be cleared to fully remove the source of the alarm output. Individual “sticky” alarms should be cleared first so that all individual alarms associated with a logic block won’t cause a re-assertion of the block “sticky” alarm.

Note: Clearing of all sticky bits via the registers may not result in the Alarm output pin negating for up to 200µsec and so that GPIO should not be used as a direct input to a CPU’s interrupt input or multiple interrupts may be generated within that CPU for a single alarm event.

There are also several configuration bits that act on the alarm output logic as a whole. There is a global alarm enable control that will enable or disable all alarm sources. This can be used during alarm service routines to prevent new alarms while that handler is executing in external software. The user can also designate a GPIO as an Alert (aggregated alarm) output and determine which individual alarms will be able to drive it. The GPIO can be programmed to invert the Alert (aggregated alarm) if desired.
Device Initial Configuration

During its reset sequence, the 8A34044 will load its initial configuration, enable internal regulators, establish and enable internal clocks, perform initial calibration of the Analog PLL, and lock it to the reference on the OSCI/OSCO pins. Depending on the initial configuration, it may also bring up Digital PLLs, lock to input references including any OCXO/TCXOs, and generate output clocks.

The following four mechanisms can be used to establish the initial configuration during the reset sequence:

- State of certain GPIO pins (see Table 19) at the rising edge of the nMR signal
- Configuration previously stored in One-Time Programmable memory
- Configuration stored in an external I2C EEPROM
- Default values for internal registers

Each of these is discussed individually in the following sections and then integrated into the reset sequence.

Use of GPIO Pins at Reset

All of the device GPIO pins are sampled at the rising edge of the nMR (master reset) signal and some of them may be used in setting the initial configuration. Table 19 shows which pins are used to control what aspects of the initial configuration. All of these register settings can be overwritten later via serial port accesses. Note also that several GPIOs can be used as a JTAG port when in Test mode. For information, see JTAG Interface. If these GPIOs are being used as a JTAG interface, it is recommended that they not be used for any of the reset functions outlined below.

Table 19. GPIO Pin Usage at Start-Up

<table>
<thead>
<tr>
<th>GPIO Number</th>
<th>Function</th>
<th>Internal Pull-up or Pull-down</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>0 = Main serial port uses SPI protocol</td>
<td>Pull-up</td>
</tr>
<tr>
<td></td>
<td>1 = Main serial port uses I2C protocol</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Must be high during reset active period</td>
<td>Pull-up</td>
</tr>
</tbody>
</table>
| 4 pins      | Identifies which stored configuration in OTP to use for initial configuration (has no effect with “-000” unprogrammed devices).
| user selectable[a] | See details just below this table.                                      |                              |
| 1 pin user selectable[a] | Disables EEPROM accesses during start-up sequence.
|             | By default, no GPIO is used for this purpose, so the device will attempt to find an external EEPROM to check for additional start-up information by default.
|             | See details just below this table.                                       | Pull-up                       |
| 1 pin user selectable[a] | Provides pin control for I2C slave serial port (for serial port selected by GPIO[9] as I2C) default base address bit A2. Has no effect on serial port selected as SPI.
|             | By default no GPIO is used for this purpose, so the default I2C slave port base address will have a 0 for bit A2.
|             | See details just below this table.                                       | Pull-up                       |

[a] Selection of this mode for a GPIO is performed using the Device Information block in the OTP memory, which is programmed by IDT at the factory for dash codes that are non-zero. “-000” dash code devices are considered unprogrammed and so will have the default behavior indicated above.
Any of the available GPIOs can be used as the following:

- **I2C base address bit A2** – This is for the serial port when selected as I2C during the start-up sequence using GPIO[9]. If no GPIOs are configured in this mode, bit A2 of the slave serial port base address will be zero. The value of the I2C base address and the serial port configuration can be overwritten by SCSR configuration data or serial port accesses later in the start-up sequence. If more than one GPIO is programmed with this functionality, only the one with the highest index will be used (e.g., if both GPIO[5] and GPIO[7] are programmed to do this, only GPIO[7] would be used).

- **EEPROM Access Disable control** – A high input value on a GPIO programmed with this function prevents a device from attempting to read device update information or SCSR configuration data from an external I2C EEPROM. This will speed up device reset time but prevent access to updated information that may be stored in EEPROM. If no GPIOs are configured in this mode then the device will attempt to locate an external EEPROM at the appropriate point in the start-up sequence. If multiple GPIOs are configured to perform this function then any one of them being active will disable EEPROM accesses, so it is recommended that no more than one GPIO be programmed for this function.

- **Default Configuration Select control** – If no GPIOs are selected then GPIO[3:0] will be assumed and the value on those pins at the rising edge of the nMR signal will be used to select which of the SCSR configurations in OTP memory is to be used. Note that since a GPIO is pulled-up by default, unless these pins are pulled or driven low during the reset period, this will select SCSR Configuration 15. If one or more GPIOs are selected for this function, then the value on those pins at the rising edge of nMR will be used to select the SCSR configuration to be loaded. The Device Information block of the OTP can be configured to select any of up to four GPIO pins to be used for this purpose if the default GPIOs are not convenient. The GPIOs chosen do not have to be sequential, but whichever ones are chosen, the one with the lowest index number will be the LSB and so on in order of the index until the GPIO with the highest index is the MSB. No GPIO that appears elsewhere in this table should be used for this purpose.

For example, if GPIO[8], GPIO[6], GPIO[5] and GPIO[2] are used, GPIO[8] is the MSB, GPIO[6] is next most significant, GPIO[5] is next and GPIO[2] is the LSB.

If less than four GPIO pins are selected, then the selected GPIOs will be used as the least-significant bits of a 4-bit selection value, with the upper bits set to zero. If more than four GPIOs are programmed for this function, then the GPIOs will form a larger bit-length word for selection of internal configuration.

**Default Values for Registers**

All registers are defined so that the default state (without any configuration data from OTP or EEPROM being loaded) will cause the device to power-up with none of the outputs enabled and all GPIO signals in General-Purpose Input mode. Users can then program any desired configuration data over the serial port once the reset sequence has completed.

**One-Time Programmable (OTP) Memory**

The 8A34044 contains a 32kbytes One-Time Programmable (OTP) memory block that is customer programmable. The term “one-time programmable” refers to individual blocks within the memory structure. Different blocks can be programmed at different times, but each block can only be programmed once. The data structure within the OTP is designed to facilitate multiple updates and multiple configurations being stored, up to the limit of the physical memory space.

Access to OTP memory is via serial port through registers that communicate with an internal OTP controller state machine. The state machine protocol is handled via IDT’s Timing Commander GUI software, which is the recommended access mechanism. For customers that wish to program OTP via another method, such as in their own production processes, should contact IDT for details on this state machine interface. Note that OTP programming is considered an “offline” function and should not be performed while the device is in an operational system.

After reset of the 8A34044, all internal registers are reset to their default values, then OTP contents are loaded into the device’s internal registers. A Device Information block programmed by IDT at Final Test will always be loaded. This provides information that is specific to the device, including product ID codes and revision information. In addition there are zero or more device configurations stored in the OTP by customer programming or by IDT at the factory if a special dash-code part number is requested. Certain GPIO pins are sampled at the rising edge of the external nMR input signal. The state of those pins at that time will be used by the 8A34044 to determine which of up to 16 configurations stored in the OTP to load into the device registers. For information on how to select a configuration, see Use of GPIO Pins at Reset.
Storage of configuration data in OTP does not require having a value stored for every register in the device. Register default values are defined to ensure that most functions will be disabled or otherwise made as neutral as possible. This allows only features that are being used in any particular configuration (and their associated trigger registers as defined in the 8A3xxx Family Programming Guide) to need to be stored in OTP for that configuration. The intent of this is to minimize the size a configuration takes in OTP to allow more configurations to be stored there. For this reason, the exact number of configurations storable in OTP cannot be predetermined. There will be a minimum of two configurations and a maximum of 16 configuration capacity in the OTP.

Part numbers with -000 as the dash code number are considered “unprogrammed” parts, but will come with at least a Device Information block pre-programmed with IDT-proprietary information, including parameters needed to successfully boot the device to the point where it can read its configuration data. One Device Update block may also be programmed if determined to be appropriate by IDT.

Custom user configurations indicated with non-zero dash code part numbers will in addition have one or more SCSR Configuration sections pre-programmed as indicated in the datasheet addendum for that particular dash code part number.

Note that a programmed configuration, Device Information block, or Device Update block may be invalidated via the OTP programming interface, and if sufficient OTP space remains, a new one added to replace it. Note that this does not erase or remove the original data and the space it consumes. It just marks it to be ignored by the device. This allows for a limited ability to update a device in the field either from a device functional update or configuration data perspective. This is a purely software-driven process handled over the serial port. Please contact IDT for support if this type of in-field upgrade / change is desired. Note that the ability to perform this type of in-field update is highly dependent on the size of the change versus the remaining space in OTP, so it will not be possible in all cases.

**Configuration Data in OTP**

Users can program multiple configurations into the internal One-Time Programmable memory. IDT’s Timing Commander GUI Software can perform this function. Please contact IDT for sample code if this needs to be performed in another way by the end user. By using the GPIO pins at start-up as outlined in Use of GPIO Pins at Reset, one of those configurations can be chosen for use as the initial values in the device registers after reset. Register values can be changed at any time over the serial port, but any such changes are not stored in OTP and will be lost on reset or power-down.

The OTP is organized so that only configuration data that changes from the register default values needs to be stored. This saves OTP space and allows the potential for more configurations to be stored in the OTP.

If the indicated configuration in OTP has a checksum error, it will not be loaded and registers will be left at their default values.

**Use of External I²C EEPROM**

The 8A34044 can search for additional configuration or device updates in an external I²C EEPROM. As described in the Use of GPIO Pins at Reset, a GPIO can be configured to select whether or not this search will be performed during the reset sequence. The EEPROM search will not be performed if the serial port is set to SPI mode since the necessary I²C Master signals are not available in that mode. The remainder of this description assumes the EEPROM search is enabled.

The 8A34044 will use its I²C Master Port to attempt to access an external I²C EEPROM at base address 1010000 (binary) at an I²C frequency of 1MHz. If there is no response, this will be repeated at base address 1010001 (binary) at 1MHz. This will repeat up to address 1010111 (binary) at 1MHz. If there still are no responses, the search will be repeated at 400kHz and then again at 100kHz. If no response is received after this entire sequence, the device will assume there is no EEPROM available. Any errors in the process will be reported in status registers.

**Device Updates in External I²C EEPROM**

As indicated in Reset Sequence, if enabled, the 8A34044 will search for Device Update information in an external I²C EEPROM. It will first identify all valid EEPROMs attached to the I²C master port as described above. Each valid EEPROM will be checked for a valid Device Update Block header with valid checksum at address offset 0x0000 within the EEPROM. The first such valid block will be used as described in Reset Sequence.
**Configuration Data in External I²C EEPROM**

As a final option for device configuration, the initial configuration can be read from an external I²C EEPROM. IDT’s Timing Commander GUI Software can generate the necessary EEPROM load information as an Intel HEX file for this purpose. The 8A34044 will search each EEPROM identified during the above search sequence for a valid configuration data block (valid header and checksum). The first valid block found will be loaded into internal registers after checksum validation. The search will terminate after the first valid block is found and loaded. This means that only a single valid configuration block can be stored via the EEPROM method.

When the device searches for an EEPROM configuration, it will check for a valid block at address offsets 0x0000 and 0xF000 within an EEPROM. If using this configuration method, see the warning in Step 5 – Search for Configuration in External EEPROM.

**Reset Sequence**

Figure 17 shows the relationship between the master reset signal (nMR) and the supply voltages for the 8A34044. There are no power sequencing requirements between the power rails, so V_DD in the diagram represents any of the supply voltages. To ensure there is no anomalous behavior from the device as it powers up, it is recommended that the nMR signal be asserted (low) before any voltage supply reaches the minimum voltage shown in the figure. nMR should remain asserted until a short hold time (t_HOLD ~10nsec) after all supply voltages reach the operating window of 95% of nominal voltage. nMR must be asserted or the device will not function correctly after power-up.

One additional consideration is that once minimum voltage is reached on all voltage supplies, internal regulators and voltage references will need the amount of start-up time specified in Table 38, “Regulators Ready.” If the time t_RAMP shown in Figure 17 is less than the voltage regulators’ start-up time indicated in Table 38, then release of nMR should be delayed.

**Figure 17. Power-Up Reset Sequencing**

In cases where the device is not powering up and just being reset, a low pulse on nMR of 20ns will be sufficient to reset the device.

The following reset sequence will start from the rising (negating) edge of the nMR (master reset) signal when nTEST is de-asserted (high).

**Step 0 – Reset Sequence Starting Condition**

Once power rails reach nominal values and the nMR signal has been asserted, the 8A34044 will be in the following state:
- All Qx / nQx outputs will be in a high-impedance state.
- All GPIO pins will be set to General-Purpose Inputs, so none will be driving the output.
- The serial port protocols are not set at this point in the reset sequence, so the ports will not respond.
- Device Information block loaded from internal OTP to configure what GPIOs will be used for what start-up functions in Step 1.
- The System APLL will be configured and calibrated based on frequency information in the Device Information block then locked to the reference clock on the OSCI input.
Step 1 – Negation of nMR (Rising Edge)
At the rising edge of the nMR signal, the state on the GPIO pins at that time is latched. After a short hold time, the GPIOs can release their reset levels and assume their normal operation modes. The latched values will be used in later stages of the reset sequence.

Step 2 – Internally Set Default Conditions
An internal image of the device registers will be created in internal RAM with all registers set to their default values. This will not result in any changes to the GPIO or output clock signals from their Step 0 condition.

Based on the serial port protocol selection made via the GPIO pin in Step 1, serial port configuration will be completed as indicated by the GPIO input pin. If SPI mode is selected by the GPIO, the register default values will configure it to use 4-wire SPI mode.

Step 3 – Scan for Device Updates in EEPROM
If enabled to do so, the 8A34044 will check for device functional update information in any available EEPROMs (for information on how EEPROMs are searched for, see Use of External I\(^2\)C EEPROM). If such information is found, it will be loaded, the device functionality updated, and then the part will reinitialize to Step 0.

Step 4 – Read Configuration from OTP
Using the GPIO values latched in Step 1, the device will search the internal OTP memory for the indicated configuration number. If no such configuration is found or the configuration has an invalid checksum, the device will skip to Step 5. Any errors in this process will be reported. If loading from OTP was successful, which configuration number was loaded will be reported.

If the requested configuration is found and is valid, the device will load the registers indicated in the configuration data with the stored data values in the internal register image. Any register not included in the configuration data set will remain at its default value in the register image.

Note: Many register modules have explicitly defined trigger registers that when written will cause the other register settings in that module to take effect. Users must ensure that the configuration in OTP will cause a write to all applicable trigger registers, even if that register’s contents would be all zero. Multi-byte register fields also require all bytes of the field to be written to ensuring triggering. For indications of which trigger registers are associated with which other registers, see the 8A3xxxx Family Programming Guide.

The contents of several of the registers will be used to guide the remainder of the reset sequence:
- If the APLL feedback divider value was programmed in this step, perform APLL calibration in parallel with remaining reset activities.
- Re-configure the serial ports to use I\(^2\)C or SPI protocols as indicated. For information, see I2C Slave Operation or SPI Operation.

Step 5 – Search for Configuration in External EEPROM
The 8A34044 will check for configuration information in any available EEPROM (for information on how EEPROMs are searched for, see Use of External I\(^2\)C EEPROM).

If a valid configuration data block is found, it will be read, its checksum validated and if that passes, loaded into the internal register image similarly to OTP configuration data described in Step 4. If the data found is not of the correct format or the data block fails a checksum comparison, it will be ignored. The search will continue through the EEPROM and on to the next EEPROM address until the complete range has been searched or a valid configuration block has been found and applied to the internal register image. Then the sequence will proceed to Step 6.

Note: Since OTP and EEPROM configuration data rarely consists of a full register image, reading of configuration data from OTP and then from a configuration block stored in EEPROM may result in internal registers being loaded with conflicting settings drawn partially from each of the configuration data sets being loaded. It is strongly recommended that a configuration block placed in EEPROM only be used when no valid configuration is being pointed to in OTP by GPIO signals (or there is no valid configuration in OTP at all). If multiple configurations are to be used then the user must ensure all registers are set to the desired values by the final configuration block to be loaded.

Step 6 - Load OTP Hotfix and Execute
If the 8A34044 OTP memory contains a hotfix, that information will be loaded into RAM and executed at this point.
Step 7 – Complete Configuration

The 8A34044 will complete the reset and initial configuration process at this point and begin normal operations. Completion steps include the following:

1. If configuration information was loaded in Step 4 or Step 5, recalibrate the System APLL and lock it to the reference clock on the OSC input.
2. Enable serial port operation as configured.
3. Apply configuration settings from the internal register image to the actual registers and enable output clocks and GPIOs as configured.
5. Enable alarm operation as configured.

Note that there are several scenarios in which the reset sequence will reach this point without retrieving any configuration data and with all registers in the default state. This may be intentional for users who wish to configure only via the serial port or the result of a problem in the loading of a configuration. Users can read appropriate status bits to determine what failures, if any, occurred during the reset sequence.

Clock Gating and Logic Power-Down Control

The 8A34044 can disable the clocks to many logic blocks inside the device. It also can turn off internal power regulators, disabling individual power domains within the part. Because of the potentially complex interactions of the logic blocks within the device, logic within the part will handle the decision-making of what will be powered-off, versus clock-gated, versus fully operational at any time. By default, the device will configure itself with functions in the lowest power-consuming state consistent with powering up the part and reading a user configuration. User configurations, whether stored in internal OTP, external EEPROM, or manually adjusted over the serial port, should make use of register bits to only turn on functions that are needed. Also if a function is no longer needed, register bits should be used to indicate it is no longer required. Internal logic will reduce its power-consumption state in reaction to these indicators to the greatest extent possible.

For more information on how to calculate power consumption for a particular configuration, consult IDT’s Timing Commander software for more precise results for a particular configuration.

Serial Port Functions

The 8A34044 supports one serial port. The signals on the port share the functions of an I²C Master port used for loading configuration data at reset and a configurable slave I²C or SPI port that can be used at any time after the reset sequence is complete to monitor and/or configure the device. Note that the I²C master port can only be used when the slave port is configured in I²C mode. Since I²C master operation only occurs immediately after reset, while configuration or other data is being loaded from an external I²C serial EEPROM, I²C mode for the serial port can be selected via GPIOs as indicated in Use of GPIO Pins at Reset.

The operation of the serial port when in I²C master operation (during self-configuration only) is described in I2C Master. The SCLK and SDIO pins are used for this purpose if the slave port is configured in I²C mode. If the slave port is configured as SPI then I²C master mode operation is not supported.

For information on the operation of the master I²C and slave I²C or SPI ports, see the appropriate section below.

A slave serial port can be reconfigured at any time by accessing the appropriate registers within a single burst write. This includes configuration options with each protocol or switching between protocols (I²C to SPI or vice versa). However, it is recommended that the full operating mode configuration, including page sizes for registers for a serial port be set in the initial configuration data read from OTP or external EEPROM (for information, see Device Initial Configuration).
**Note on Signal Naming in the Remainder of the Serial Port Sections**

The pin names indicated in the Pin Description table are meant to indicate the function of that signal when used in SPI mode and also the function when in I²C mode. In the remainder of the Serial Port Functions descriptions, the SPI descriptions will refer to the signals by their function in the selected mode, as shown in Table 20.

**Table 20. Serial Port Pin to Function Mapping**

<table>
<thead>
<tr>
<th>SPI Mode Signal Name</th>
<th>Function</th>
<th>I²C Mode Signal Name</th>
<th>Function</th>
<th>Package Pin Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>SPI Clock Input</td>
<td>SCLK</td>
<td>I²C Clock Input</td>
<td>SCLK</td>
</tr>
<tr>
<td>CS</td>
<td>SPI Chip Select (active low)</td>
<td>A0</td>
<td>I²C Slave Address Bit 0</td>
<td>CS_A0</td>
</tr>
<tr>
<td>SDI</td>
<td>SPI Data Input (unused in 3-wire mode)</td>
<td>A1</td>
<td>I²C Slave Address Bit 1</td>
<td>SDI_A1</td>
</tr>
<tr>
<td>SDIO</td>
<td>SPI Data Out (4-wire mode) SPI Data In/Out (3-wire mode)</td>
<td>SDA</td>
<td>I²C Data In/Out</td>
<td>SDIO</td>
</tr>
</tbody>
</table>

**Addressing Registers within the 8A34044**

The address space that is externally accessible within the 8A34044 is 64KB in size, and thus, needs 16 bits of address offset information to be provided during slave serial port accesses. Of that 64KB, only the upper 32KB contains user accessible registers.

The user may choose to operate the serial port providing the full offset address within each burst, or to operate in a paged mode where part of the address offset is provided in each transaction and another part comes from an internal page register in each serial port. Figure 18 shows how page register and offset bytes from each serial transaction interact to address a register within the 8A34044.

**Figure 18. Register Addressing Modes via Serial Port**
I²C Slave Operation

The I²C slave protocol of the 8A34044 complies with the I²C specification, version UM10204 Rev.6 – 4 April 2014. Figure 19 shows the sequence of states on the I²C SDA signal for the supported modes of operation.

Figure 19. I²C Slave Sequencing

Sequential 8-bit Read

<table>
<thead>
<tr>
<th>S</th>
<th>Dev Addr + W</th>
<th>A</th>
<th>Offset Addr X</th>
<th>A</th>
<th>Sr</th>
<th>Dev Addr + R</th>
<th>A</th>
<th>Data X</th>
<th>A</th>
<th>Data X+1</th>
<th>A</th>
<th>…</th>
<th>A</th>
<th>Data X+n</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
</table>

Sequential 8-bit Write

<table>
<thead>
<tr>
<th>S</th>
<th>Dev Addr + W</th>
<th>A</th>
<th>Offset Addr X</th>
<th>A</th>
<th>Data X</th>
<th>A</th>
<th>Data X+1</th>
<th>A</th>
<th>…</th>
<th>A</th>
<th>Data X+n</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
</table>

Sequential 16-bit Read

<table>
<thead>
<tr>
<th>S</th>
<th>Dev Addr + W</th>
<th>A</th>
<th>Offset Addr X MSB</th>
<th>A</th>
<th>Offset Addr X LSB</th>
<th>A</th>
<th>Sr</th>
<th>Dev Addr + R</th>
<th>A</th>
<th>Data X</th>
<th>A</th>
<th>Data X+1</th>
<th>A</th>
<th>…</th>
<th>A</th>
<th>Data X+n</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
</table>

Sequential 16-bit Write

<table>
<thead>
<tr>
<th>S</th>
<th>Dev Addr + W</th>
<th>A</th>
<th>Offset Addr X MSB</th>
<th>A</th>
<th>Offset Addr X LSB</th>
<th>A</th>
<th>Data X</th>
<th>A</th>
<th>Data X+1</th>
<th>A</th>
<th>…</th>
<th>A</th>
<th>Data X+n</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
</table>

The Dev Addr shown in the figure represents the base address of the 8A34044. This 7-bit value can be set in an internal register that can have a user-defined value loaded at reset from internal OTP memory or an external EEPROM. The default value if those methods are not used is 1011000b. Note that the levels on the A0 and A1 signals can be used to control Bit 0 and Bit 1, respectively, of this address. There is also an option to designate the reset state of a GPIO pin to set the default value of the A2 bit of the I²C slave port base address (for information, see Use of GPIO Pins at Reset). In I²C operation these inputs are expected to remain static. They have different functions when the part is in SPI mode. The resulting base address is the I²C bus address that this device will respond to.

When I²C operation is selected for a slave serial port, the selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be configured. These offsets are used in conjunction with the page register for each serial port to access registers internal to the device. Because the I²C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8 bits of the register offset address come from the Offset Addr byte and the upper 8 bits come from the page register. The page register can be accessed at any time using an offset byte value of 0xFC. This 4-byte register must be written in a single-burst write transaction.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes, so the page register only needs to be set up once after reset via a 4-byte burst access at offset 0xFFFC.

Note: I²C burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I²C burst access. Bursts can be of greater length if desired, but must not extend beyond the end of the register page (Offset Addr 0xFF in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

Figure 20 and Table 21 show the detailed timing on the interface. 100kHz, 400kHz, and 1MHz operation are supported.
I²C 1-byte (1B) Addressing Examples
8A34044 I²C 7-bit I²C address is 0x5B with LSB = R/W

Example write “0x50” to register 0xCBE4:

B6* FC 00 CB 10 20  #Set Page Register, *I²C Address is left-shifted one bit.
B6 E4 50  #Write data 50 to CB E4

Example read from register 0xC024:

B6* FC 00 C0 10 20  #Set Page Register, *I²C Address is left-shifted one bit.
B6 24*  #Set I²C pointer to 0xC024, *I²C instruction should use “No Stop”
B7 <read back data>  #Send address with Read bit set.

I²C 2-byte (2B) Addressing
8A34044 I²C 7-bit I²C address is 0x5B with LSB = R/W

Example write “50” to register 0xCBE4:

B6* FF FD 00 10 20  #Set Page Register, *I²C Address is left-shifted one bit.
B6 CB E4 50  #Write data to CB E4

Example read from register 0xC024:

B6* FF FD 00 10 20  #Set Page Register (*I²C Address is left-shifted one bit.)
B6 C0 24*  #Set I²C pointer to 0xC024, *I²C instruction should use “No Stop”
B7 <read back data>  #Send address with Read bit set.

Figure 20. I²C Slave Timing Diagram

![I²C Slave Timing Diagram](image)

Table 21. I²C Slave Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCLK</td>
<td>SCLK Operating Frequency</td>
<td></td>
<td>1</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>tLOW</td>
<td>SCLK Pulse Width Low</td>
<td></td>
<td>130</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tHIGH</td>
<td>SCLK Pulse Width High</td>
<td></td>
<td>9</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSU:STA</td>
<td>Start or Repeat Start Setup Time to SCLK</td>
<td></td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tHD:STA</td>
<td>Start or Repeat Start Hold Time from SCLK</td>
<td></td>
<td>18</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSU:DAT</td>
<td>Data Setup Time to SCLK rising edge</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tHD:DAT</td>
<td>Data Hold Time from SCLK rising edge</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSU:STO</td>
<td>Stop Setup Time to SCLK</td>
<td></td>
<td>12</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tBUF</td>
<td>Minimum Time from Stop to Next Start</td>
<td></td>
<td>0.5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
**I²C Master**

The 8A34044 can load its register configuration from an external I²C EEPROM during its reset sequence, but only if the serial port is configured in I²C mode. For information on what accesses occur under what conditions, see **Reset Sequence**.

As needed during the reset sequence, the 8A34044 will arbitrate for the I²C bus and attempt to access an external I²C EEPROM using the access sequence shown in **Figure 21**. The I²C master protocol of the 8A34044 complies with the I²C specification, version UM10204 Rev.6 – 4 April 2014. As displayed in the figure, the I²C master port can be configured to support I²C EEPROMs with either 1-byte or 2-byte offset addressing. The I²C master logic will negotiate with any EEPROMs found to use the highest speed of 1MHz, 400kHz, or 100kHz.

**Figure 21. I²C Master Sequencing**

Sequential Read (1-byte Offset Address)

<table>
<thead>
<tr>
<th></th>
<th>S</th>
<th>Dev Addr + W</th>
<th>A</th>
<th>Offset Addr X</th>
<th>A</th>
<th>Sr</th>
<th>Dev Addr + R</th>
<th>A</th>
<th>Data X</th>
<th>A</th>
<th>Data X+1</th>
<th>A</th>
<th>...</th>
<th>A</th>
<th>Data X+n</th>
<th>A</th>
<th>P</th>
</tr>
</thead>
</table>

Sequential Read (2-byte Offset Address)

|   | S | Dev Addr + W | A | Offset Addr X | A | Offset Addr X | A | Sr | Dev Addr + R | A | Data X | A | Data X+1 | A | ... | A | Data X+n | A | P |

- **S** = Start
- **Sr** = Repeated start
- **A** = Acknowledge
- **A** = Non-acknowledge
- **P** = Stop

From master to slave

From slave to master
SPI Operation

The 8A34044 supports SPI operation as a selectable protocol on the serial port. The port can be configured for either 3-wire or 4-wire operation. In 4-wire mode, there are separate data in (to the 8A34044) and data out signals (SDI and SDIO respectively). In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal. Figure 22 shows the sequencing of address and data on the serial port in both 3-wire and 4-wire SPI mode. 4-wire SPI mode is the default. The R/W bit is high for Read Cycles and low for Write Cycles.

Figure 22. SPI Sequencing

SPI Read Sequence*

SPI Write Sequence*

* See the timing diagrams for exact timing relationships.

A serial port can be configured for the following settings. These settings can come from register defaults, or from an internal OTP or external EEPROM configuration loaded at reset:

- 1-byte (1B) or 2-byte (2B) offset addressing (see Figure 18)
  - In 1B operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed using an Offset Address of 0x7C with a 4-byte burst access.
  - In 2B operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and taking the upper 1-bit from the page register. Note that this bit will always be 1 for register accesses, so the page register only needs to be set once in 2B operation. The page register can be accessed using a 3-byte burst access Offset Address of 0x7FFD. It should be accessed in a single burst write transaction to set it.

- Data sampling on falling or rising edge of SCLK
- Output (read) data positioning relative to active SCLK edge
- 4-wire (SCLK, CS, SDIO, SDI) or 3-wire (SCLK, CS, SDIO) operation
- In 3-wire mode, SDIO is a bi-directional data pin.
- Output signal protocol compatibility / drive strength and termination voltage
Note: SPI burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts can be of greater length if desired, but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

**SPI 1-byte (1B) Addressing Example**

Example write to “50” to register 0xCBE4

7C 80 CB 10 20 #Set Page register
64* 50 #*MSB is 0 for write transactions

Example read from 0xC024:

7C 00 C0 10 20 #Set Page register
A4* 00 #*MSB is set, so this is a read command

**SPI 2-byte (2B) Addressing Example**

Example write to “50” to register 0xCBE4

7F FD 80 10 20 #Set Page register
4B E4* 50 #*MSB is 0 for write transactions

Example read from 0xC024:

7F FD 80 10 20 #Set Page register
C0* 24 00 #*MSB is set, so this is a read command

SPI timing is shown in Figure 23 and Table 22.
**Figure 23. SPI Timing Diagram**

**SPI_CLOCK_SELECTION = 0**

![SPI Timing Diagram for SPI_CLOCK_SELECTION = 0](image)

**SPI_CLOCK_SELECTION = 1**

![SPI Timing Diagram for SPI_CLOCK_SELECTION = 1](image)

**Table 22. SPI Timing**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Maximum operating frequency for serial port</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PWH}$</td>
<td>SCLK Pulse Width High</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PWL}$</td>
<td>SCLK Pulse Width Low</td>
<td>6</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SU1}$</td>
<td>CS Setup Time to SCLK rising or falling edge</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HD1}$</td>
<td>CS Hold Time from SCLK rising or falling edge</td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SU2}$</td>
<td>SDIO Setup Time to SCLK rising or falling edge</td>
<td>4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HD2}$</td>
<td>SDIO Hold Time from SCLK rising or falling edge</td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{D1}[a]$</td>
<td>Read Data Valid Time from SCLK rising or falling edge with no data delay added</td>
<td>$V_{CCCS} = 3.3V$</td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
The 8A34044 provides a JTAG interface that can be used in non-operational situations with the device when nTEST control pin is held low. The JTAG interface is compliant with IEEE-1149.1 (2001) and supports the IDCODE, BYPASS, EXTEST, SAMPLE, PRELOAD, HIGHZ, and CLAMP instructions.

For information on the value the IDCODE instruction will return for the 8A34044, see the “Product Identification” table located at the end of this document.

JTAG port signals share five pins with GPIO functions as outlined in Table 23. Assertion of the nTEST input (active low) will place those pins in JTAG mode and the device in non-operational mode. The nMR signal should be asserted when nTEST is negated to ensure the device resumes operational mode in a clean state.

### Table 22. SPI Timing (Cont.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tD1d[a]</td>
<td>Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing[b]</td>
<td>$V_{CCS} = 3.3\text{V}$</td>
<td>$6 + \text{half SCLK period}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CCS} = 2.5\text{V}$</td>
<td>$6 + \text{half SCLK period}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CCS} = 1.8\text{V}$</td>
<td>$6 + \text{half SCLK period}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tD2</td>
<td>SDIO Read Data Hi-Z Time from CS High[c]</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] Measurement performed approximately 1cm away from device pad. Observing at a greater distance on a heavily loaded trace may show slower edge rates and longer delays. This is highly dependent on PCB loading.

[b] Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.

[c] This is the time until the 8A34044 releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

### JTAG Interface

The 8A34044 provides a JTAG interface that can be used in non-operational situations with the device when nTEST control pin is held low. The JTAG interface is compliant with IEEE-1149.1 (2001) and supports the IDCODE, BYPASS, EXTEST, SAMPLE, PRELOAD, HIGHZ, and CLAMP instructions.

For information on the value the IDCODE instruction will return for the 8A34044, see the “Product Identification” table located at the end of this document.

JTAG port signals share five pins with GPIO functions as outlined in Table 23. Assertion of the nTEST input (active low) will place those pins in JTAG mode and the device in non-operational mode. The nMR signal should be asserted when nTEST is negated to ensure the device resumes operational mode in a clean state.

### Table 23. JTAG Signal Mapping

<table>
<thead>
<tr>
<th>Function with nTEST Active (Low)</th>
<th>Function when nTEST Inactive (High)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCK</td>
<td>GPIO[0]</td>
</tr>
<tr>
<td>TMS</td>
<td>GPIO[1]</td>
</tr>
<tr>
<td>TDI</td>
<td>GPIO[2]</td>
</tr>
<tr>
<td>TDO</td>
<td>GPIO[3]</td>
</tr>
<tr>
<td>TRSTn</td>
<td>GPIO[4]</td>
</tr>
</tbody>
</table>
Basic Operating Modes (Synthesizer / Clock Generator / Jitter Attenuator)

Free-Running Synthesizer Operation

Any DPLL or Satellite channel can be used in a free-running synthesizer configuration independently of any of the other channels in the part. When configured as a free-running synthesizer, the blocks shown in Figure 24 are used. An external crystal is used as a reference by the System Analog PLL (APLL) which generates a high-frequency, low phase-noise signal. For information on APLL configuration, see System Analog PLL (APLL).

Figure 24. Free-Running Synthesizer Operation

The high-frequency output signal from the APLL is divided-down by the Fractional Divider block to a frequency from 500MHz to 1GHz (for information, see System Analog PLL (APLL)). The output frequency is unrelated to the APLL frequency since fractional division is used. Note that in synthesizer mode, the Fractional Divider block is not steerable, so it is just performing the divide function. That signal is in turn fed to the output stage, where it is further divided by the integer divider(s) and provided to the output in the selected output format. For more information, see FOD Multiplexing and Output Stages.

Clock Generator Operation

Any DPLL or Satellite channel can be used in a clock generator configuration. When configured as a clock generator as shown in Figure 25, the external crystal input (OSCI) is over-driven (for more information, see Overdriving the XTAL Interface) by an external clock signal which is used as a reference by the System Analog PLL (APLL). The APLL generates a high-frequency, low phase-noise signal from this reference. Note that because the APLL is shared by all channels, this mode is not truly independent for all channels. Each channel can generate unrelated output frequencies via the Fractional Divider. Otherwise, this mode of operation functions the same as the free-running synthesizer operation in the previous section.

Figure 25. Clock Generator Operation
**Synthesizer Disciplined with Oscillator Operation**

If an external oscillator, such as an XO, TCXO or OCXO is used, any channel may have its output frequency disciplined by the oscillator for stability and/or close-in phase noise improvement reasons. When configured as shown in Figure 26, the Fractional Divider is behaving as indicated in the description, but in this case the System Digital PLL (SDPLL) is locked to the oscillator and providing a steering signal to the Fractional Divider. Note that the oscillator may be connected to the dedicated oscillator input pin (XO_DPLL) or to any of the input reference clocks (CLKx / nCLKx). Please refer to the Digital Phase Locked Loop (DPLL) section for details.

**Figure 26. Synthesizer Disciplined with Oscillator Operation**

---

**Jitter Attenuator Operation**

Any DPLL channel can be operated as a Jitter Attenuator independently from any other channel as shown in Figure 27.

**Figure 27. Jitter Attenuator Operation**

---

The high-frequency output signal from the APLL is divided-down by the FOD block to a frequency from 500MHz to 1GHz. The output frequency is unrelated to the APLL frequency since fractional division is used (for information, see System Analog PLL (APLL)). That signal is in turn fed to the output stage, where it is further divided by the integer divider(s) and provided to the output in the selected output format. For more information, see FOD Multiplexing and Output Stages.

The DPLL is locked to the input clock, and therefore there is a digital control signal from the Digital PLL (DPLL) block being used to steer the FOD. This signal will adjust the frequency of the FOD to track the input reference signal the DPLL is locked to. So the steerable FOD is acting as a Digitally Controlled Oscillator (DCO) in this mode. This steering signal may be copied to any other Satellite or DPLL channel so they track the same input. The DPLL logic supports several options on how the phase of the output reacts to changes in which input reference is selected, as well as supporting holdover operation if all relevant inputs are lost. For information on how the input reference clock is selected, see DPLL Input Clock Qualification and Selection; for information on DPLL options and operation, see Digital Phase Locked Loop (DPLL).
Jitter Attenuator Operation with External Digital Loop Filter

For some applications, it may be preferable to use an external digital loop filter implemented in software to control a DPLL channel. This function is supported as shown in Figure 28.

Figure 28. Jitter Attenuator Operation with External Digital Loop Filter

In this case, the phase error measured by the DPLL’s phase detector is digitized and decimated to a user selected update rate and provided via registers for use by an external digital filter (for information, see Digital Phase Locked Loop (DPLL)). That data is read from the 8A34044 and provided to the digital filter algorithm. That algorithm then generates a Frequency Control Word (FCW) and writes that back into 8A34044’s registers. The FCW will provide direct control of the steerable FOD.

Handling of input reference switchover and holdover operation is under control of the external filter algorithm in this case. Necessary control and status signals to handle these cases in external logic can be provided by proper configuration of the GPIO pins, as described in the General Purpose Input/Outputs (GPIOs).

Jitter Attenuator Disciplined with Oscillator Operation

Similarly to the Synthesizer mode being disciplined by an external oscillator, a jitter attenuator may also be similarly disciplined as shown in Figure 29. This provides stability for the DPLL channel when in holdover. Also, when the jitter attenuator is locked, the oscillator may be used to enhance close-in phase noise performance.

Figure 29. Jitter Attenuator Disciplined with Oscillator Operation
Digitally-Controlled Oscillator Operation via External Control

Any DPLL channel can be operated as an externally-controlled DCO independently from any other channel. There are several different control methods that can be used depending on the application needs. Each is described individually in the following sub-sections. Phase and/or frequency updates will be calculated using external methods and written into the 8A34044 over the serial port.

Write-Frequency Mode

For a DPLL or Satellite channel in this mode a Frequency Control Word (FCW) is used to adjust the frequency output of the DCO (by steering the FOD) and the phase detector and loop filter are essentially bypassed. All the filtering is done by an external device and the frequency offset written into the Write Frequency Configuration register is passed on directly to the output clocks, as displayed in Figure 30. When applied, the FCW will not cause any missing pulses or glitches in the output clock, although a large frequency jump may cause issues with devices receiving this clock. The output will remain at this frequency until a new FCW is written.

If supported by the device, Combo Mode can be used to add additional offsets to the write frequency offset.

Figure 30. External DCO Control via Frequency Control Word

The FCW is a 42-bit 2’s-complement value. The FCW has a granularity of $1.11 \times 10^{-10}$ppm and a full range of $+244.20$ppm to -$244.08$ppm of the nominal DCO frequency. A positive value will increase the output frequency and a negative one will decrease the output frequency. The formula for calculation of the FCW from the fractional frequency offset (FFO) is:

$$
FCW = \left[ 1 - \frac{1}{1 + \frac{FFO}{10^6}} \right] \times 2^{53}
$$

Where,

FFO = Fractional Frequency Offset, in ppm

FCW = Frequency Control Word (Positive or Negative Integer)

The value resulting from the above calculation must be converted to a 42-bit 2’s complement value and then sign-extended to 48 bits to be written into the register.

Write frequency mode can be used to make phase changes on the output. For fine resolution, phase changes are done by controlling the DCO’s frequency. Coarse phase adjustments should be done by snap-alignment method by using the Phase Offset registers (for information, see Output Coarse Phase Adjustment). Using the Phase Offset registers is referred to as the snap-alignment method since the output will snap directly to that new phase rather than moving smoothly to it over time. The snap-alignment method provides fast coarse phase alignments, and therefore, it should be used to bring the phase close to the desired value and then use the DCO in write frequency mode to fine tune it. Since write frequency mode is changing the frequency, the phase will move smoothly over time without any jumps.
Increment / Decrement Registers and Pins

The DCO frequency update can also be done by applying a preset frequency offset value to be added or to be subtracted from a cumulative FCW value. The cumulative FCW value functions as described in the previous section.

One or more GPIO pins can be configured to perform the increment or decrement frequency offset function on a specific DCO. For information on how to configure the GPIOs, see General Purpose Input/Outputs (GPIOs).

Write-Phase Mode

In this mode of operation for a DPLL or Satellite channel, the Phase Control Word (PCW) is written by the external control logic over the serial port to directly control the DCO phase with hardware controlled bandwidth and phase slope limiting (see Figure 31). In this mode, the DPLL loop bandwidth and the phase slope limiting are programmable and will affect the output phase as it is adjusted.

The PCW applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop. The update rate needs to be at least 60 times the loop filter bandwidth. As an example, for 0.1Hz per G.8273.2, the update should be greater than 6Hz; but for 17Hz the update should be greater than 1000Hz. The rate of adjustment of phase on the DCO output is controlled by Digital Loop Filter settings. For information on configuring related DPLL parameters such as loop bandwidth and phase slope limiting, see Digital Phase Locked Loop (DPLL). This method allows for a better control of the output clock since all parameters are controlled in hardware. This change will not cause any missing pulses or glitches in the output clock. Also, because the output frequency is changed only at a rate determined by the loop filter, this should not cause any issues, if properly configured, with devices receiving this clock.

Note that the PCW must be reduced over time or the DPLL will continue to adjust the DCO frequency to remove the “phase error”. This can be adjusted by external software.

Figure 31. External DCO Control via Phase Control Word

To assist in the above, there is an optional timer associated with the PCW. This allows a phase control word to be applied for a limited period of time after which it will be automatically reset to zero or placed into holdover by the 8A34044, and therefore, it will avoid the DCO continuing to apply the phase adjustment indefinitely until it reaches its tuning range limits. The timer value is a 16-bit integer that has a granularity of 1 millisecond and a full range of up to 65.535 seconds.

The PCW is a 32-bit 2’s-complement value. The resolution of the PCW is 50ps and the range is ±107.3741824ms. Writing a positive value will result in the output frequency getting faster. This will shorten the clock periods, moving the clock edges to the left as seen on an oscilloscope. A negative value will slow the output frequency.
Adjusting Phase while in Closed Loop Operation

There may be usage scenarios that require adding a phase offset from an external software-controlled process to an output clock that is locked to an input clock. That function can also be supported as shown in Figure 32. In this mode, the amount of phase offset needed consists of two components. The first is dependent on which input the DPLL is locked to. So a phase offset register is provided for each input to allow individual offsets to be specified per-input.

The second part of the phase offset configuration is for each DPLL. There is a register for each DPLL that allows for another offset value to be specified that is independent of which input is active. The actual Phase Offset Value applied will be calculated by the 8A34044 using the per-input phase offset value for the currently active input summed with the phase offset value for the DPLL channel. During input reference switching, this value will be automatically recalculated at any switchover and applied as shown. Note that if an input is used on multiple DPLL channels, it may not be possible to maintain unique values per-input-per-DPLL. The calculated offset value is then summed with the measured phase error for that channel (phase difference between input reference and feedback value) to drive the DPLL to the desired phase.

The Phase Offset Value applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop.

Figure 32. Phase Control in Closed Loop Operation

Combo Mode

The combo mode is shown in Figure 33. In this mode, up to three channels are used, one of which is usually a DPLL channel. Each (receiving) DPLL or Satellite channel can source up to two other DPLLs including the System DPLL. In this mode, one DPLL is locked to an input reference clock, such as a Synchronous Ethernet clock, and can generate output clocks of different frequencies that track the Synchronous Ethernet input reference clock. The second channel is used as a DCO and it will be controlled externally, as an example by an IEEE 1588 clock recovery servo algorithm running in an external processor, or just track the first channel directly. This will not cause any missing pulses or glitches in the output clocks from either channel since all frequency changes are limited by at least one loop filter.

The physical layer clock and its output clock will act as the local oscillator for the DCO, and therefore the DCO can rely on a very stable clock. This is done all inside the device, no need to route the clocks externally. It is also important to be able to control phase transients in the SyncE clock. This can be done by either using an internal filter that will filter the SyncE transients, or by suppressing the SyncE based on SSM clock quality level.
In this example, the IEEE 1588 timestamps are used to calculate the phase offset between the IEEE 1588 master’s 1PPS pulse and the IEEE 1588 slave’s 1PPS pulse and then align the two pulses by moving the slave’s 1PPS pulse in phase. The slave must be able to move the 1PPS pulse by ±0.5s, and the 8A34044 provides this capability.
AC and DC Specifications

Abbreviations Used in this Section

Many signals will be concatenated in the specification tables that follow. Table 24 shows a list of abbreviations used and will be referred to in footnotes for the various other tables.

Table 24. Abbreviated Signal Names and the Detailed Signal Names Referenced by Them

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Signals Referenced by this Abbreviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD_CLKx}$</td>
<td>$V_{DD_CLK}$</td>
</tr>
<tr>
<td>Input CLK</td>
<td>CLK[3:0], nCLK[3:0]</td>
</tr>
<tr>
<td>Output Q</td>
<td>Q[11:0], nQ[11:0]</td>
</tr>
<tr>
<td>Status Outputs</td>
<td>GPIO[9,5:0], SDIO</td>
</tr>
<tr>
<td>GPIO</td>
<td>GPIO[9,5:0]</td>
</tr>
<tr>
<td>$V_{DDx}$</td>
<td>$V_{DDA_PDCP_XTAL}$, $V_{DDA_CLK}$, $V_{DDA_FB}$, $V_{DDA_BG_LC}$, $V_{DDA_DIG}$, $V_{DDA_GPIO_FOD}$, $V_{DDA_DIA_FOD_A}$, $V_{DDA_DIA_FOD_B}$, $V_{DDO_Q0}$, $V_{DDO_Q1}$, $V_{DDO_Q2}$, $V_{DDO_Q3}$, $V_{DDO_Q4}$, $V_{DDO_Q5}$, $V_{DDO_Q6}$, $V_{DDO_Q7}$, $V_{DDO_Q8}$, $V_{DDO_Q9}$, $V_{DDO_Q10}$, $V_{DDO_Q11}$</td>
</tr>
<tr>
<td>$V_{DDO_Qx}$</td>
<td>$V_{DDO_Q0}$, $V_{DDO_Q1}$, $V_{DDO_Q2}$, $V_{DDO_Q3}$, $V_{DDO_Q4}$, $V_{DDO_Q5}$, $V_{DDO_Q6}$, $V_{DDO_Q7}$, $V_{DDO_Q8}$, $V_{DDO_Q9}$, $V_{DDO_Q10}$, $V_{DDO_Q11}$</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8A34044 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 25. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDx[a]</td>
<td>Any voltage supply</td>
<td></td>
<td>-0.5</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Voltage on any input</td>
<td>OSCI[b], OSCO, FILTER, CREG,XTAL</td>
<td>0</td>
<td>2.75</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All other inputs</td>
<td>-0.5</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>IIN</td>
<td>Differential Input Current</td>
<td>Input CLK[a]</td>
<td>±50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IOUT</td>
<td>Output Current - Continuous</td>
<td>Output Q[b]</td>
<td>30</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Status Outputs[a]</td>
<td>25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Output Current - Surge</td>
<td>Output Q</td>
<td>60</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Status Outputs</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ŮJMAX</td>
<td>Maximum Junction Temperature</td>
<td></td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>TS</td>
<td>Storage temperature</td>
<td>-65</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>-</td>
<td>ESD - Human Body Model</td>
<td></td>
<td>2000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>-</td>
<td>ESD - Charged Device Model</td>
<td></td>
<td>1500</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

[a] For information on the signals referenced by this abbreviation, see Table 24.
[b] This limit only applies to the OSCI input when being over-driven by an external signal. No limit is implied when this is connected directly to a crystal.

Recommended Operating Conditions

Table 26. Recommended Operating Conditions[a][b]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TA</td>
<td>Ambient air temperature</td>
<td>-40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature</td>
<td></td>
<td>125</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

[a] It is the user’s responsibility to ensure that device junction temperature remains below the maximum allowed.
[b] All conditions in this table must be met to guarantee device functionality.
## Supply Voltage Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD_CLK} )</td>
<td>Supply Voltage for Input Clock Buffers and Dividers</td>
<td>( V_{DD_CLK} = 3.465 \text{V}, ) PMOS mode</td>
<td>3</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLK} = 3.465 \text{V}, ) NMOS mode</td>
<td>6</td>
<td>7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLK} = 3.465 \text{V}, ) CMOS mode</td>
<td>1.5</td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLK} = 2.625 \text{V}, ) PMOS mode</td>
<td>2.6</td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLK} = 2.625 \text{V}, ) NMOS mode</td>
<td>6</td>
<td>7</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLK} = 2.625 \text{V}, ) CMOS mode</td>
<td>1</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD_CLKx} )</td>
<td>Supply Current for ( V_{DD_CLKx} )</td>
<td>( V_{DD_CLKx} = 3.465 \text{V}, ) PMOS mode</td>
<td>48</td>
<td>55</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DD_CLKx} = 2.625 \text{V}, ) PMOS mode</td>
<td>33</td>
<td>40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DDA_PDCP_XTAL} )</td>
<td>Analog Supply Voltage for oscillator and for SysAPLL Phase detector &amp; Charge Pump</td>
<td></td>
<td>2.375</td>
<td>[e]</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DDA_PDCP_XTAL} )</td>
<td>Supply Current for ( V_{DDA_PDCP_XTAL} )</td>
<td>( V_{DDA_PDCP_XTAL} = 3.3 \text{V} )</td>
<td>48</td>
<td>55</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DDA_PDCP_XTAL} = 2.5 \text{V} )</td>
<td>33</td>
<td>40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DDA_FB} )</td>
<td>Analog Supply Voltage for SysAPLL Feedback Divider</td>
<td>( V_{DDA_PDCP_XTAL} = 1.89 \text{V} )</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DDA_FB} )</td>
<td>Supply Current for ( V_{DDA_FB} )</td>
<td>( V_{DDA_FB} = 1.89 \text{V} )</td>
<td>22</td>
<td>37</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DDA_BG_LC} )</td>
<td>Analog Supply Voltage for SysAPLL Bandgap reference and LC Resonator</td>
<td>( V_{DDA_BG_LC} = 3.465 \text{V} )</td>
<td>125</td>
<td>147</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DDA_BG_LC} = 2.625 \text{V} )</td>
<td>88</td>
<td>93</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DDA_BG_LC} )</td>
<td>Supply Current for ( V_{DDA_BG_LC} )</td>
<td>( V_{DDA_BG_LC} = 1.89 \text{V} )</td>
<td>190</td>
<td>380</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DD_DIG} )</td>
<td>Digital Supply Voltage</td>
<td>( V_{DD_DIG} = 1.89 \text{V} )</td>
<td>1.14</td>
<td>[f]</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DD_DIG} )</td>
<td>Supply Current for ( V_{DD_DIG} )</td>
<td>( V_{DD_DIG} = 1.89 \text{V} )</td>
<td>180</td>
<td>295</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
Table 27. Power Supply DC Characteristics[^a][^b]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{DD_GPIO_FOD}[^g]</td>
<td>Supply Voltage for:</td>
<td>▪ GPIO and other status control signals</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>▪ FOD_5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{DD_GPIO_FOD}</td>
<td>Supply Current for V\textsubscript{DD_GPIO_FOD}[^h]</td>
<td>V\textsubscript{DD_GPIO_FOD} = 1.89V</td>
<td>30</td>
<td>53</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Base current (FOD Off)</td>
<td>I\textsubscript{DD(FODBASE)}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Adder for FOD at 500MHz</td>
<td>I\textsubscript{DD(FODPERFOD)}</td>
<td>30</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Adder per 1MHz over 500MHz on FOD</td>
<td>I\textsubscript{DD(FODPERMHZ)}</td>
<td></td>
<td>0.012</td>
<td></td>
<td>mA/MHz</td>
</tr>
<tr>
<td>V\textsubscript{DDA_DIA_FOD_A}</td>
<td>Supply Voltage for:</td>
<td>▪ FOD_0</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>▪ FOD_0 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_1 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_4 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_5 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_5 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{DDA_DIA_FOD_A}</td>
<td>Supply Current for V\textsubscript{DDA_DIA_FOD_A}[^i]</td>
<td>V\textsubscript{DDA_DIA_FOD_A} = 1.89V</td>
<td>45</td>
<td>85</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Base current (FODs Off)</td>
<td>I\textsubscript{DD(BASE)}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Adder for FOD at 500MHz</td>
<td>I\textsubscript{DD(DCOPERFOD)}</td>
<td>30</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Adder for each FOD control (if enabled) at 500MHz</td>
<td>I\textsubscript{DD(CTLPERFOD)}</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Adder per 1MHz over 500MHz on FOD</td>
<td>I\textsubscript{DD(DCOPERMHZ)}</td>
<td></td>
<td>0.012</td>
<td></td>
<td>mA/MHz</td>
</tr>
<tr>
<td></td>
<td>Adder per 1MHz over 500MHz on FOD control that is enabled</td>
<td>I\textsubscript{DD(CTLPERMHZ)}</td>
<td></td>
<td>0.018</td>
<td></td>
<td>mA/MHz</td>
</tr>
<tr>
<td>V\textsubscript{DDA_DIA_FOD_B}</td>
<td>Supply Voltage for:</td>
<td>▪ FOD_2</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>▪ FOD_2 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_3 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_6 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ FOD_7 control logic</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[^a]: IDT is not responsible for the accuracy of the data contained in this table.
[^b]: Contact IDT for accuracy and verification of the data contained in this table.
Table 27. Power Supply DC Characteristics[a][b]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD_DIA_FOD_B[1]</td>
<td>Supply Current for VDDA_DIA_FOD_B[1]</td>
<td>VDDA_DIA_FOD_B = 1.89V Base current (FODs Off) IDD(BASE)</td>
<td>69</td>
<td>110</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adder for FOD at 500MHz IDD(DCOPERFOD)</td>
<td>30</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adder for each FOD control (if enabled) at 500MHz IDD(CTLPERFOD)</td>
<td>10</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adder per 1MHz over 500MHz on FOD IDD(DCOPERMHZ)</td>
<td>0.012</td>
<td>mA/MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Adder per 1MHz over 500MHz on FOD control that is enabled IDD(CTLPERMHZ)</td>
<td>0.012</td>
<td>mA/MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDDO_Qx[k]</td>
<td>Output Clock Q Supply Voltage[l]</td>
<td>1.14</td>
<td>3.465</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] VSS = 0V, TA = -40°C to 85°C
[b] Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply being all enabled and running at full capacity. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device. Please refer to the section Power Consumption to determine actual consumption for the exact configuration of the device.
[c] Supports 1.8V±5%, 2.5V±5% or 3.3V±5% operation, not a continuous range.
[d] IDD_CLKx denotes the current consumed by the appropriate VDD_CLKx supply voltage
[e] Supports 2.5V±5% or 3.3V±5% operation, not a continuous range.
[f] Supports 1.2V±5% or 1.8V±5% operation, not a continuous range.
[g] GPIO and status/control pins will support only 1.8V on this device due to sharing of this pin with the FOD blocks which only support 1.8V operation.
[h] The IDD_GPIO_FOD current consumed is dependent on the number of FODs attached to the voltage rail that are supported and the frequency of operation of those FODs. A calculation needs to be performed using the formula below, where fFOD is the operating frequency of each FOD, NumFOD is the number of FODs on that supply that are enabled. Note that only the base current is needed if all FODs are disabled. Current for the GPIO and status / control signals is included in the base value.

\[
I_{DD(FOD)} = I_{DD(BASE)} + \text{NumFOD} \times I_{DD(FODPERFOD)} + \sum_{\text{operatingDCO}} (f_{FOD} - 500) \times I_{DD(FODPERMHZ)}
\]

[i] The IDD_DIA current consumed is dependent on the number of FODs attached to the voltage rail that are supported and the frequency of operation of those FODs. A calculation needs to be performed using the formula below, where fFOD is the operating frequency of each FOD, NumFOD is the number of FODs on that supply that are enabled. Note that only the base current is needed if all FODs are disabled.

\[
I_{DD(DCOQ8)} = I_{DD(BASE)} + I_{DD(DCOPERFOD)} + (f_{FOD} - 500) \times I_{DD(DCOPERMHZ)} + \sum_{\text{operatingCTRL}} (f_{FOD} - 500) \times I_{DD(CTLPERMHZ)}
\]

[j] VDDA_DIA_FOD_B consumes higher current than VDDA_DIA_FOD_A because it has some additional circuitry, besides the FODs on it.
[k] Please refer to Table 24 for details on the signals referenced by this abbreviation.
[l] Currents for the outputs are shown in Table 28 or Table 29 as appropriate for the mode the individual output is operating in.
Table 28. Output Supply Current (Output Configured as Differential)[a][b][c]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>SWING[d] = 00</th>
<th>SWING = 01</th>
<th>SWING = 10</th>
<th>SWING = 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDDO_Qx[e]</td>
<td>Qx / nQx Supply Current[f]</td>
<td>V_DDO_Qx[g] = 3.465V</td>
<td>15</td>
<td>22</td>
<td>17</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 2.625V</td>
<td>14</td>
<td>20</td>
<td>16</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.89V</td>
<td>14</td>
<td>19</td>
<td>15</td>
<td>20</td>
</tr>
</tbody>
</table>

[a] Output current consumption is not affected by any of the core device power supply voltage levels.
[b] Internal dynamic switching current at maximum f_OUT is included.
[c] V_DDO_Qx = 3.3V±5% or 2.5V±5% or 1.8V±5%, V_SS = 0V, T_A = -40°C to 85°C.
[d] Refers to the output voltage (swing) setting programmed into device registers for each output.
[e] IDDO_Qx denotes the current consumed by each V_DDO_Qx supply.
[g] For information on the signals referenced by this abbreviation, see Table 24.

Table 29. Output Supply Current (Output Configured as LVCMOS)[a][b][c]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>TERM[d] = 00</th>
<th>TERM = 01</th>
<th>TERM = 10</th>
<th>TERM = 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDDO_Qx[e]</td>
<td>Qx, nQx Supply Current[f]</td>
<td>V_DDO_Qx[g] = 3.465V</td>
<td>24</td>
<td>32</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 2.625V</td>
<td>18</td>
<td>25</td>
<td>19</td>
<td>27</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.89V</td>
<td>12</td>
<td>20</td>
<td>14</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.575V</td>
<td>9</td>
<td>17</td>
<td>11</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.26V</td>
<td>6</td>
<td>13</td>
<td>6</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>Qx enabled and nQx Tri-stated</td>
<td>V_DDO_Qx[g] = 3.465V</td>
<td>14</td>
<td>23</td>
<td>14</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 2.625V</td>
<td>11</td>
<td>19</td>
<td>11</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.89V</td>
<td>9</td>
<td>16</td>
<td>10</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.575V</td>
<td>8</td>
<td>15</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDO_Qx = 1.26V</td>
<td>5</td>
<td>12</td>
<td>5</td>
<td>12</td>
</tr>
</tbody>
</table>

[a] Output current consumption is not affected by any of the core device power supply voltage levels.
[b] Internal dynamic switching current at maximum f_OUT is included.
[c] V_SS = 0V, T_A = -40°C to 85°C
[d] Refers to the LVCMOS output drive strength (termination) setting programmed into device registers for each output.
[e] IDDO_Qx denotes the current consumed by each V_DDO_Qx supply.
[g] For information on the signals referenced by this abbreviation, see Table 24.
[h] Measured with outputs unloaded.
### DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>nMR, nTEST, GPIO[9,5:0], SCLK, SDIO, SDI_A1, CS_A0</td>
<td>$V_{DD,GPIO,FOD} = 1.8V \pm 5%$</td>
<td>$0.65 \times V_{DD,GPIO,FOD}$</td>
<td>$V_{DD,GPIO,FOD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>XO_DPLL</td>
<td>$V_{DD,DIG} = 1.8V \pm 5%$</td>
<td>1.17</td>
<td>3.465V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>CLK[3:0], nCLK[3:0]$^e$</td>
<td>$V_{DD,CLK} = 3.3V \pm 5%$</td>
<td>2</td>
<td>$V_{DD,CLK} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,CLK} = 2.5V \pm 5%$</td>
<td>1.7</td>
<td>$V_{DD,CLK} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,CLK} = 1.8V \pm 5%$</td>
<td>0.65 $\times V_{DD,CLK}$</td>
<td>$V_{DD,CLK} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>nMR, nTEST, GPIO[9,5:0], SCLK, SDIO, SDI_A1, CS_A0</td>
<td>$V_{DD,GPIO,FOD} = 1.8V \pm 5%$</td>
<td>-0.3</td>
<td>$0.35 \times V_{DD,GPIO,FOD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>XO_DPLL</td>
<td>$V_{DD,DIG} = 1.8V \pm 5%$</td>
<td>-0.3</td>
<td>$0.35 \times V_{DD,DIG}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,DIG} = 1.2V \pm 5%$</td>
<td>-0.3</td>
<td>$0.35 \times V_{DD,DIG}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,CLK} = 3.3V \pm 5%$</td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,CLK} = 2.5V \pm 5%$</td>
<td>-0.3</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{DD,CLK} = 1.8V \pm 5%$</td>
<td>-0.3</td>
<td>$0.35 \times V_{DD,CLK}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>nMR, nTEST, GPIO[9,5:0], SCLK, SDIO, SDI_A1, CS_A0</td>
<td>$V_{IN} = V_{DD,GPIO,FOD} = V_{DD,GPIO,FOD} \ (max)$</td>
<td>5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>XO_DPLL</td>
<td>$V_{IN} = 3.465V$, $V_{DD,DIG} = V_{DD,DIG} \ (max)$</td>
<td>150</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>CLK[3:0]</td>
<td>$V_{IN} = V_{DD,CLK} = V_{DD,CLK} \ (max)$</td>
<td>150</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>nCLK[3:0]</td>
<td></td>
<td>5</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>nMR, nTEST, GPIO[9,5:0], SCLK, SDIO, SDI_A1, CS_A0</td>
<td>$V_{IN} = 0V$, $V_{DD,GPIO,FOD} = V_{DD,GPIO,FOD} \ (max)$</td>
<td>-150</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>XO_DPLL</td>
<td>$V_{IN} = 0V$, $V_{DD,DIG} = V_{DD,DIG} \ (max)$</td>
<td>-5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>CLK[3:0]</td>
<td>$V_{IN} = 0V$, $V_{DD,CLK} = V_{DD,CLK} \ (max)$</td>
<td>-5</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>nCLK[3:0]</td>
<td></td>
<td>-150</td>
<td>μA</td>
</tr>
</tbody>
</table>
Table 30.  LVCMOS/LVTTL DC Characteristics\textsuperscript{[a][b][c][d][e]} (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DD_GPIO_FOD} = 1.8\text{V} \pm 5%$, $I_{OH} = -100\mu\text{A}$</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>0.2</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>-0.2</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output Low Voltage</td>
<td>$V_{DD_GPIO_FOD} = 1.8\text{V} \pm 5%$, $I_{OH} = -2\text{mA}$</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>0.45</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>-0.45</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output High Voltage</td>
<td>$V_{DD_GPIO_FOD} = 1.8\text{V} \pm 5%$, $I_{OL} = 100\mu\text{A}$</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>0.2</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>-0.2</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$V_{DD_GPIO_FOD} = 1.8\text{V} \pm 5%$, $I_{OL} = 2\text{mA}$</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>0.45</td>
<td>$V_{DD_GPIO_FOD}$</td>
<td>-0.45</td>
</tr>
</tbody>
</table>

\textsuperscript{[a]} $V_{IL}$ should not be less than -0.3V.
\textsuperscript{[b]} 3.3V characteristics in accordance with JESD8C-01,
2.5V characteristics in accordance with JESD8-5A.01,
1.8V characteristics in accordance with JESD8-7A,
1.5V characteristics in accordance with JESD8-11A.01,
1.2V characteristics in accordance with JESD8-12A.01
\textsuperscript{[c]} $V_{SS} = 0\text{V}$, $T_A = -40\degree\text{C}$ to 85\degree\text{C}.
\textsuperscript{[d]} When Output Q are configured as LVCMOS, their output characteristics are specified in Table 35.
\textsuperscript{[e]} Input pair used as two single-ended clocks rather than as a differential clock.

Table 31.  Differential Input DC Characteristics\textsuperscript{[a]}

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$V_{IN} = V_{DD_CLK} = V_{DD_CLK}$ (max)</td>
<td>150</td>
<td>5</td>
<td>$V_{DD_CLK}$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{IN} = 0\text{V}$, $V_{DD_CLK} = V_{DD_CLK}$ (max)</td>
<td>-5</td>
<td>-150</td>
<td>0.15</td>
<td>$V_{DD_CLK}$</td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Peak-to-Peak Voltage\textsuperscript{[b][c]}</td>
<td>Any input protocol</td>
<td>0.15</td>
<td>1.3</td>
<td>0.1</td>
<td>$V_{DD_CLK}$</td>
</tr>
<tr>
<td>$V_{CMR}$</td>
<td>Common Mode Input Voltage\textsuperscript{[b][c][d]}</td>
<td>Input protocol = HCSL, HSTL, SSTL, LVDS, LVPECL, CML</td>
<td>0.1</td>
<td>0.7</td>
<td>0.1</td>
<td>$V_{DD_CLK}$</td>
</tr>
</tbody>
</table>

\textsuperscript{[a]} $V_{SS} = 0\text{V}$, $T_A = -40\degree\text{C}$ to 85\degree\text{C}.
\textsuperscript{[b]} $V_{IL}$ should not be less than -0.3V.
\textsuperscript{[c]} $V_{PP}$ is the single-ended amplitude of the output signal. The differential specs is 2$^*V_{PP}$.
\textsuperscript{[d]} Common mode voltage is defined as the cross-point.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OVS}^{[e]})</td>
<td>Output Voltage Swing</td>
<td>SWING = 00(^{[f]})</td>
<td>336</td>
<td>402</td>
<td>462</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 01</td>
<td>478</td>
<td>605</td>
<td>698</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 10</td>
<td>658</td>
<td>791</td>
<td>910</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 11</td>
<td>739</td>
<td>870</td>
<td>997</td>
<td></td>
</tr>
<tr>
<td>(V_{CMR}^{[g]})</td>
<td>Output Common Mode Voltage</td>
<td>CENTER = 00(^{[h]})</td>
<td>0.86</td>
<td>0.95</td>
<td>1.07</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 001</td>
<td>0.98</td>
<td>1.14</td>
<td>1.28</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 010</td>
<td>1.13</td>
<td>1.33</td>
<td>1.51</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 011</td>
<td>1.30</td>
<td>1.53</td>
<td>1.73</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 100</td>
<td>1.46</td>
<td>1.73</td>
<td>1.95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 101</td>
<td>1.63</td>
<td>1.93</td>
<td>2.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 110</td>
<td>1.80</td>
<td>2.12</td>
<td>2.39</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 111</td>
<td>1.96</td>
<td>2.30</td>
<td>2.59</td>
<td></td>
</tr>
</tbody>
</table>

\[a\] For information on the signals referenced by this abbreviation, see Table 24.

\[b\] Terminated with 100Ω across Qx and nQx.

\[c\] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 001 or 010.

\[d\] If LVPECL operation is desired, the user should select SWING = 10 and CENTER = 101 or 110 for 3.3V LVPECL, and SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation.

\[e\] \(V_{OVS}\) is the single-ended amplitude of the output signal. The differential specs is \(2V_{OVS}\).

\[f\] Refers to the differential voltage swing setting programmed into device registers for each output.

\[g\] Not all \(V_{CMR}\) selections can be supported with particular \(V_{DDO,Qx}\) and \(V_{OVS}\) settings. For information on which combinations are supported, see Table 17.

\[h\] Refers to the differential voltage crossing point (center voltage) setting programmed into device registers for each output.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOVS[e]</td>
<td>Output Voltage Swing</td>
<td>SWING = 00[f]</td>
<td>295</td>
<td>393</td>
<td>448</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 01</td>
<td>457</td>
<td>591</td>
<td>677</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 10</td>
<td>587</td>
<td>761</td>
<td>881</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 11</td>
<td>733</td>
<td>835</td>
<td>943</td>
<td></td>
</tr>
<tr>
<td>VCMR[g]</td>
<td>Output Common Mode Voltage</td>
<td>CENTER = 000[h]</td>
<td>0.85</td>
<td>0.93</td>
<td>1.03</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 001</td>
<td>0.94</td>
<td>1.10</td>
<td>1.23</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 010</td>
<td>1.09</td>
<td>1.28</td>
<td>1.44</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 011</td>
<td>1.24</td>
<td>1.46</td>
<td>1.65</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 100</td>
<td>1.39</td>
<td>1.65</td>
<td>1.86</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 101</td>
<td>Not Supported</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 110</td>
<td>Not Supported</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 111</td>
<td>Not Supported</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] For information on the signals referenced by this abbreviation, see Table 24.
[b] Terminated with 100Ω across Qx and nQx.
[c] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 001 or 010.
[d] If LVPECL operation is desired, the user should select SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation. For VDDO = 2.5V, 3.3V LVPECL levels cannot be generated.
[e] VOVS is the single-ended amplitude of the output signal. The differential specs is 2*VOVS.
[f] Refers to the differential voltage swing setting programed into device registers for each output.
[g] Not all VCMR selections can be supported with particular VDDO_Qx and VOVS settings. For information on which combinations are supported, see Table 17.
[h] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.
Table 34. Differential Output DC Characteristics (V_DDO_Qx = 1.8V+5%, V_SS = 0V, T_A = -40°C to 85°C)[a][b][c]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{OVS}[^d]</td>
<td>Output Voltage Swing</td>
<td>SWING = 00[^e]</td>
<td>299</td>
<td>411</td>
<td>485</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 01</td>
<td>470</td>
<td>586</td>
<td>700</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 10</td>
<td>582</td>
<td>713</td>
<td>852</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SWING = 11</td>
<td>612</td>
<td>750</td>
<td>899</td>
<td></td>
</tr>
<tr>
<td>V_{CMR}[^f]</td>
<td>Output Common Mode Voltage</td>
<td>CENTER = 00[^g]</td>
<td>0.84</td>
<td>0.91</td>
<td>0.99</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 001</td>
<td>0.91</td>
<td>1.05</td>
<td>1.18</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 010</td>
<td>1.05</td>
<td>1.21</td>
<td>1.36</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 011</td>
<td></td>
<td></td>
<td></td>
<td>Not Supported</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 101</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CENTER = 111</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] For information on the signals referenced by this abbreviation, see Table 24.
[b] Terminated with 100Ω across Qx and nQx.
[c] If LVDS operation is desired, the user should select SWING = 00 and CENTER = 010.
[d] V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.
[e] Refers to the differential voltage swing setting programed into device registers for each output.
[f] Not all V_{CMR} selections can be supported with particular V_DDO_Qx and V_{OVS} settings. For information on which combinations are supported, see Table 17.
[g] Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.
### Table 35. LVCMOS Clock Output DC Characteristics[^a][^b]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>TERM[^c] = 00</th>
<th>TERM = 01</th>
<th>TERM = 10</th>
<th>TERM = 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{OH}</td>
<td>Output</td>
<td>V_{DDO_Qx} = 3.3V±5%</td>
<td>0.74 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td>High Voltage</td>
<td>V_{DDO_Qx} = 2.5V±5%</td>
<td>0.70 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.8V±5%</td>
<td>0.65 × V_{DDO_ Qx}</td>
<td>0.71 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
<td>0.75 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.5V±5%</td>
<td>0.61 × V_{DDO_ Qx}</td>
<td>0.66 × V_{DDO_ Qx}</td>
<td>0.70 × V_{DDO_ Qx}</td>
<td>0.72 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.2V±5%</td>
<td>0.56 × V_{DDO_ Qx}</td>
<td>0.59 × V_{DDO_ Qx}</td>
<td>0.63 × V_{DDO_ Qx}</td>
<td>0.66 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output</td>
<td>V_{DDO_Qx} = 3.3V±5%</td>
<td>0.29 × V_{DDO_ Qx}</td>
<td>0.25 × V_{DDO_ Qx}</td>
<td>0.25 × V_{DDO_ Qx}</td>
<td>0.25 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td>Low Voltage</td>
<td>V_{DDO_Qx} = 2.5V±5%</td>
<td>0.32 × V_{DDO_ Qx}</td>
<td>0.27 × V_{DDO_ Qx}</td>
<td>0.25 × V_{DDO_ Qx}</td>
<td>0.25 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.8V±5%</td>
<td>0.39 × V_{DDO_ Qx}</td>
<td>0.33 × V_{DDO_ Qx}</td>
<td>0.30 × V_{DDO_ Qx}</td>
<td>0.26 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.5V±5%</td>
<td>0.44 × V_{DDO_ Qx}</td>
<td>0.38 × V_{DDO_ Qx}</td>
<td>0.35 × V_{DDO_ Qx}</td>
<td>0.31 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.2V±5%</td>
<td>0.50 × V_{DDO_ Qx}</td>
<td>0.46 × V_{DDO_ Qx}</td>
<td>0.42 × V_{DDO_ Qx}</td>
<td>0.38 × V_{DDO_ Qx}</td>
</tr>
<tr>
<td>Z_{OUT}</td>
<td>Output</td>
<td>V_{DDO_Qx} = 3.3V±5%</td>
<td>35</td>
<td>25</td>
<td>21</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td>Impedance</td>
<td>V_{DDO_Qx} = 2.5V±5%</td>
<td>31</td>
<td>23</td>
<td>20</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.8V±5%</td>
<td>42</td>
<td>31</td>
<td>25</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.5V±5%</td>
<td>71</td>
<td>47</td>
<td>35</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{DDO_Qx} = 1.2V±5%</td>
<td>101</td>
<td>86</td>
<td>66</td>
<td>49</td>
</tr>
</tbody>
</table>

[^a]: V_{SS} = 0V, T_{A} = -40°C to 85°C.
[^b]: V_{DDO_Qx} is used to refer to the appropriate V_{DDO_Qx} power supply voltage for each output. For more information, see Table 24 and the “Pin Description” table.
[^c]: This refers to the register settings for the LVCMOS output drive strength within the device.
### Table 36. Input Frequency Characteristics\[^{[a]}\]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>f\textsubscript{IN}</td>
<td>Input Frequency</td>
<td>OSCI, OSCO</td>
<td>Using a Crystal[^{[b]}]</td>
<td>25</td>
<td>54</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Over-driving Crystal Input Doubler Logic Enabled[^{[c]}]</td>
<td>25</td>
<td>62.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Over-driving Crystal Input Doubler Logic Disabled</td>
<td>50</td>
<td>125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Input CLK[^{[d][e]}]</td>
<td>Differential Mode</td>
<td>0.001</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Single-ended Mode</td>
<td>0.001</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GPIO</td>
<td></td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>f\textsubscript{IN}</td>
<td>Input Frequency</td>
<td>XO_DPLL</td>
<td></td>
<td>1</td>
<td>150[^{[f]}]</td>
<td>MHz</td>
</tr>
<tr>
<td>f\textsubscript{SCLK}</td>
<td>Serial Port Clock SCLK (slave mode)</td>
<td>I\textsuperscript{2}C Operation</td>
<td></td>
<td>100</td>
<td>1200</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SPI Operation</td>
<td></td>
<td>0.1</td>
<td>50</td>
<td>MHz</td>
</tr>
</tbody>
</table>

\[^{[a]}\] V\textsubscript{SS} = 0V, T\textsubscript{A} = -40°C to 85°C

\[^{[b]}\] For crystal characteristics, see Table 37.

\[^{[c]}\] Refer to Overdriving the XTAL Interface.

\[^{[d]}\] For information on the signals referenced by this abbreviation, see Table 24.

\[^{[e]}\] For proper device operation, the input frequency must be divided down to 150MHz or less (DPLL Phase Detector maximum frequency = 150MHz).

\[^{[f]}\] If the System DPLL needs to be driven with a higher frequency, one of the CLK\textsubscript{x} / nCLK\textsubscript{x} inputs can be routed via register settings to the System DPLL instead of using XO\_DPLL.

### Table 37. Crystal Characteristics\[^{[a]}\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td>Fundamental</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>C\textsubscript{L} = 18pF, crystal frequency (\leq) 40MHz</td>
<td>25</td>
<td>54</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C\textsubscript{L} = 18pF, crystal frequency &gt; 40MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td>C\textsubscript{L} = 12pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Capacitance (C\textsubscript{L})</td>
<td></td>
<td>12</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

\[^{[a]}\] V\textsubscript{SS} = 0V, T\textsubscript{A} = -40°C to 85°C
## AC Electrical Characteristics

Table 38. AC Characteristics\[^{[a] [b]}\]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{VCO} )</td>
<td>Analog PLL VCO Operating Frequency</td>
<td>( V_{DDA_X} = 3.3V \pm 5% )</td>
<td>13.4</td>
<td>13.8</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DDA_X} = 2.5V \pm 5% )</td>
<td>13.5</td>
<td>13.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{FOD} )</td>
<td>Fractional Output Divider Operating Frequency</td>
<td>Measured with output divider set to /1</td>
<td>500</td>
<td>1000</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{OUT} )</td>
<td>Output Frequency</td>
<td>Differential Output</td>
<td>0.0000005</td>
<td>1000</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVCMOS Output</td>
<td>0.0000005</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta f_{OUT} )</td>
<td>Output Frequency Accuracy[^{[d]}]</td>
<td>Switchover or Entering Holdover State</td>
<td>0</td>
<td>ppb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Initial Frequency Offset[^{[e]}]</td>
<td></td>
<td>1</td>
<td>ppb</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Phase Change in Fully Hitless Switching[^{[f]}]</td>
<td>Input references with phase difference &lt; 100( \mu )s</td>
<td>350</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input references with phase difference ( \geq 100\mu )s</td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SK} )</td>
<td>Output to Output Skew[^{[g] [h]}]</td>
<td>Any two differential outputs[^{[i]}]</td>
<td>80</td>
<td>160</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any two outputs configured as LVCMOS in-phase[^{[j]}]</td>
<td>Any two outputs configured as LVCMOS in-phase[^{[j]}]</td>
<td>100</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DDQ_{QX}} = 3.3V \pm 5% , 2.5V \pm 5% , 1.8V \pm 5% or 1.5V \pm 5% )</td>
<td>160</td>
<td>360</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Test Condition</td>
<td>Minimum</td>
<td>Typical</td>
<td>Maximum</td>
<td>Units</td>
</tr>
<tr>
<td>--------</td>
<td>-----------</td>
<td>----------------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>--------</td>
</tr>
<tr>
<td>tSK(B)</td>
<td>Output to Output Skew within a Bank[9][10]</td>
<td>Differential Outputs</td>
<td>1st Bank: Q0, Q1, Q6, Q7</td>
<td>25</td>
<td>65</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2nd Bank: Q2, Q3, Q4, Q5</td>
<td>25</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3rd Bank[11]: Q8, Q11</td>
<td>30</td>
<td>65</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4th Bank: Q9, Q10</td>
<td>30</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Outputs Configured as LVCMOS in-phase</td>
<td>1st Bank: Q0, Q1, Q6, Q7</td>
<td>30</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2nd Bank: Q2, Q3, Q4, Q5</td>
<td>30</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3rd Bank[11]: Q8, Q11</td>
<td>30</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4th Bank: Q9, Q10</td>
<td>30</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q to nQ of same output pair, cfg. as LVCMOS in-phase</td>
<td>1st Bank: Q0, Q1, Q6, Q7</td>
<td>50</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2nd Bank: Q2, Q3, Q4, Q5</td>
<td>50</td>
<td>225</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3rd Bank[11]: Q8, Q11</td>
<td>50</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4th Bank: Q9, Q10</td>
<td>50</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 3.3V±5% or 2.5V±5% or 1.8V±5%</td>
<td>10</td>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 1.5V±5% or 1.2V±5%</td>
<td>15</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔtSK</td>
<td>Temperature Variation[l] Output-Output</td>
<td></td>
<td>4</td>
<td>ps/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tALIGN</td>
<td>Input - Output Alignment Variation[m]</td>
<td>Delay variation as shown in Figure 34 for any CLK/CLKn input pair to any Q/Qn output pair in differential mode when using internal loopback.</td>
<td>-500</td>
<td>500</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>ΔtALIGN</td>
<td>Temperature Variation[n] Input-Output</td>
<td></td>
<td>4</td>
<td>ps/°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 38. AC Characteristics[^a][^b] (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>tR / tF</td>
<td>Differential Output[^n][^o]</td>
<td>VDDO_Qx[^p] = 3.3V±5%, 2.5V±5% or 1.8V±5%</td>
<td>SWING[^q] = 00</td>
<td>100</td>
<td>450</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SWING = 01</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SWING = 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SWING = 11</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 3.3V±5%</td>
<td>TERM[^s] = 00</td>
<td>100</td>
<td>254</td>
<td>380</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 01</td>
<td>100</td>
<td>262</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 10</td>
<td>110</td>
<td>275</td>
<td>460</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 11</td>
<td>115</td>
<td>268</td>
<td>510</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVCMOS Output[^l]</td>
<td>VDDO_Qx = 3.3V±5%</td>
<td>TERM = 00</td>
<td>115</td>
<td>285</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 01</td>
<td>120</td>
<td>293</td>
<td>470</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 10</td>
<td>120</td>
<td>315</td>
<td>525</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 11</td>
<td>140</td>
<td>347</td>
<td>565</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 2.5V±5%</td>
<td>TERM = 00</td>
<td>205</td>
<td>417</td>
<td>590</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 01</td>
<td>205</td>
<td>458</td>
<td>715</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 10</td>
<td>230</td>
<td>459</td>
<td>800</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 11</td>
<td>235</td>
<td>482</td>
<td>880</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 1.8V±5%</td>
<td>TERM = 00</td>
<td>415</td>
<td>558</td>
<td>730</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 01</td>
<td>545</td>
<td>747</td>
<td>985</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 10</td>
<td>615</td>
<td>890</td>
<td>1145</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 11</td>
<td>690</td>
<td>1011</td>
<td>1305</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDO_Qx = 1.5V±5%[^l]</td>
<td>TERM = 00</td>
<td>800</td>
<td>986</td>
<td>1250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 01</td>
<td>1180</td>
<td>1416</td>
<td>1835</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 10</td>
<td>1415</td>
<td>1715</td>
<td>2195</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TERM = 11</td>
<td>1650</td>
<td>1980</td>
<td>2520</td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Test Condition</td>
<td>Minimum</td>
<td>Typical</td>
<td>Maximum</td>
<td>Units</td>
</tr>
<tr>
<td>--------</td>
<td>-----------</td>
<td>----------------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>-------</td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td>Differential Output</td>
<td>PULSE = 50% f(_{\text{OUT}}) &lt; 500MHz</td>
<td>47</td>
<td>50</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>500MHz ≤ f(_{\text{OUT}}) &lt; 800MHz</td>
<td>45</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f(_{\text{OUT}}) ≥ 800MHz</td>
<td>40</td>
<td>50</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVCMOS PULSE = 50% V(_{\text{DDO}_x}) = 3.3V or 2.5V</td>
<td>47</td>
<td>50</td>
<td>53</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V(_{\text{DDO}_x}) = 1.8V or 1.5V</td>
<td>45</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V(_{\text{DDO}_x}) = 1.2V</td>
<td>42</td>
<td>50</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>Any Output Type Operating as a Frame or Sync Pulse</td>
<td>PULSE = Sync Pulse, 100ns</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 1μs</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 10μs</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 100μs</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 1ms</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 10ms</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Sync Pulse, 100ms</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Frame Pulse, 0.2UI</td>
<td>0.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Frame Pulse, 1UI</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PULSE = Frame Pulse, 2UI</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>tjit(Φ)</td>
<td>Phase Jitter, RMS (Random)([l])</td>
<td>10kHz to 20MHz 122.88MHz</td>
<td>133</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>49.152MHz 156.25MHz</td>
<td>156</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>245.76MHz</td>
<td>115</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>312.5MHz</td>
<td>146</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>322.265625MHz</td>
<td>155</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>983.04MHz</td>
<td>109</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10kHz to 20MHz 122.88MHz</td>
<td>138</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>49.152MHz 156.25MHz</td>
<td>153</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>245.76MHz</td>
<td>126</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>312.5MHz</td>
<td>147</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>322.265625MHz</td>
<td>160</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>983.04MHz</td>
<td>104</td>
<td></td>
<td></td>
<td>fs</td>
</tr>
</tbody>
</table>

\([a]\)\([b]\)\([l]\): [Note]: (Please refer to the datasheet for detailed information.)
### Table 38. AC Characteristics[^a][^b] (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
</table>
|        | PSRR      |                 | f\_NOISE = 10kHz  
V\_DDO\_Qx = 3.3V |         | -48.3   |         | dBc   |
|        |           |                 | f\_NOISE = 25kHz  
V\_DDO\_Qx = 3.3V |         | -50.5   |         |       |
|        |           |                 | f\_NOISE = 50kHz  
V\_DDO\_Qx = 3.3V |         | -52.6   |         |       |
|        |           |                 | f\_NOISE = 100kHz 
V\_DDO\_Qx = 3.3V |         | -74.3   |         |       |
|        |           |                 | f\_NOISE = 500kHz 
V\_DDO\_Qx = 1.8V |         | -59.5   |         |       |
|        |           |                 | f\_NOISE = 1MHz   
V\_DDO\_Qx = 1.8V |         | -64.5   |         |       |
|        | t\_startup| Start-up Time[^i] | Regulators  
Ready[^i] | 3 |         | μs      |       |
|        |           |                 | Internal OTP  
Start-up | Synthesizer mode | 7 | 10 | ms |
|        |           |                 |         | DPLL mode, with a loop  
bandwidth setting of 300Hz[^i] | 1.5 |         | s |

[^a]: V\_SS = 0V, T\_A = -40°C to 85°C.
[^b]: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
[^c]: V\_DDA\_X refers to V\_DDA\_PDCP, V\_DDA\_XTAL, V\_DDA\_LC, and V\_DDA\_BG.
[^d]: Long-term frequency error with respect to the DPLL input reference. The typical value shown assumes the DPLL has been phase-locked to a stable input reference for at least 306 minutes (based on a 0.1mHz advanced holdover filter setting) before going into an advanced holdover state on disqualification of the input reference.
[^e]: This parameter will vary with the quality of the reference to the system DPLL. The typical value shown assumes an ideal reference used for the system DPLL.
[^f]: This parameter will vary with the quality of the TDC and system DPLL references. The typical value shown assumes an ideal reference is used as input to the TDC and system DPLL.
[^g]: Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
[^h]: This parameter is defined in accordance with JEDEC Standard 65.
[^i]: Measured at the differential cross points.
[^j]: Measured at V\_DDO\_Qx / 2.
[^k]: Output-output skew numbers valid for all multiplexer settings for these outputs.
[^l]: This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.
[^m]: Measured from the differential cross point of the input to the differential cross point of the associated output after device is locked and input is stable. Measured using integer-related input and output frequencies.
[^n]: Rise and fall times on differential outputs are independent of the power supply voltage on the output.
[^o]: Measured with outputs terminated with 50Ω to GND.
[^p]: For information on the signals referenced by this abbreviation, see Table 24.
[^q]: Refers to the differential voltage swing setting programmed into device registers for each output.
[^r]: Measured with outputs terminated with 50Ω to V\_DDO\_Qx / 2.
[^s]: Refers to the LVCMOS output drive strength (termination) setting programmed into device registers for each output.
Figure 34. Input-Output Delay

CLKx

<table>
<thead>
<tr>
<th>a = Fixed delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>b = Delay variation</td>
</tr>
</tbody>
</table>

Qy

- Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.
- 100mV peak-peak sine-wave noise signal injected on indicated power supply pin(s).
- Noise spur amplitude measured relative to 156.25MHz carrier.
- Measured from the rising edge of nMR after all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.
- At power-up, the nMR signal must be asserted for at least this period of time.
- Start-up time will depend on the actual configuration used. For more information on estimating start-up time, please contact IDT technical support.
Clock Phase Noise Characteristics

Figure 35. 156.25MHz Output Phase Noise

Phase noise 10.00dB/Ref 0.000dBc/Hz

---

*Figure 35. 156.25MHz Output Phase Noise Diagram*

- **Phase Noise**
  - 10 Hz: -91.5487 dBc/Hz
  - 100 Hz: -101.3826 dBc/Hz
  - 1 kHz: -111.5996 dBc/Hz
  - 10 kHz: -132.5831 dBc/Hz
  - 100 kHz: -139.1027 dBc/Hz
  - 1 MHz: -132.2977 dBc/Hz
  - 10 MHz: -137.2446 dBc/Hz
  - 30 MHz: -151.0052 dBc/Hz
  - >50 MHz: -158.8891 dBc/Hz

---

**Analysis Information**
- **Center**: 10.005 MHz
- **Span**: 19.98 MHz
- **RMS Noise**: 144.487 μrad
- **RMS Jitter**: 8.27049 ns
- **Residual FM**: 1.38996 kHz

---

©2019 Integrated Device Technology, Inc

June 17, 2019
Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLKx / nCLKx Input
For applications that do not require the use of the reference clock input, both CLK and nCLK should be left floating. If the CLK/nCLK input is connected but not used by the device, it is recommended that CLK and nCLK not be driven with active signals.

LVCMOS Control Pins
LVCMOS control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVCMOS Outputs
Any LVCMOS output can be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to tri-stated to avoid any noise being generated.

Differential Outputs
All unused differential outputs can be left floating. IDT recommends that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Power Connections
The power connections of the 8A34044 can be grouped as shown if all members of the groups are using the same voltage level:

- V_DD_DIG, V_DD_CLK, V_DD_CLKB
- V-DDA_PDCP_XTAL
- V-DDA_FB
- V-DDA_BG_LC, V-DD_GPIO_FOD, V-DDA_DIA_FOD_A, V-DDA_DIA_FOD_B (combining these is a possible source of coupling between frequency domains; should remain separate unless all outputs are in the same frequency domain)
- V_DDO_Qn (can share supplies if output frequencies are the same, otherwise keep separated to avoid spur coupling)
  - If all outputs Qn/nQn associated with any particular V_DDO_Qn pin are not used, the power pin can be left floating

Clock Input Interface
The 8A34044 accepts both single-ended and differential inputs. For information on input terminations, see Quick Guide - Output Terminations (AN-953) located on the 8A34044 product page.

If you have additional questions on input types not covered in the application discussion, or if you require information about register programming sequences for changing the differential inputs to accept LVCMOS inputs levels, see Termination - AC Coupling Clock Receivers (AN-844) or contact IDT technical support.
Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 1.8V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 36. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. For limits on the frequency that can be used, see Table 36.

Figure 36. 1.8V LVCMOS Driver to XTAL Input Interface

![Figure 36](image)

Figure 37 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

Figure 37. LVCMOS Driver to XTAL Input Interface

![Figure 37](image)

Figure 38 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

![Figure 38](image)
Wiring the Differential Input to Accept Single-Ended Levels
For information, see the Differential Input to Accept Single-ended Levels Application Note (AN-836).

Differential Output Termination
For all types of differential protocols, the same termination scheme is recommended (see Figure 39). This scheme is the same as normally used for an LVDS output type: the recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

For alternate termination schemes, see “LVDS Termination” in Quick Guide - Output Terminations (AN-953) located on the 8A34044 product page, or contact IDT for support.

Crystal Recommendation
For the latest vendor / frequency recommendations, please contact IDT.
**External I²C Serial EEPROM Recommendation**

An external I²C EEPROM can be used to store configuration data and/or to contain device update data. An EEPROM with 8Kbit capacity is sufficient to store a full configuration. However, the recommendation is to use an EEPROM with a 1Mbit capacity in order to support future device updates. IDT has validated and recommends the use of the Microchip 24FC1025 or OnSemi CAT24M01 1Mbit EEPROM.

**Schematic and Layout Information**

The 8A34044 requires external load capacitors to ensure the crystal will resonate at the proper frequency. For recommended values for external tuning capacitors, see Table 39.

**Table 39. Recommended Tuning Capacitors for Crystal Input**

<table>
<thead>
<tr>
<th>Crystal Nominal $C_L$ Value (pF)</th>
<th>Recommended Tuning Capacitor Value (pF) $^[a]$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OSCI Capacitor (pF)</td>
</tr>
<tr>
<td>8</td>
<td>2.7</td>
</tr>
<tr>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td>12</td>
<td>27</td>
</tr>
<tr>
<td>18$^[b]$</td>
<td>27</td>
</tr>
</tbody>
</table>

$^[a]$ Recommendations are based on 4pF stray capacitance on each leg of the crystal. Adjust according to the PCB capacitance.

$^[b]$ This will tune the crystal to a CL of 12pF, which is fine when channels are running in jitter attenuator mode or referenced to an XO. It will present a positive ppm offset for channels running exclusively in Synthesizer mode and referenced only to the crystal.

**Power Considerations**

For power and current consumption calculations, refer to IDT’s Timing Commander tool.
QFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 40. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

Figure 40. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing Not to Scale)

Thermal Characteristics

Table 40. Thermal Characteristics for 72-QFN Package

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} )</td>
<td>Theta ( J_A ), Junction to Ambient Air Thermal Coefficient[^a][^b]</td>
<td>0 m/s air flow</td>
<td>13.71 °C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 m/s air flow</td>
<td>10.67 °C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 m/s air flow</td>
<td>9.46 °C/W</td>
</tr>
<tr>
<td>( \theta_{JB} )</td>
<td>Theta ( J_B ), Junction to Board Thermal Coefficient[^a]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \theta_{JC} )</td>
<td>Theta ( J_C ), Junction to Device Case Thermal Coefficient[^a]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>Moisture Sensitivity Rating (Per J-STD-020)</td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

[^a]: Multi-Layer PCB with 2 ground and 2 voltage planes.
[^b]: Assumes ePAD is connected to a ground plane using a grid of 9x9 thermal vias.
Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nlnlg72-package-outline-100x100-mm-body-epad-77-mm-sq-050-mm-pitch-qfn-sawn

Marking Diagram

- Lines 1 and 2 indicate the part number.
  - “-000” is the dash code, which may differ for a device with a different ordering code (for the exact number, see the specific datasheet addendum).
- Line 3 indicates the following:
  - “#” denotes stepping.
  - “YY” is the last two digits of the year; “WW” is the work week number when the part was assembled.
  - “$” denotes the mark code.

Ordering Information

<table>
<thead>
<tr>
<th>Orderable Part Number</th>
<th>Package</th>
<th>MSL Rating</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8A34044E-dddNLG[a]</td>
<td>10 × 10 × 0.9 mm, 72-QFN</td>
<td>3</td>
<td>Tray</td>
<td>-40° to +85°C</td>
</tr>
<tr>
<td>8A34044E-dddNLG8</td>
<td>10 × 10 × 0.9 mm, 72-QFN</td>
<td>3</td>
<td>Tape and Reel, Pin 1 Orientation: EIA-481-C</td>
<td>-40° to +85°C</td>
</tr>
<tr>
<td>8A34044E-dddNLG#</td>
<td>10 × 10 × 0.9 mm, 72-QFN</td>
<td>3</td>
<td>Tape and Reel, Pin 1 Orientation: EIA-481-D</td>
<td>-40° to +85°C</td>
</tr>
</tbody>
</table>

[a] Replace “ddd” with the desired pre-programmed configuration code provided by IDT in response to a custom configuration request or use “000” for unprogrammed parts.
Table 41. Pin 1 Orientation in Tape and Reel Packaging

<table>
<thead>
<tr>
<th>Part Number Suffix</th>
<th>Pin 1 Orientation</th>
<th>Illustration</th>
</tr>
</thead>
<tbody>
<tr>
<td>NLG8</td>
<td>Quadrant 1 (EIA-481-C)</td>
<td>![ Illustration of NLG8 orientation ]</td>
</tr>
<tr>
<td>NLG#</td>
<td>Quadrant 2 (EIA-481-D)</td>
<td>![ Illustration of NLG# orientation ]</td>
</tr>
</tbody>
</table>

Product Identification

Table 42: Product Identification

<table>
<thead>
<tr>
<th>Part Number</th>
<th>JTAG ID</th>
<th>Product ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>8A34044</td>
<td>0x064E</td>
<td>0x4044</td>
</tr>
</tbody>
</table>
## Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1PPS</td>
<td>One Pulse Per Second.</td>
</tr>
<tr>
<td>eCLK</td>
<td>Embedded clock.</td>
</tr>
<tr>
<td>eCSR</td>
<td>Embedded CSR access.</td>
</tr>
<tr>
<td>eDATA</td>
<td>Embedded DATA channel.</td>
</tr>
<tr>
<td>ePP2S</td>
<td>Embedded PP2S.</td>
</tr>
<tr>
<td>ePPS</td>
<td>Embedded PPS. This describes a means to embed 1PPS on a clock using PWM.</td>
</tr>
<tr>
<td>EPPS</td>
<td>Even PPS.</td>
</tr>
<tr>
<td>ESEC</td>
<td>Even Second pulse. PP2S and ESEC are used interchangeably or sometimes combined as PP2S/ESEC.</td>
</tr>
<tr>
<td>eSYNC</td>
<td>Embedded SYNC pulse.</td>
</tr>
<tr>
<td>PP2S</td>
<td>Pulse Per 2 Second. This represents a 0.5Hz pulse.</td>
</tr>
<tr>
<td>PPS</td>
<td>Pulse Per Second.</td>
</tr>
<tr>
<td>REF-SYNC</td>
<td>Combination of high-speed clock (i.e., &gt; 1MHz) and low-speed frame/sync pulse (i.e., &lt; 8kHz).</td>
</tr>
<tr>
<td>SCSR</td>
<td>Standard Control / Status Register</td>
</tr>
<tr>
<td>ZDB</td>
<td>Zero Delay Buffer</td>
</tr>
<tr>
<td>ZDPLL</td>
<td>Zero Delay Phase Locked Loop</td>
</tr>
</tbody>
</table>
Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
</table>
| June 17, 2019 | ▪ Adjusted descriptions and expanded DPLL loop bandwidth limits  
▪ Adjusted OSCI / OSCO input capacitance values in Table 2  
▪ Updated Table 7 to remove activity limits that were only available in obsolete Device Update revisions  
▪ Added a description of External Feedback  
▪ Fixed Increment / Decrement Registers and Pins to remove reference to a single 16-bit register that is not implemented  
▪ Fixed inconsistency between DC Specifications table for CMOS mode output clocks and output buffer descriptive text with respect to 1.2V and 1.5V CMOS operation  
▪ Removed temperature sensor due to inconsistent operation  
▪ Added Power Supply Noise Rejection rows to AC characteristics in Table 38  
▪ Table 38 Updated Tuning capacitor recommendations in Table 39 to limit crystal drive strength  
▪ Added application information for 1.8V LVCMOS to over-drive the crystal input (see Overdriving the XTAL Interface)  
▪ Updated marking diagram and ordering information to Revision E |
| February 6, 2019 | ▪ Revision C device (which has Device Update v4.7 embedded) has the following functional differences:  
▪ Reset sequence sped-up, altering the way external EEPROMs are searched. Changes made to Reset Sequence and Use of External I2C EEPROM sections  
▪ Corrected the clock and GPIO mapping in Table 5  
▪ Changed Activity Monitor limits (this is with Device Update v4.7 regardless of hardware revision) in Table 7  
▪ Clarified the following areas of the datasheet: Steerable Fractional Output Divider (FOD), JTAG Interface, and External I2C Serial EEPROM Recommendation  
▪ Changed Marking Diagram and Ordering Information to show C revision |
| November 19, 2018 | Initial release. |
72-VFQFPN, Package Outline Drawing

10.0 x 10.0 x 0.90 mm Body, Epad 7.70 x 7.70 mm 0.50mm Pitch
NLG72P4, PSC-4208-04, Rev 02, Page 1

INDEX AREA

TOP VIEW

SIDE VIEW

BOTTOM VIEW

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN IDENTIFIER)
RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.