General Description

The IDT8N3SV75 is a LVPECL Frequency-Programmable VCXO with very flexible frequency and pull-range programming capabilities. The device uses IDT’s fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory-programmed to any frequency in the range of 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz to the very high degree of frequency precision of 218Hz or better. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Frequency programming resolution is 218Hz and better
- Factory-programmable VCXO pull range and control voltage polarity
- Absolute pull range (APR) programmable from typical ±4.5 to ±754.5ppm
- One 2.5V/3.3V LVPECL clock output
- Output enable control input, LVCMOS/LVTTL compatible
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.5ps (typical),
- 2.5V or 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package

Block Diagram

Pin Assignment

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VC</td>
<td>Input</td>
</tr>
<tr>
<td>OE</td>
<td>Output</td>
</tr>
<tr>
<td>VEE</td>
<td>Input</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply</td>
</tr>
</tbody>
</table>

Configuration Register (ROM) (Frequency, Pull-range, Polarity)
Pin Description and Characteristic Tables

Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VC</td>
<td>Input</td>
<td>VCXO Control Voltage input.</td>
</tr>
<tr>
<td>2</td>
<td>OE</td>
<td>Input</td>
<td>Pullup</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output enable pin. See Table 3A for function. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>3</td>
<td>VEE</td>
<td>Power</td>
<td>Negative power supply.</td>
</tr>
<tr>
<td>4, 5</td>
<td>Q, nQ</td>
<td>Output</td>
<td>Differential clock output. LVPECL interface levels.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Power</td>
<td>Positive power supply.</td>
</tr>
</tbody>
</table>

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td>OE</td>
<td>5.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VC</td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>50</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Function Tables

Table 3A. OE Configuration

<table>
<thead>
<tr>
<th>Input</th>
<th>Output Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE</td>
<td>Outputs Q, nQ are in high-impedance state.</td>
</tr>
<tr>
<td>0</td>
<td>Outputs are enabled.</td>
</tr>
<tr>
<td>1 (default)</td>
<td></td>
</tr>
</tbody>
</table>

Table 3B. Output Frequency Range

<table>
<thead>
<tr>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>15.476MHz to 866.67MHz</td>
</tr>
<tr>
<td>975MHz to 1,300MHz</td>
</tr>
</tbody>
</table>

NOTE: Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.
**Principles of Operation**

The block diagram consists of the internal 3rd overtone crystal and oscillator which provide the reference clock \( f_{XTAL} \) of 114.285MHz. The PLL includes the FemtoClock® NG VCO along with the Pre-divider \( P \), the feedback divider \( M \) and the post divider \( N \). The \( P, M, \) and \( N \) dividers determine the output frequency based on the \( f_{XTAL} \) reference. The feedback divider is fractional supporting a huge number of output frequencies. Internal registers are used to hold up the factory pre-set configuration setting. The \( P, M, \) and \( N \) frequency configurations support an output frequency range 15.476MHz to 866.67MHz and 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator. The output frequency is determined by the 2-bit pre-divider \( P \), the feedback divider \( M \) and the 7-bit post divider \( N \). The feedback divider \( M \) consists of both a 7-bit integer portion \( MINT \) and an 18-bit fractional portion \( MFRAC \) and provides the means for high-resolution frequency generation. The output frequency \( f_{OUT} \) is calculated by:

\[
f_{OUT} = f_{XTAL} \cdot \frac{P \cdot MINT + MFRAC + 0.5}{2^{18}}
\]

**Frequency Configuration**

An order code is assigned to each frequency configuration and the VCXO pull-range programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information Section in this document. For available order codes, see the FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information document.

For more information on programming capabilities of the device for custom frequency and pull-range configurations, see the FemtoClock NG Ceramic 5x7 Module Programming Guide.
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the **DC Characteristics** or **AC Characteristics** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{CC}$</td>
<td>3.63V</td>
</tr>
<tr>
<td>Inputs, $V_i$</td>
<td>-0.5V to $V_{CC} + 0.5V$</td>
</tr>
<tr>
<td>Outputs, $I_O$ (LVPECL)</td>
<td>50mA</td>
</tr>
<tr>
<td>Continuous Current</td>
<td>100mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td></td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>49.4°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%, V_{EE} = 0V, T_A = -40°C to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td></td>
<td>130</td>
<td>160</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Table 4B. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%, V_{EE} = 0V, T_A = -40°C to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td></td>
<td>120</td>
<td>155</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Table 4C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%, V_{EE} = 0V, T_A = -40°C to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{CC} - 1.4$</td>
<td>$V_{CC} - 0.8$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{CC} - 2.0$</td>
<td>$V_{CC} - 1.7$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.6</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

**Table 4D. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%, V_{EE} = 0V, T_A = -40°C to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{CC} - 1.4$</td>
<td>$V_{CC} - 0.8$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{CC} - 2.0$</td>
<td>$V_{CC} - 1.5$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.4</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$. 
Table 4E. LVCMOS/LVTTL DC Characteristic, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{CC} = 3.3V$</td>
<td>2</td>
<td>$V_{CC} + 0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.5V$</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{CC} = V_{IN} = 3.465V$</td>
<td>-0.3</td>
<td>0.8</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = V_{IN} = 2.5V$</td>
<td>-0.3</td>
<td>0.7</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>OE, $V_{CC} = V_{IN} = 3.465V$ or $2.625V$</td>
<td>5</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>OE, $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$</td>
<td>-150</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
AC Electrical Characteristics

Table 5A. AC Characteristics, \( V_{CC} = 3.3V \pm 5\% \) or \( 2.5V \pm 5\% \), \( V_{EE} = 0V \), \( T_A = -40^\circ C \) to \( 85^\circ C \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{OUT} )</td>
<td>Output Frequency Q, nQ</td>
<td></td>
<td>15.476</td>
<td>866.67</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>975</td>
<td>1,300</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_I )</td>
<td>Initial Accuracy</td>
<td>Measured @ 25°C, ( V_C = V_{CC}/2 )</td>
<td>±10</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_S )</td>
<td>Temperature Stability</td>
<td>Option code = A or B</td>
<td>±100</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Option code = E or F</td>
<td>±50</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Option code = K or L</td>
<td>±20</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_A )</td>
<td>Aging</td>
<td>Frequency drift over 10 year life</td>
<td>±3</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Frequency drift over 15 year life</td>
<td>±5</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_T )</td>
<td>Total Stability</td>
<td>Option code A, B (10 year life)</td>
<td>±113</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Option code E, F (10 year life)</td>
<td>±63</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Option code K, L (10 year life)</td>
<td>±33</td>
<td>ppm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( j_{it(cc)} )</td>
<td>Cycle-to-Cycle Jitter; NOTE 1</td>
<td></td>
<td>6</td>
<td>12</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( j_{it(per)} )</td>
<td>Period Jitter; NOTE 1</td>
<td></td>
<td>1.8</td>
<td>2.8</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( j_{it(\Phi)} )</td>
<td>RMS Phase Jitter (Random); NOTE 2, 3</td>
<td>156.25MHz, Integration Range: 12kHz - 20MHz</td>
<td>0.5</td>
<td>0.66</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( j_{it(\Phi)} )</td>
<td>RMS Phase Jitter (Random); NOTE 2, 3</td>
<td>156.25MHz, Integration Range: 1kHz - 40MHz</td>
<td>0.9</td>
<td>1.3</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( j_{it(\Phi)} )</td>
<td>RMS Phase Jitter (Random); NOTE 2,3,4</td>
<td>( f_{XTAL} = 114.285mhz )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 500MHz &lt; f_{OUT} \leq 1300MHz )</td>
<td>0.44</td>
<td>0.77</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 100MHz &lt; f_{OUT} \leq 500MHz )</td>
<td>0.52</td>
<td>0.90</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 15MHz \leq f_{OUT} \leq 100MHz )</td>
<td>0.74</td>
<td>1.2</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(100) )</td>
<td>Single-side band phase noise, 100Hz from Carrier</td>
<td>156.25MHz</td>
<td>-69</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(1k) )</td>
<td>Single-side band phase noise, 1kHz from Carrier</td>
<td>156.25MHz</td>
<td>-98</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(10k) )</td>
<td>Single-side band phase noise, 10kHz from Carrier</td>
<td>156.25MHz</td>
<td>-123</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(100k) )</td>
<td>Single-side band phase noise, 100kHz from Carrier</td>
<td>156.25MHz</td>
<td>-128</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(1M) )</td>
<td>Single-side band phase noise, 1MHz from Carrier</td>
<td>156.25MHz</td>
<td>-140</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_N(10M) )</td>
<td>Single-side band phase noise, 10MHz from Carrier</td>
<td>156.25MHz</td>
<td>-145</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSNR</td>
<td>Power Supply Noise Rejection</td>
<td>50mV Sinusoidal Noise 1kHz - 50MHz</td>
<td>-71.2</td>
<td>dBC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_R / t_F )</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>80</td>
<td>500</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( \text{odc} )</td>
<td>Output Duty Cycle</td>
<td></td>
<td>45</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( t_{STARTUP} )</td>
<td>Device startup time after power up</td>
<td></td>
<td>10</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.

NOTE 1: This parameter is defined in accordance with JEDEC standard 65.

NOTE 2: Refer to the phase noise plot.

NOTE 3: Please see the FemtoClock NG Ceramic 5x7 Modules Programming guide for more information on PLL feedback modes and the optimum configuration for phase noise.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>KV</td>
<td>Oscillator Gain, NOTE 1, 2, 3</td>
<td>V_CC = 3.3V</td>
<td>7.57</td>
<td>477.27</td>
<td>ppm/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillator Gain, NOTE 1, 2, 3</td>
<td>V_CC = 2.5V</td>
<td>10</td>
<td>630</td>
<td>ppm/V</td>
<td></td>
</tr>
<tr>
<td>LVC</td>
<td>Control Voltage Linearity; NOTE 4</td>
<td>BSL Variation</td>
<td>-1</td>
<td>±0.1</td>
<td>+1</td>
<td>%</td>
</tr>
<tr>
<td>BW</td>
<td>Modulation Bandwidth</td>
<td></td>
<td>100</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZVC</td>
<td>VC Input Impedance</td>
<td></td>
<td>500</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCNOM</td>
<td>Nominal Control Voltage</td>
<td>V_CC/2</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VC</td>
<td>Control Voltage Tuning Range; NOTE 4</td>
<td></td>
<td>0</td>
<td>V_CC</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: V_C = 10% to 90% of V_CC.

NOTE 2: Nominal oscillator gain: Pull range divided by the control voltage tuning range of 3.3V. E.g. for ADC_GAIN [6:0] = 000001 the pull range is ±12.5ppm, resulting in an oscillator gain of 25ppm ÷ 3.3V = 7.57ppm/V.

NOTE 3: For best phase noise performance, use the lowest KV that meets the requirements of the application.

NOTE 4: BSL = Best Straight Line Fit: Variation of the output frequency vs. control voltage V_C, in percent. V_C ranges from 10% to 90% V_CC.
Typical Phase Noise at 156.25MHz (12kHz - 20MHz)

Carrier 156.25MHz +1.2dBc/Hz
X: Start 12 kHz
Stop 20 MHz
Center 10.005 MHz
Span 19.998 MHz

Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Integ Noise: -68.3665 dBc/Hz / 19.998 MHz
RMS Noise: 527.481 μrad
RMS Jitter: 337.272 μs
Residual FM: 3.98899 kHz
Parameter Measurement Information

2.5 LVPECL Output Load AC Test Circuit

3.3V LVPECL Output Load AC Test Circuit

RMS Phase Jitter

Output Rise/Fall Time

Output Duty Cycle /Pulse Width/Period

Cycle -to-Cycle Jitter
Parameter Measurement Information, continued

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Reference Point</th>
<th>Histogram</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean Period</td>
<td>(First edge after trigger)</td>
<td>Trigger Edge</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Voltage Output High</td>
<td>VREF</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Voltage Output Low</td>
<td>VOL</td>
<td></td>
</tr>
</tbody>
</table>

Period Jitter

Applications Information

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 1A and 1B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 1A. 3.3V LVPECL Output Termination

Figure 1B. 3.3V LVPECL Output Termination
**Termination for 2.5V LVPECL Outputs**

*Figure 2A* and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2\, \text{V}$. For $V_{CC} = 2.5\, \text{V}$, the $V_{CC} - 2\, \text{V}$ is very close to ground level. The R3 in *Figure 2B* can be eliminated and the termination is shown in *Figure 2C*.

---

**Figure 2A. 2.5V LVPECL Driver Termination Example**

**Figure 2B. 2.5V LVPECL Driver Termination Example**

**Figure 2C. 2.5V LVPECL Driver Termination Example**
Schematic Layout

Figure 3 shows an example of IDT8N3SV75 application schematic. In this example, the device is operated at $V_{CC} = 3.3\,\text{V}$. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

![Figure 3. IDT8N3SV75 Application Schematic](image)
Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N3SV75. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N3SV75 is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for \( V_{CC} = 3.3V + 5\% = 3.465V \), which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 160mA = 554.40mW
- Power (outputs)_{MAX} = 30mW/Loaded Output pair

Total Power_{MAX} (3.3V, with all outputs switching) = 554.40mW + 30mW = 584.40mW

2. Junction Temperature.

Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, \( T_j \), to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for \( T_j \) is as follows: \( T_j = \theta_{JA} * P_{d\_total} + T_A \)

\( T_j = \) Junction Temperature

\( \theta_{JA} = \) Junction-to-Ambient Thermal Resistance

\( P_{d\_total} = \) Total Device Power Dissipation (example calculation is in section 1 above)

\( T_A = \) Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{JA} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, \( T_j \) for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.584W * 49.4°C/W = 113.8°C. This is below the limit of 125°C.

This calculation is only an example. \( T_j \) will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance \( \theta_{JA} \) for 6 Lead Ceramic VFQFN, Forced Convection

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>49.4°C/W</td>
<td>44.2°C/W</td>
<td>42.1°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.
The purpose of this section is to calculate the power dissipation for the LVPECL output pair.
LVPECL output driver circuit and termination are shown in Figure 4.

![Diagram of LVPECL Driver Circuit and Termination](image)

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH, MAX} = V_{CC, MAX} - 0.9V$
  $\left(\frac{V_{CC, MAX} - V_{OH, MAX}}{50\Omega}\right) * 0.9V = 19.8mW$

- For logic low, $V_{OUT} = V_{OL, MAX} = V_{CC, MAX} - 1.7V$
  $\left(\frac{V_{CC, MAX} - V_{OL, MAX}}{50\Omega}\right) * 1.7V = 10.2mW$

$P_{d, H}$ is power dissipation when the output drives high.

$P_{d, L}$ is the power dissipation when the output drives low.

$$P_{d, H} = \left(\frac{V_{OH, MAX} - (V_{CC, MAX} - 2V)/RL}{RL}\right) * (V_{CC, MAX} - V_{OH, MAX}) = \left[\frac{(2V - (V_{CC, MAX} - V_{OH, MAX}))}{50\Omega}\right] * 0.9V = 19.8mW$$

$$P_{d, L} = \left(\frac{V_{OL, MAX} - (V_{CC, MAX} - 2V)/RL}{RL}\right) * (V_{CC, MAX} - V_{OL, MAX}) = \left[\frac{(2V - (V_{CC, MAX} - V_{OL, MAX}))}{50\Omega}\right] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $P_{d, H} + P_{d, L} = 30mW$
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>$\theta_{JA}$ vs. Air Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>49.4°C/W</td>
</tr>
<tr>
<td>1</td>
<td>44.2°C/W</td>
</tr>
<tr>
<td>2</td>
<td>42.1°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for IDT8N3SV75 is: 47,414
Package Outline and Package Dimensions

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DIMENSION IN MM</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>MIN.</td>
</tr>
<tr>
<td></td>
<td>4.85</td>
</tr>
<tr>
<td>B</td>
<td>6.85</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
</tr>
<tr>
<td>D₁</td>
<td>2.41</td>
</tr>
<tr>
<td>D₂</td>
<td>4.95</td>
</tr>
<tr>
<td>E</td>
<td>2.47</td>
</tr>
<tr>
<td>F</td>
<td>0.47</td>
</tr>
<tr>
<td>G</td>
<td>1.27</td>
</tr>
<tr>
<td>H</td>
<td>-</td>
</tr>
<tr>
<td>J</td>
<td>-</td>
</tr>
</tbody>
</table>
Ordering Information for FemtoClock® NG Ceramic-Packaged XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. Table 8 specifies the available order codes, including the device options. Example part number: the order code 8N3SV75FC-0001CDI specifies a programmable VCXO with a voltage supply of 2.5V, ±50 ppm crystal frequency accuracy, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100 MHz and the VCXO pull range of ±100 ppm.

Other default frequencies and order codes are available from IDT on request.

Table 8. Order Codes

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Shipping Package</th>
<th>Ambient Temperature Range</th>
<th>Package Code</th>
<th>Default-Frequency and VCXO Pull Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>8N X X XXX X - dddd XX X X</td>
<td>8: Tape &amp; Reel</td>
<td>“I”: Industrial: (TA = -40°C to 85°C)</td>
<td>CD: Lead-Free, 6/10-lead ceramic 5mm x 7mm x 1.55mm</td>
<td>See document FemtoClock NG Ceramic-Packaged XO and VCXO Ordering Product Information.</td>
</tr>
<tr>
<td></td>
<td>(no letter): Tray</td>
<td>(no letter) : (TA = 0°C to 70°C)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Part Number

<table>
<thead>
<tr>
<th>Function</th>
<th>#pins</th>
<th>OE fct. at pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>XO</td>
<td>10 OE@2</td>
</tr>
<tr>
<td>003</td>
<td>XO</td>
<td>10 OE@1</td>
</tr>
<tr>
<td>V01</td>
<td>VCXO</td>
<td>10 OE@2</td>
</tr>
<tr>
<td>V03</td>
<td>VCXO</td>
<td>10 OE@1</td>
</tr>
<tr>
<td>V75</td>
<td>VCXO</td>
<td>6 OE@2</td>
</tr>
<tr>
<td>V76</td>
<td>VCXO</td>
<td>6 nOE@2</td>
</tr>
<tr>
<td>V85</td>
<td>VCXO</td>
<td>6 —</td>
</tr>
<tr>
<td>085</td>
<td>XO</td>
<td>6 OE@1</td>
</tr>
<tr>
<td>270</td>
<td>XO</td>
<td>6 OE@1</td>
</tr>
<tr>
<td>271</td>
<td>XO</td>
<td>6 OE@2</td>
</tr>
<tr>
<td>272</td>
<td>XO</td>
<td>6 nOE@2</td>
</tr>
<tr>
<td>273</td>
<td>XO</td>
<td>6 nOE@1</td>
</tr>
</tbody>
</table>

Die Revision: C

Option Code (Supply Voltage and Frequency-Stability)

<table>
<thead>
<tr>
<th>Function</th>
<th>Supply Voltage</th>
<th>Frequency Stabilty</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>VCC = 3.3V±5%</td>
<td>±100 ppm</td>
</tr>
<tr>
<td>B</td>
<td>VCC = 2.5V±5%</td>
<td>±100 ppm</td>
</tr>
<tr>
<td>E</td>
<td>VCC = 3.3V±5%</td>
<td>±50 ppm</td>
</tr>
<tr>
<td>F</td>
<td>VCC = 2.5V±5%</td>
<td>±50 ppm</td>
</tr>
<tr>
<td>K</td>
<td>VCC = 3.3V±5%</td>
<td>±20 ppm</td>
</tr>
<tr>
<td>L</td>
<td>VCC = 2.5V±5%</td>
<td>±20 ppm</td>
</tr>
</tbody>
</table>

NOTE: For order information, see the FemtoClock NG Ceramic-Packaged XO and VCXO Ordering Product Information document.
### Table 9. Device Marking

<table>
<thead>
<tr>
<th>Marking</th>
<th>Industrial Temperature Range ($T_A = -40^\circ C$ to $85^\circ C$)</th>
<th>Commercial Temperature Range ($T_A = 0^\circ C$ to $70^\circ C$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDT8N3SV75yCd</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dddCDI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$y =$ Option Code, $ddd$=Default-Frequency and VCXO Pull Range</td>
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<td></td>
</tr>
</tbody>
</table>
## Revision History Sheet

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>5A</td>
<td>6</td>
<td>RMS Phase Jitter, Test Conditions, corrected typos for 500MHz and 100MHz; “≤” to “&lt;”</td>
<td>11/19/2013</td>
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</tbody>
</table>