1:4 LVDS Fanout Buffer with 2-Input Multiplexer for 1PPS Applications

8V34S204

DATA SHEET

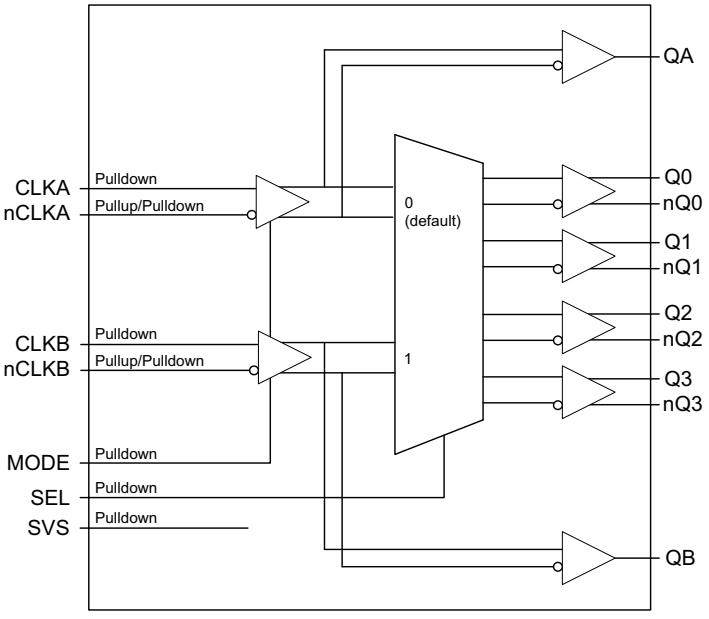
General Description

The 8V34S204 is a differential 1:4 LVDS fanout buffer with a 2:1 input multiplexer. The device accepts DC to 250MHz clock and data signals and is designed for 1Hz clock /1PPS, 2kHz and 8kHz signal distribution. Controlled by the input mode selection pin, the differential input stages accept both rectangular or sinusoidal signals. The 8V34S204 also provides level translated LVCMOS/LVTTL outputs which are copies of the individual differential inputs CLKA and CLKB. The propagation delay of the device is very low, providing an ideal solution for clock distribution circuits with tight phase alignment requirements. The multiplexer select pin (SEL) allows to select one out of two input signals, which is copied to the four differential outputs.

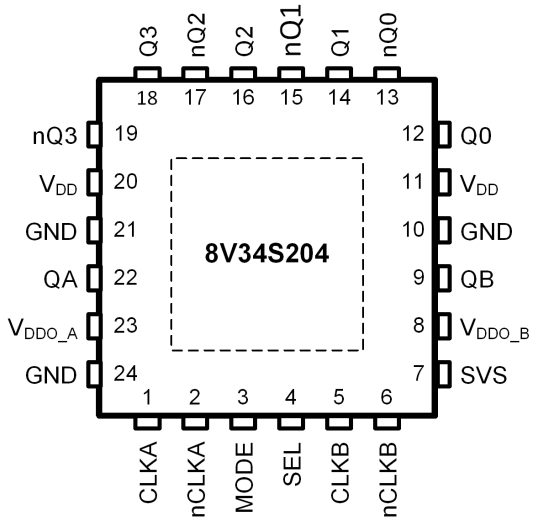
Features

- Designed for 1PPS, 2kHz, 8kHz and 10MHz GPS clock signal distribution
- High speed 1:4 LVDS fanout buffer
- Four differential LVDS output pairs
- 2:1 input multiplexer
- Two selectable differential inputs accept LVDS and LVPECL signals
- Accepts rectangular and sinusoidal input signals
- Two input monitoring outputs (LVCMOS)
- Max Output frequency: 250MHz
- Additive phase jitter, RMS;
  12kHz to 20MHz: = 65fs at 156.25MHz (typical)
- Part-to-part skew: 200ps (maximum)
- Propagation delay (differential outputs): 350ps (typical)
- Full 2.5V and 3.3V voltage supply
- -40°C to 85°C ambient operating temperature
- Lead-free 24-lead VFQFN (RoHS 6/6) packaging

Block Diagram



Pin Assignment



24-Lead VFQFN
4mm x 4mm x 0.9mm
NL Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	CLKA	Input	Pulldown	Non-inverting differential clock input.
2	nCLKA	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
3	MODE	Input	Pulldown	Input mode pin. See Table 3B. LVCMOS/LVTTL interface levels.
4	SEL	Input	Pulldown	Input selection pin. See Table 3A. LVCMOS/LVTTL interface levels.
5	CLKB	Input	Pulldown	Non-inverting differential clock input.
6	nCLKB	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
7	SVS	Input	Pulldown	Supply Voltage Select. See Table 3C. LVCMOS/LVTTL interface levels.
8	V_{DDO_B}	Power		Output supply pin for the QB output.
9	QB	Output		Single-ended output clock. LVCMOS/LVTTL interface levels.
10	GND	Power		Power supply ground.
11	V_{DD}	Power		Power supply pins for the device core.
12	Q0	Output		Differential output pair. LVDS interface levels.
13	nQ0	Output		Differential output pair. LVDS interface levels.
14	Q1	Output		Differential output pair. LVDS interface levels.
15	nQ1	Output		Differential output pair. LVDS interface levels.
16	Q2	Output		Differential output pair. LVDS interface levels.
17	nQ2	Output		Differential output pair. LVDS interface levels.
18	Q3	Output		Differential output pair. LVDS interface levels.
19	nQ3	Output		Differential output pair. LVDS interface levels.
20	V_{DD}	Power		Power supply pins for the device core.
21	GND	Power		Power supply ground.
22	QA	Output		Single-ended output clock. LVCMOS/LVTTL interface levels.
23	V_{DDO_A}	Power		Output supply pin for the QA output.
24	GND	Power		Power supply ground.

NOTE: 1. *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		MODE, SEL, SVS		2		pF
$R_{PULLDOWN}$	Pulldown Resistor				50		kΩ
R_{PULLUP}	Pullup Resistor				50		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	QA, QB	V_{DD}, V_{DDO_A}, V_{DDO_B} = 3.465V		6		pF
		QA, QB	V_{DD}, V_{DDO_A}, V_{DDO_B} = 2.625V		6		pF
R_{OUT}	Output Impedance	QA, QB	V_{DDO_A}, V_{DDO_B} = 3.3V ± 5%		24		Ω
		QA, QB	V_{DDO_A}, V_{DDO_B} = 2.5V ± 5%		28		Ω

Function Tables

Table 3A. Input Selection Function Table

Input	Outputs		
SEL	**Q0-Q3**	**QA**	**QB**
0 (default)	CLKA	CLKA	CLKB
1	CLKB	CLKA	CLKB

Table 3B. Input Mode Function Table[1]

Input	Operation
MODE	**CLKA, CLKB**
0 (default)	Inputs accept rectangular signals
1	Inputs accept sinusoidal signals

NOTE: 1. Use a rectangular wave input for inputs with edge rate greater than 1V/ns.

Table 3C. Supply Voltage Select Function Table

Input	Operation
SVS	**Supply Voltage**
0 (default)	Set to logic 0 when $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 2.5V
1	Set to logic 1 when $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current Outputs, I_O (LVCMOS)	 10 mA 15 mA -0.5V to V_{DD} + 0.5V
Maximum Junction Temperature, $T_{J, MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model, NOTE 1	2000V
ESD - Charged Device Model, NOTE 1	500V

NOTE 1. According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			93	108	mA
I_{DDO_A} + I_{DDO_B}	Output Supply Current	Outputs Unterminated		6	8	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$ = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			90	102	mA
I_{DDO_A} + I_{DDO_B}	Output Supply Current	Outputs Unterminated		5	8	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$, 3.3V ±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	MODE, SEL, SVS	$V_{DD} = V_{IN}$ = 3.465V			150	µA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$, 3.3V ±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IL}	Input Low Current	MODE, SEL, SVS	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage	QA, QB	I_{OH} = -8mA	2.6			V
V_{OL}	Output Low Voltage	QA, QB	I_{OL} = 8mA			0.5	V

Table 4D. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B}$, 2.5V ±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.8		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.6	V
I_{IH}	Input High Current	MODE, SEL, SVS	$V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	MODE, SEL, SVS	V_{DD} = 2.625V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage	QA, QB	I_{OH} = -8mA	1.8			V
V_{OL}	Output Low Voltage	QA, QB	I_{OL} = 8mA			0.5	V

Table 4E. Differential DC Characteristics, V_{DD} = 3.3V ±5% or V_{DD} = 2.5V ±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKA, CLKB, nCLKA, nCLKB	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLKA, CLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA
		nCLKA, nCLKB	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage[1]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[1 2]			1		$V_{DD} – (V_{PP}/2)$	V

NOTE: 1. V_{IL} should not be less than -0.3V and V_{IH} should not be higher than V_{DD}.

NOTE: 2. Common mode input voltage is defined at the crosspoint.

Table 4F. LVDS Differential DC Characteristics, V_{DD} = 3.3V ±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	390	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.05	1.2	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4G. LVDS Differential DC Characteristics, V_{DD} = 2.5V ±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	390	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.05	1.2	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = V_{DDO_A} = V_{DDO_B} = 3.3V ±5% or 2.5V ±5%, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
$\Delta V/\Delta t$	Input Edge Rate[2]	CLKA, CLKB	MODE = 0	1			V/ns
t_{PD}	Propagation Delay[3]	CLKA, CLKB to Q[0-3], nQ[0-3]		230	350	430	ps
	Propagation Delay[4]	CLKA, CLKB to QA, QB		1.00	1.31	1.72	ns
*tj*it(Ø)	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	Q[0-3], nQ[0-3]	f_{OUT} = 156.25MHz, Integration Range: 12kHz – 20MHz, MODE 0		65	100	fs
tsk(pp)	Part-to-Part Skew[5 6]	Q[0-3], nQ[0-3]				200	ps
tsk(o)	Output Skew[6]	Q[0-3], nQ[0-3][7]				65	ps
		QA-QB[8]; NOTE 4B				65	ps
		All outputs				1.3	ns
tsk(p)	Pulse Skew[9, 10]	Q[0-3], nQ[0-3]			10	60	ps
		QA, QB			85	200	ps
t_R / t_F	Output Rise/ Fall Time	QA, QB;	20% to 80%		250	350	ps
		Q[0-3], nQ[0-3]	20% to 80%		150	250	ps
$MUX_{ISOLATION}$	MUX Isolation[11]		f_{OUT} = 100.00MHz, V_{PP} = 400mV		40		dB

NOTE: 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: 2. In MODE = 1 sinusoidal input signals are permitted and no minimum input edge rate specification applies.

NOTE: 3. Measured from the differential input crosspoint to the differential output crosspoint using an input with 50% duty cycle.

NOTE: 4. Measured from the differential input crosspoint to the output at VDDO_X/2 using an input with 50% duty cycle.

NOTE: 5. Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE: 6. This parameter is defined in accordance with JEDEC Standard 65.

NOTE: 7. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE: 8. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO_X/2 of the output.

NOTE: 9. Output pulse skew $t_{SK(P)}$ is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

NOTE: 10. odc = input duty cycle ± ($t_{SK(p)}$/2 * 1/Output Period) * 100

NOTE: 11. Qx, nQx output measured differentially. See Parameter Measurement Information for MUX Isolation diagram.

Table 6. Characteristics for 1PPS operation, V_{DD} = 3.3V ±5% or V_{DD} = 2.5V ±5%, TA = -40°C to 85°C[1 2 3 4]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
T	Input and Output Pulse Period			1		s
T_P	Positive or negative pulse width		100			ns
t_{PD}	Propagation Delay;	CLKx/nCLKx to Qx/nQx		325	650	ps
tsk(p)	Pulse Width Distortion	CLKx/nCLKx to Qx/nQx		55	300	ps
tsk(o)	Output Skew[5]	Qx/nQx to Qy/nQy			325	ps
tsk(pp)	Part-to-Part Skew[6]				350	ps
t_R / t_F	Output Rise/Fall Time	10% to 90%	50	150	350	ps

NOTE: 1. 1PPS (one pulse per second) signals are defined as repetitive pulses with a rate (period) of 1Hz. The positive input pulse width may vary. The active signal edge is the rising edge. Parameters in this table are characterized for a positive input pulse width of 100ns, 100ms and 500ms; All device interfaces are DC-coupled. Parameters are defined in accordance with ITU-T G.703 Amendment 1 - Specifications for the physical layer of the ITU-T G8271/Y.1366 time synchronization interfaces.

NOTE: 2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: 3. t_{PD}, $t_{SK(O)}$, $t_{SK(P)}$ and $t_{SK(P)}$ parameters of differential signals are referenced to the crosspoint.

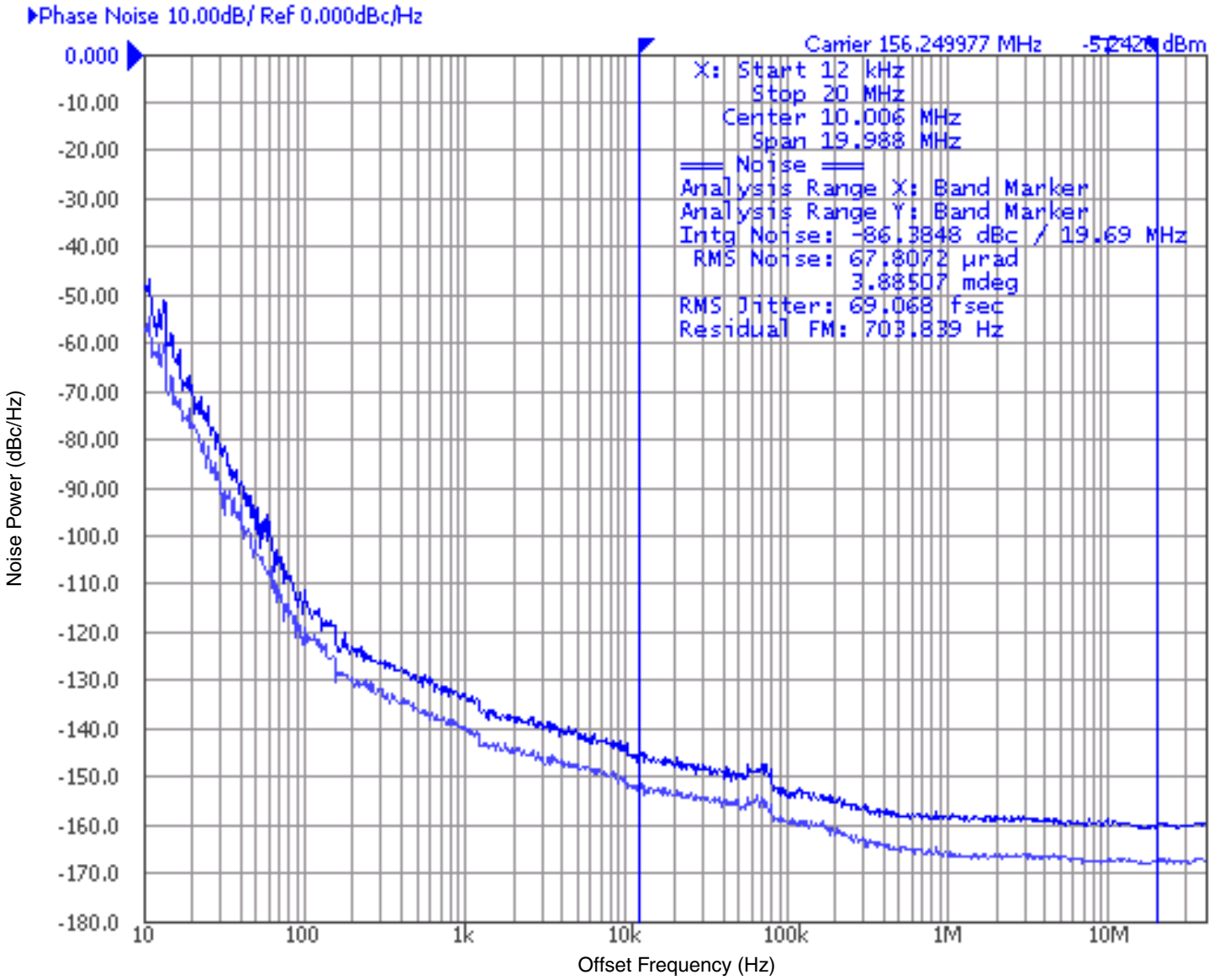
NOTE: 4. Differential outputs for 1PPS signal transmission are terminated balanced 100Ω according to the LVDS Output Load Test Circuit figures. The dedicated 1PPS outputs are the differential outputs Q0-Q3.

NOTE: 5. This parameter is defined in accordance with JEDEC Standard 65.

NOTE: 6. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Each device uses the same type of input.

Additive Phase Jitter

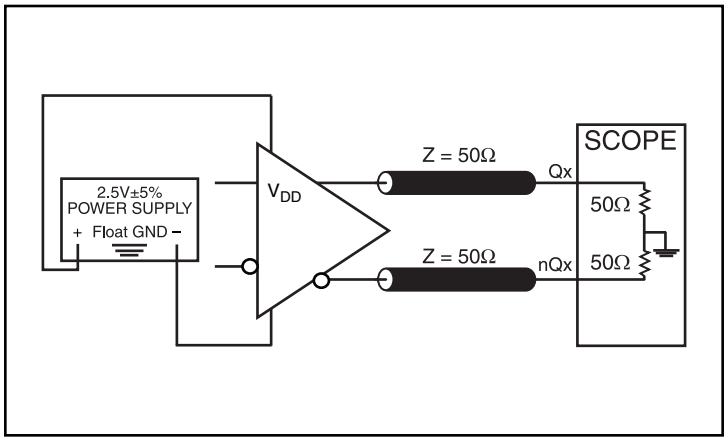
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



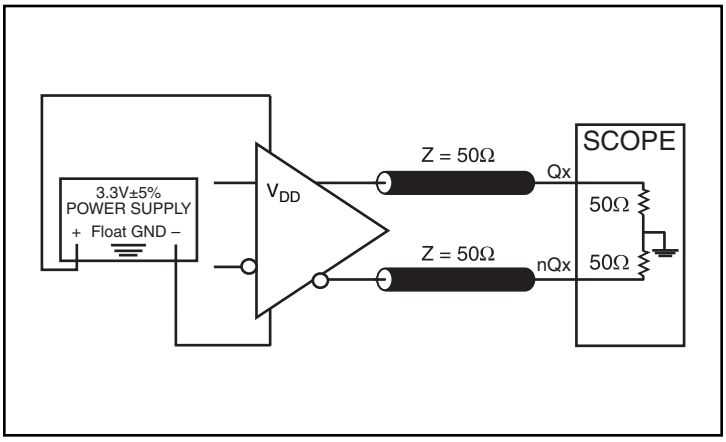
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using an Rohde & Schwarz SMA100 as the input source.

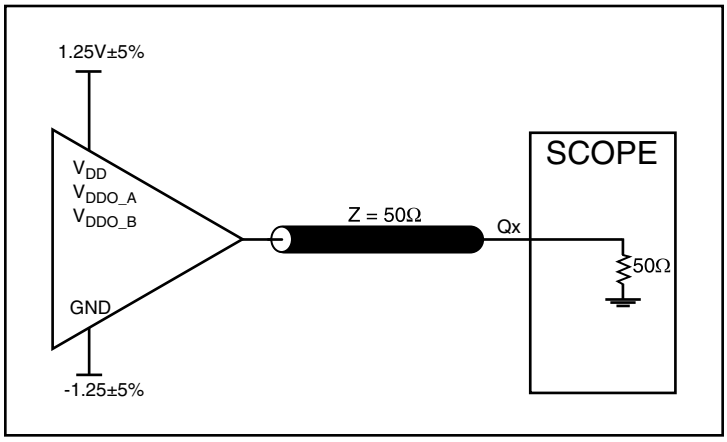
Parameter Measurement Information



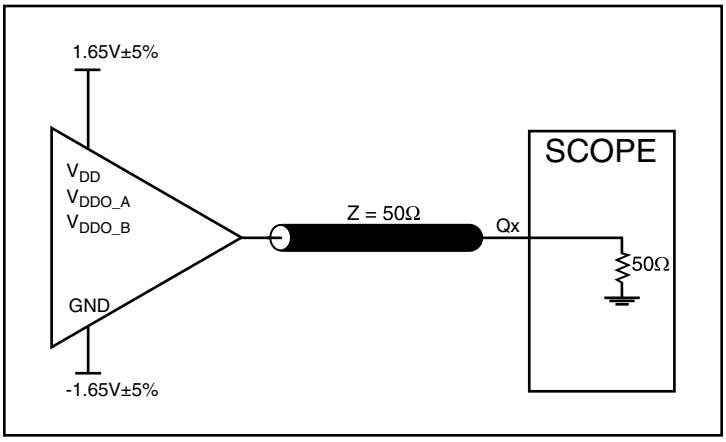
2.5V LVDS Output Load Test Circuit



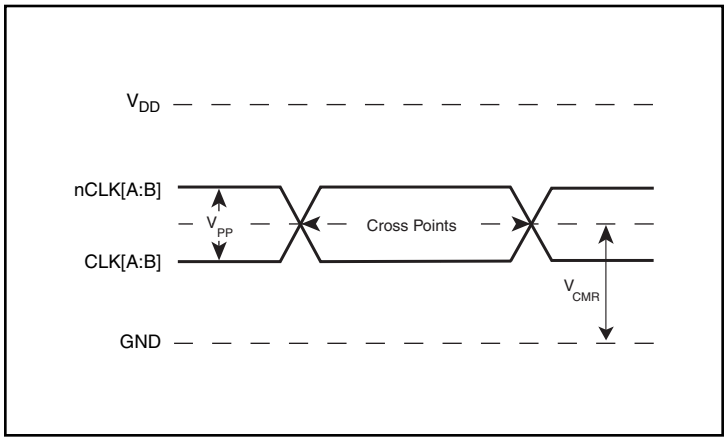
3.3V LVDS Output Load Test Circuit



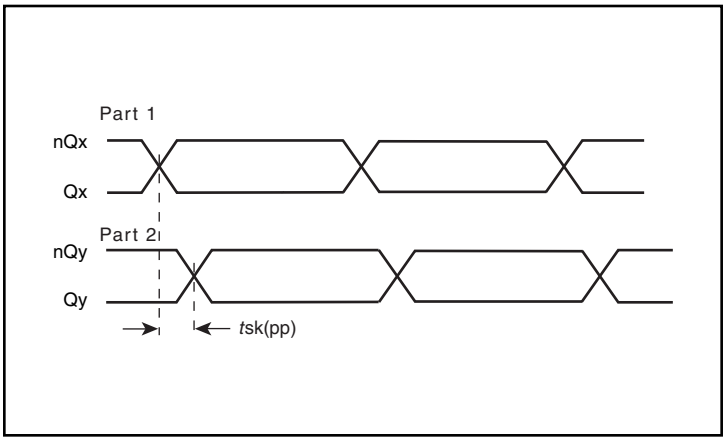
2.5V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/3.3V LVCMOS Output Load Test Circuit

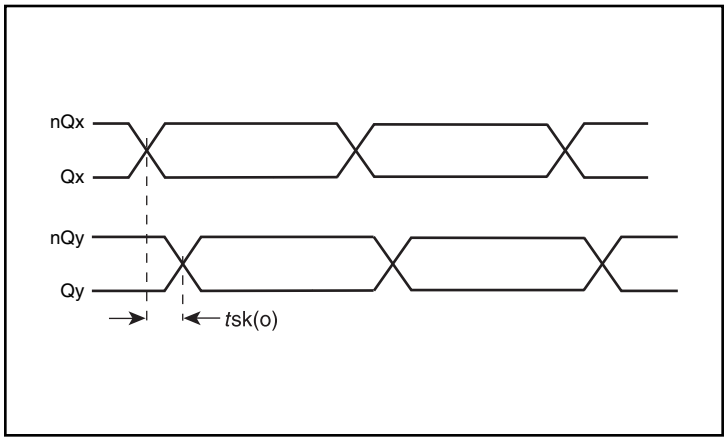


Differential Input Level

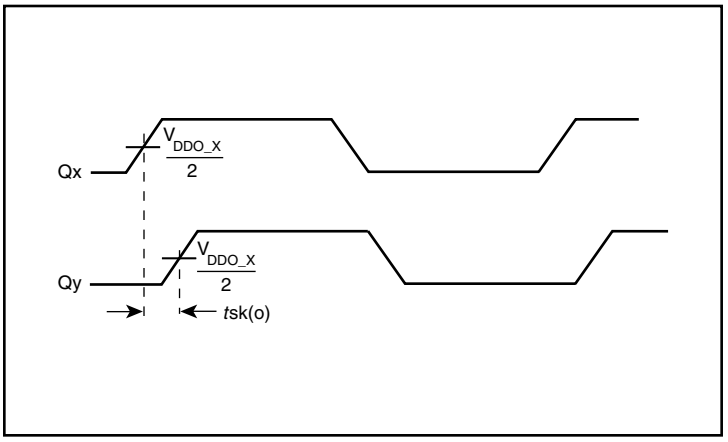


Part-to-Part Skew

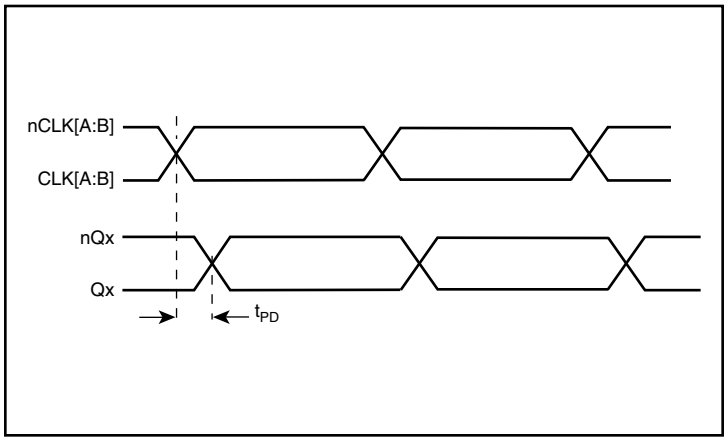
Parameter Measurement Information, Continued



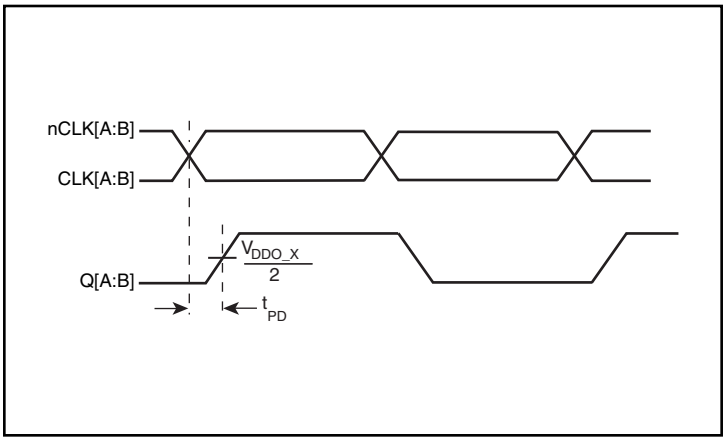
LVDS Output Skew



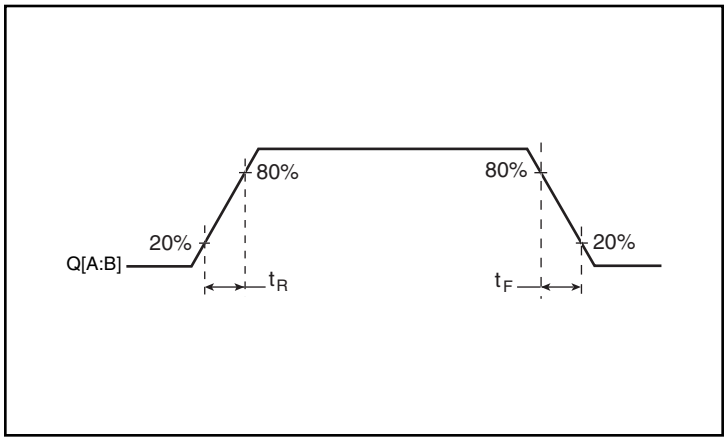
LVCMOS Output Skew



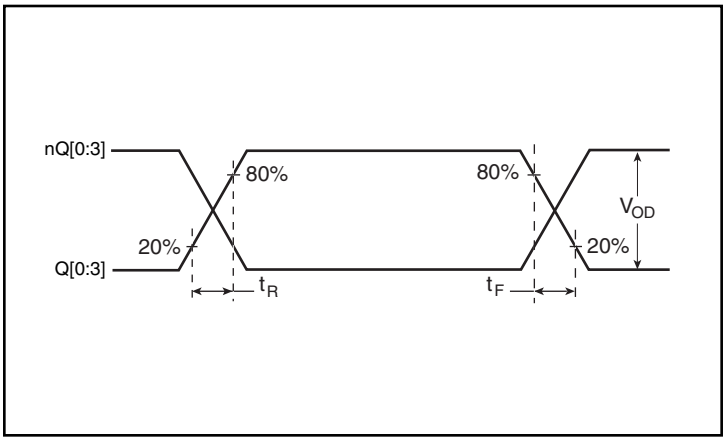
Differential Propagation Delay



Propagation Delay

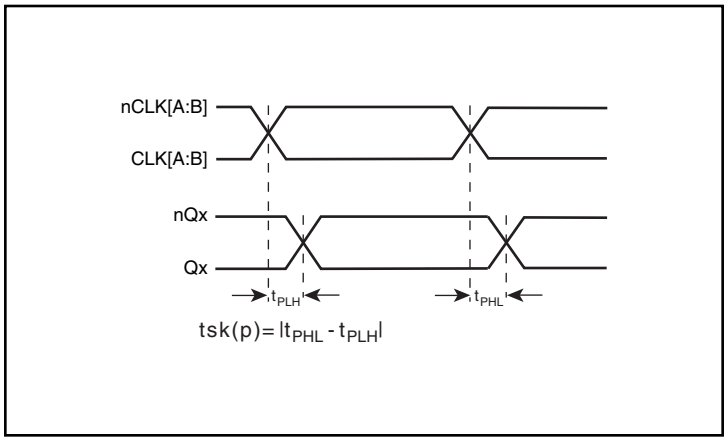


LVCMOS Output Rise/Fall Time

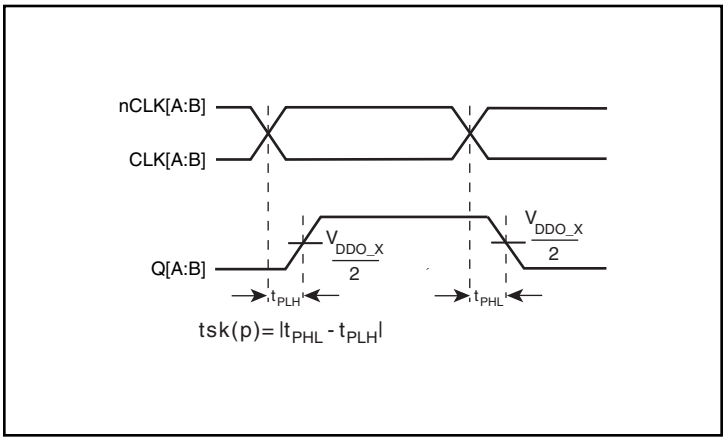


LVDS Output Rise/Fall Time

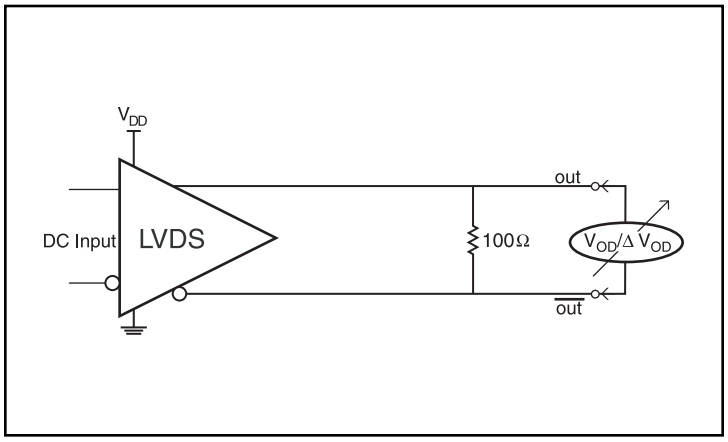
Parameter Measurement Information, Continued



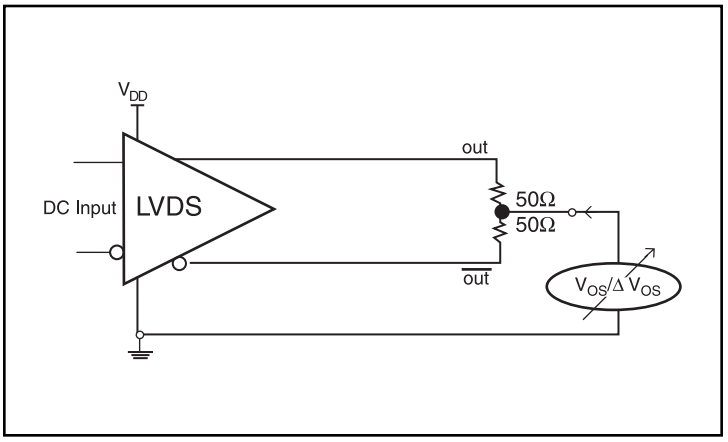
Differential Pulse Skew



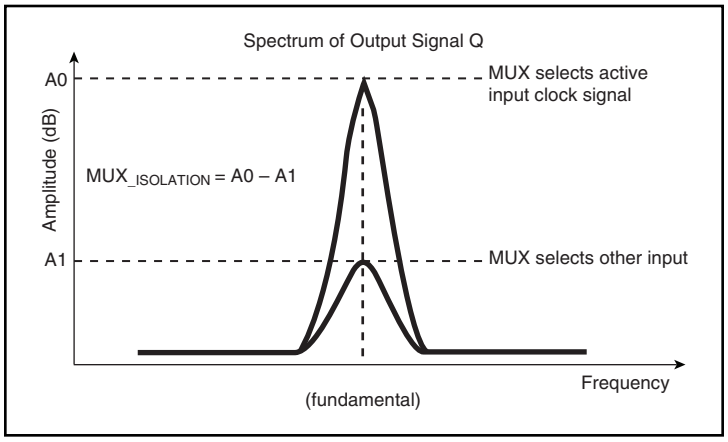
Pulse Skew



Differential Output Voltage Setup



Offset Voltage Setup



MUX Isolation

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

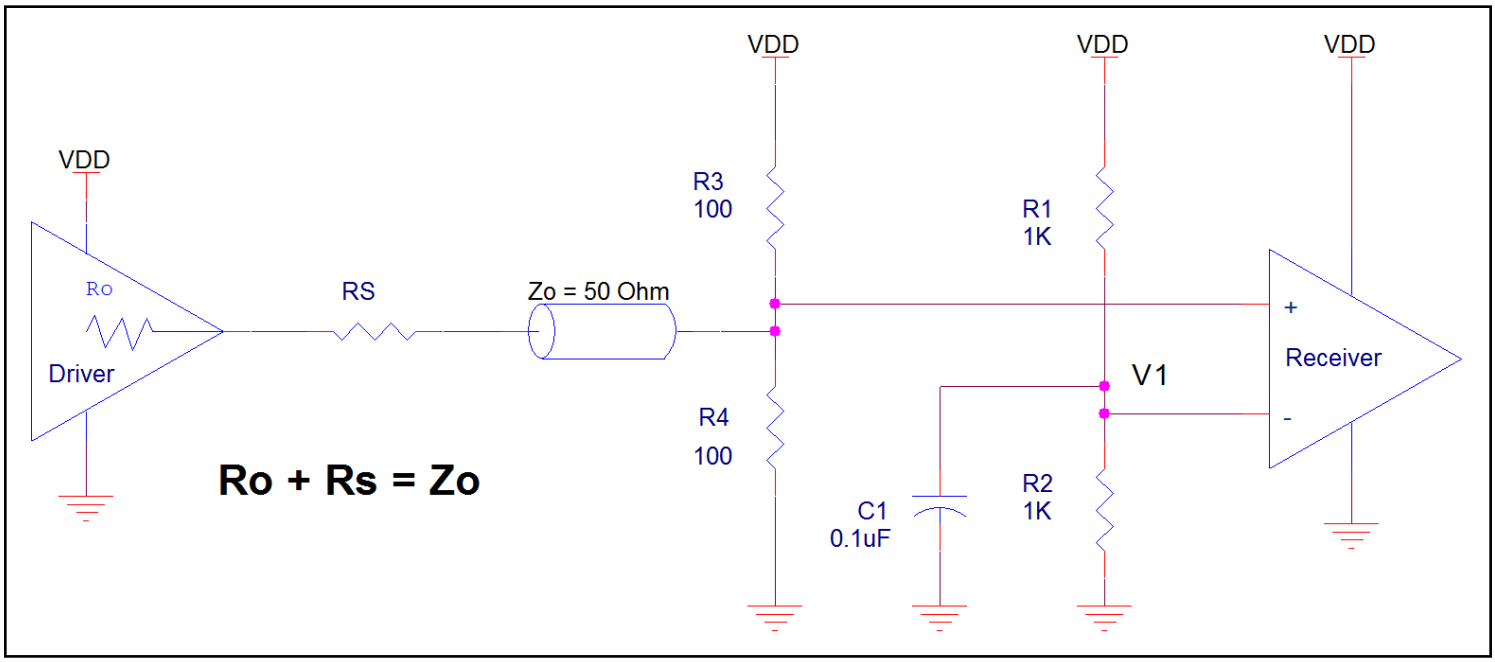


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Table 2A* to *Table 2C* show interface examples for the CLK/nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

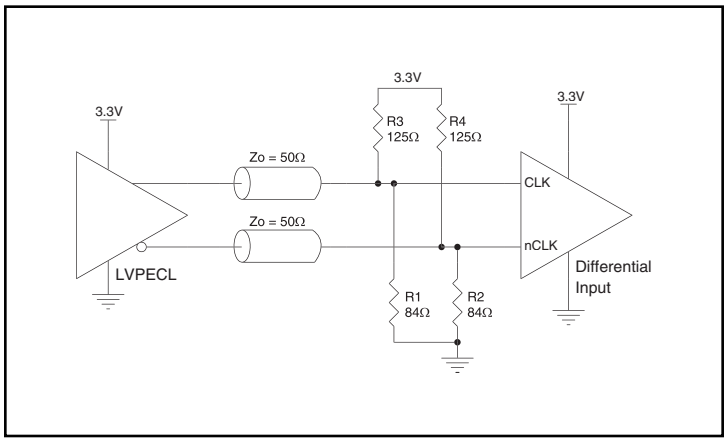


Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

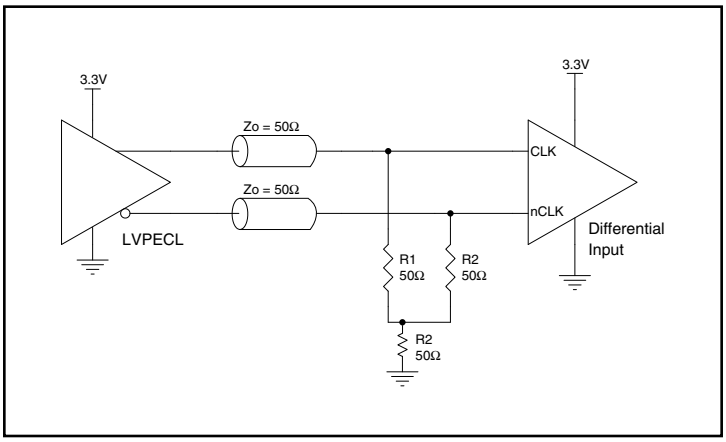


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

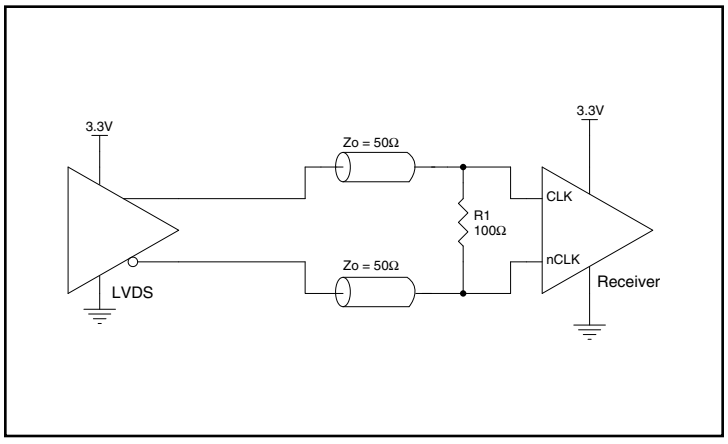


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A* to *Figure 3C* show interface examples for the CLK/nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

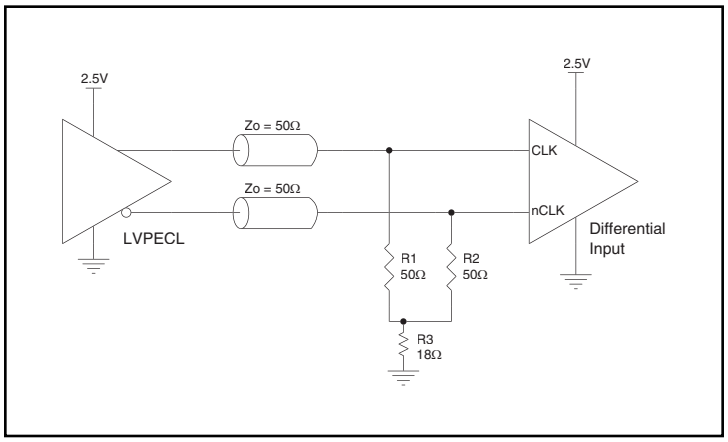


Figure 3A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

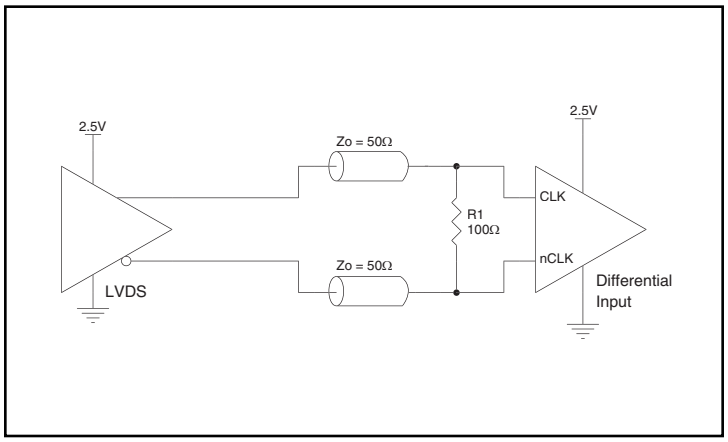


Figure 3B. CLK/nCLK Input Driven by a 2.5V LVDS Driver

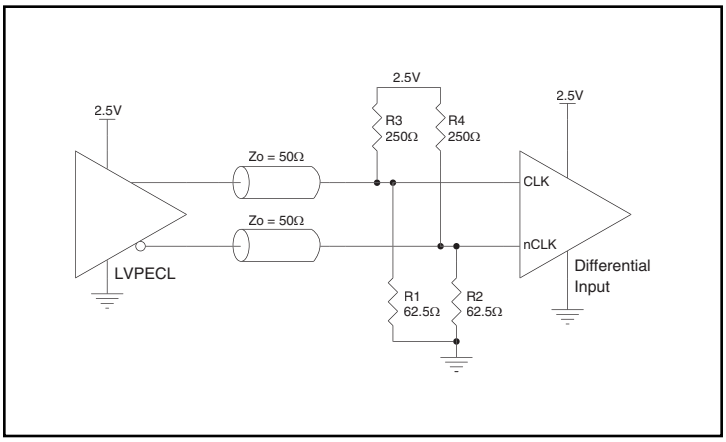


Figure 3C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullup resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Input

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

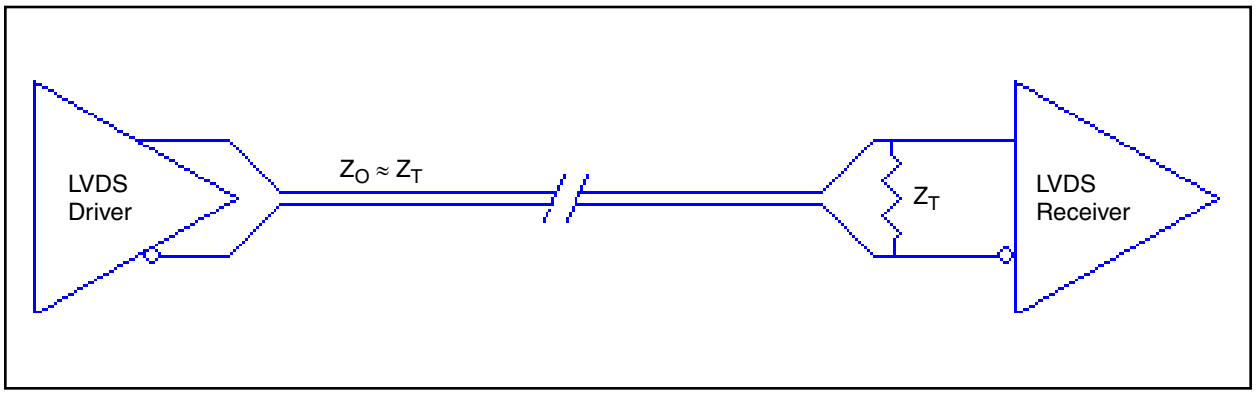


Figure 4A. Standard LVDS Termination

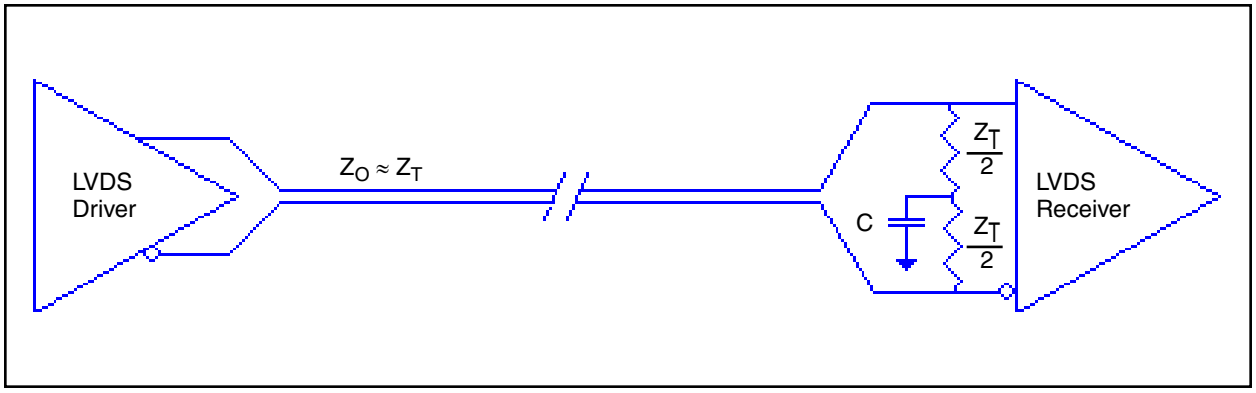


Figure 4B. Optional LVDS Termination

Power Considerations – LVDS Outputs

This section provides information on power dissipation and junction temperature for the 8V34S204 for all outputs that are configured to LVDS (LEV_SEL = 0). Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8V34S204 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD} = 108mA
I_{DDOA} = 4mA
I_{DDOB} = 4mA

- Power (core, LVDS)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDOA_MAX} + I_{DDOB_MAX})
  = 3.465V * (108mA + 4mA + 4mA) = **401.94mW**

LVCMOS Output Power Dissipation

•Dynamic Power Dissipation at 200MHz

Power (250MHz) = CPD * Frequency * (V_{DDOX_MAX})^2 = 6pF * 250MHz * (3.465V)^2 = **18.01mW per output**

Total CMOS Power = 2 * 18.01mW = **36.02mW**

Total Power$_{\_MAX}$ = 401.94mW + 36.02mW = **437.96mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 62.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.438W * 62.2°C/W = 112.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 56 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

Reliability Information

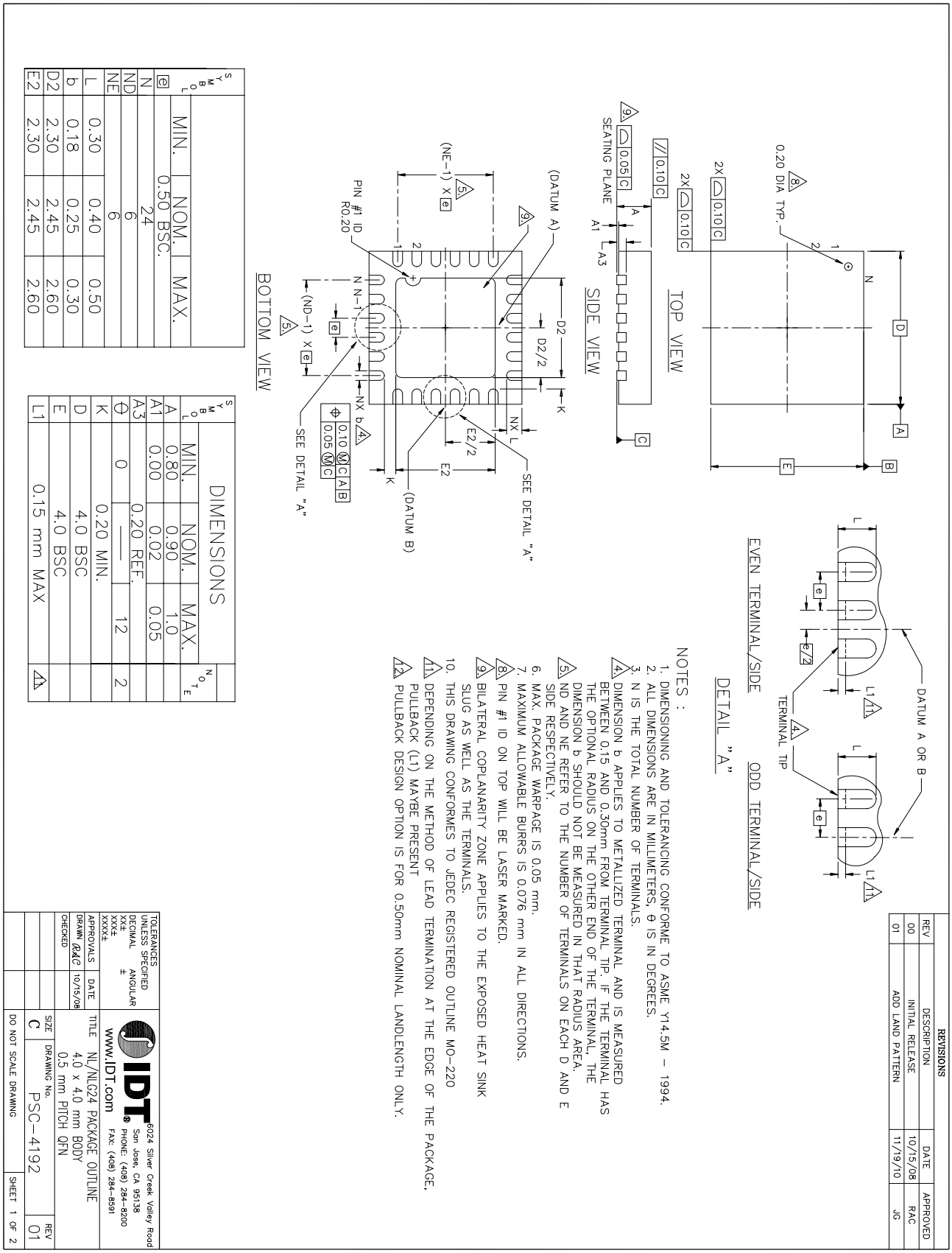
Table 8. θ_{JA} vs. Air FlowTable for a 24-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

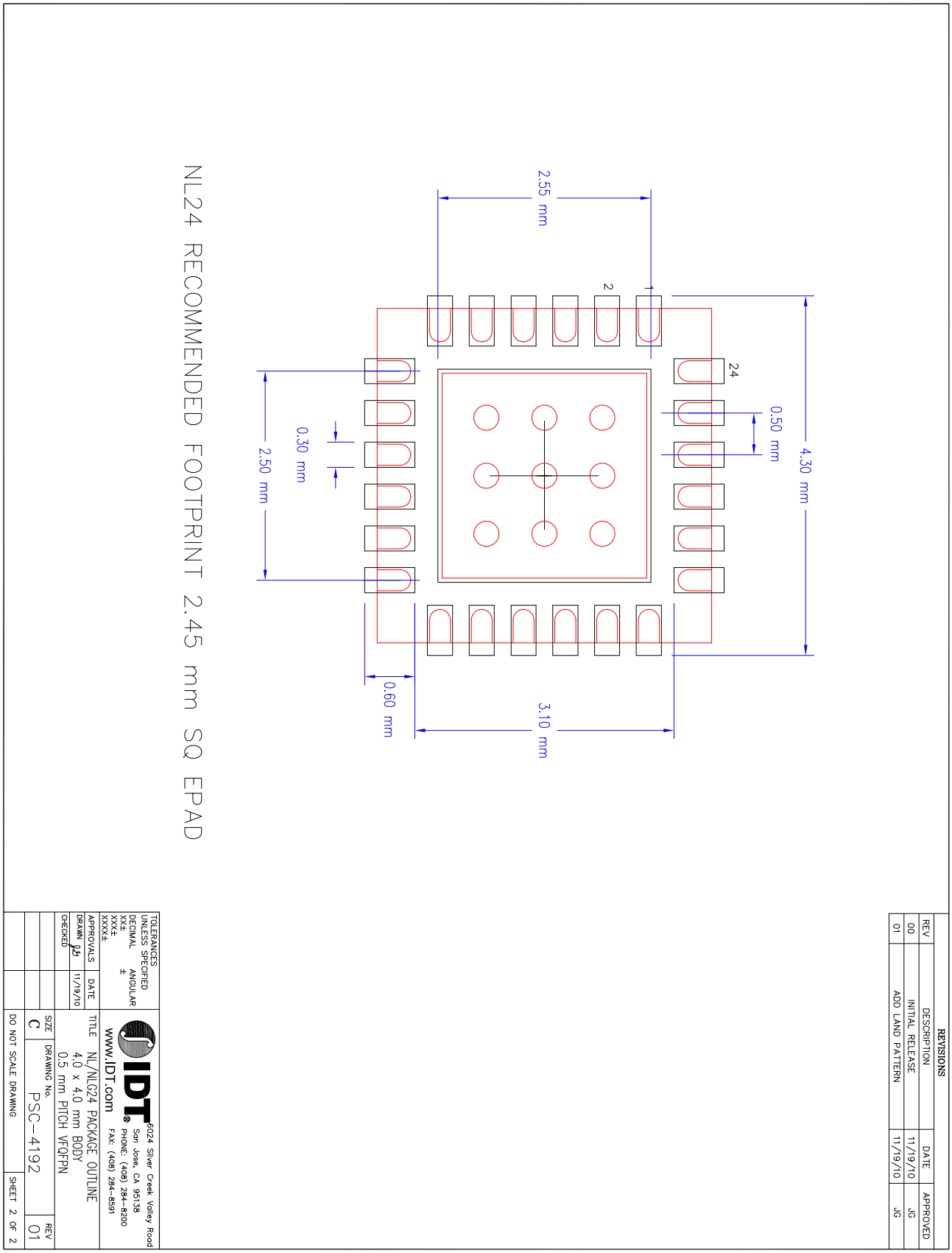
Transistor Count

The transistor count for the 8V34S204 is: 492

24-Lead VFQFN Package Information



24-Lead VFQFN Package Information



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V34S204NLGI	S204GI	“Lead-Free” 24-Lead VFQFN	Tray	-40°C to 85°C
8V34S204NLGI8	S204GI	“Lead-Free” 24-Lead VFQFN	Tape & Reel	-40°C to 85°C

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