

Four Output Differential Buffer for PCIe Gen 2 with Spread

ICS9DS400

General Description

The 9DS400 is pin compatible to the 9DB403, but adds the ability to inject spread spectrum onto the incoming differential clock, while maintaining good phase noise.

Recommended Application

DB400 where spread spectrum needs to be added to the incoming clock.

Key Specifications

- Output cycle-cycle jitter < 50ps
- Output to Output skew <50ps
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.0/3.1ps rms

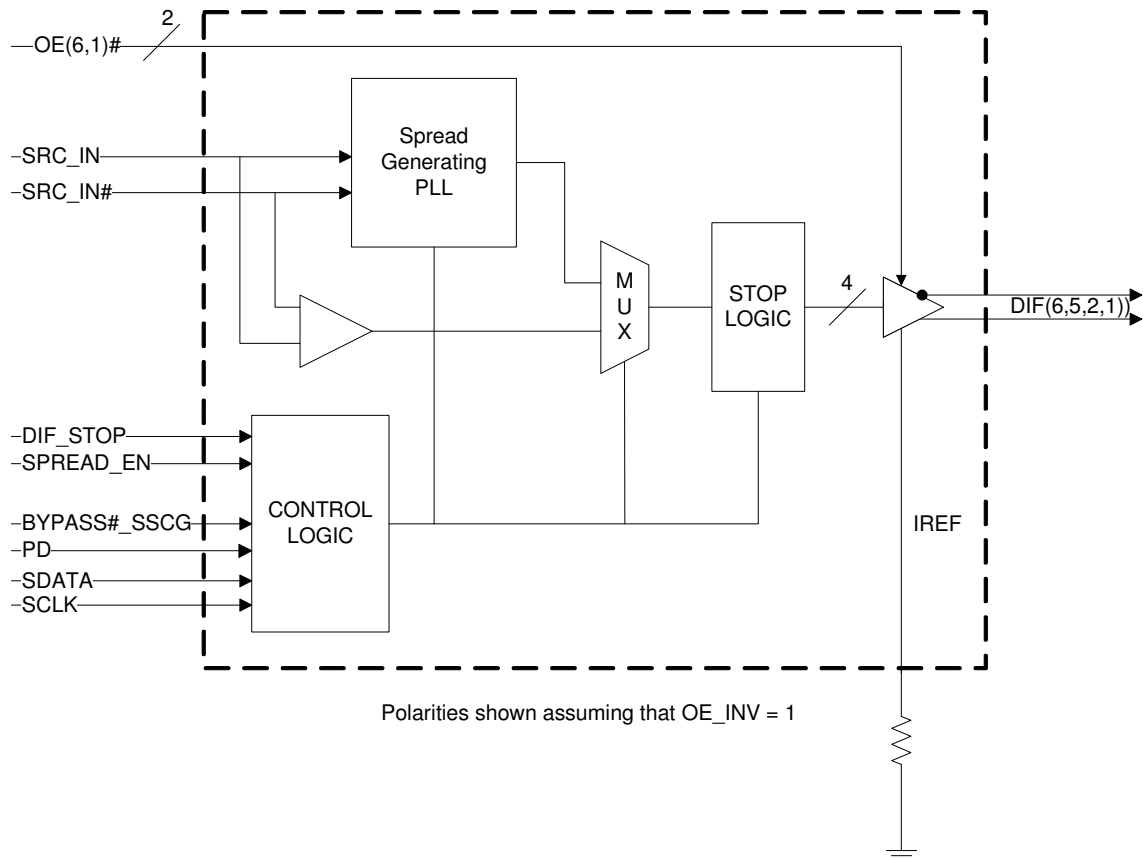
Features/Benefits

- Bypass mode
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

Output Features

- 4 - 0.7V current-mode differential output pairs.
- Supports Spread Injection mode and fanout mode.
- Two pin selectable down spread amounts: 0.5% and 0.25%.
- 50-110 MHz operation in PLL mode
- 50-400 MHz operation in Bypass mode

Functional Block Diagram



Pin Configuration

| | | | | |
|-------------------|----|------------------|----|-----------|
| VDD | 1 | ICS9DS400 | 28 | VDDA |
| SRC_IN | 2 | | 27 | GNDA |
| SRC_IN# | 3 | | 26 | IREF |
| GND | 4 | | 25 | OE_INV |
| VDD | 5 | | 24 | VDD |
| DIF_1 | 6 | | 23 | DIF_6 |
| DIF_1# | 7 | | 22 | DIF_6# |
| OE_1 | 8 | | 21 | OE_6 |
| DIF_2 | 9 | | 20 | DIF_5 |
| DIF_2# | 10 | | 19 | DIF_5# |
| VDD | 11 | | 18 | VDD |
| BYPASS#_SSCG | 12 | | 17 | SPREAD_EN |
| SCLK | 13 | | 16 | DIF_STOP# |
| SDATA | 14 | | 15 | PD# |
| OE_INV = 0 | | | | |

See Pin Description Table for pins w/internal pull up or pull down

| | | | | |
|-------------------|----|------------------|----|-----------------|
| VDD | 1 | ICS9DS400 | 28 | VDDA |
| SRC_IN | 2 | | 27 | GNDA |
| SRC_IN# | 3 | | 26 | IREF |
| GND | 4 | | 25 | OE_INV |
| VDD | 5 | | 24 | VDD |
| DIF_1 | 6 | | 23 | DIF_6 |
| DIF_1# | 7 | | 22 | DIF_6# |
| OE1# | 8 | | 21 | OE6# |
| DIF_2 | 9 | | 20 | DIF_5 |
| DIF_2# | 10 | | 19 | DIF_5# |
| VDD | 11 | | 18 | VDD |
| BYPASS#_SSCG | 12 | | 17 | SPREAD_EN |
| SCLK | 13 | | 16 | DIF_STOP |
| SDATA | 14 | | 15 | PD |
| OE_INV = 1 | | | | |

See Pin Description Table for pins w/internal pull up or pull down

Power Groups

| Pin Number | | Description |
|---------------|-----|-------------------------------|
| VDD | GND | |
| 1 | 4 | SRC_IN/SRC_IN# |
| 5, 11, 18, 24 | 4 | DIF(1,2,5,6) |
| N/A | 27 | IREF |
| 28 | 27 | Analog VDD & GND for PLL_core |

Pin Description for OE_INV = 0

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION | INTERNAL PULL UP OR PULL DOWN? |
|-------|--------------|----------|---|--------------------------------|
| 1 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input | N/A |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input | N/A |
| 4 | GND | PWR | Ground pin. | N/A |
| 5 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 6 | DIF_1 | OUT | 0.7V differential true clock output | N/A |
| 7 | DIF_1# | OUT | 0.7V differential Complementary clock output | N/A |
| 8 | OE_1 | IN | Active high input for enabling output 1. 0 = tri-state outputs, 1= enable outputs | PULL UP |
| 9 | DIF_2 | OUT | 0.7V differential true clock output | N/A |
| 10 | DIF_2# | OUT | 0.7V differential Complementary clock output | N/A |
| 11 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 12 | BYPASS#_SSCG | IN | Input to select Bypass(fan-out) or SSCG (PLL) mode 0 = Bypass mode, 1= SSCG mode | PULL UP |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. | N/A |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 3.3V tolerant. | N/A |
| 15 | PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped. | PULL UP |
| 16 | DIF_STOP# | IN | Active low input to stop differential output clocks. | PULL UP |
| 17 | SPREAD_EN | IN | Asynchronous, active high input to enable spread spectrum functionality. | PULL UP |
| 18 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 19 | DIF_5# | OUT | 0.7V differential Complementary clock output | N/A |
| 20 | DIF_5 | OUT | 0.7V differential true clock output | N/A |
| 21 | OE_6 | IN | Active high input for enabling output 6. 0 = tri-state outputs, 1= enable outputs | PULL UP |
| 22 | DIF_6# | OUT | 0.7V differential Complementary clock output | N/A |
| 23 | DIF_6 | OUT | 0.7V differential true clock output | N/A |
| 24 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#) | N/A |
| 26 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. | N/A |
| 27 | GNDA | PWR | Ground pin for the PLL core. | N/A |
| 28 | VDDA | PWR | 3.3V power for the PLL core. | N/A |

Pin Description for OE_INV = 1

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION | INTERNAL PULL UP OR PULL DOWN? |
|-------|------------------|----------|---|--------------------------------|
| 1 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input | N/A |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input | N/A |
| 4 | GND | PWR | Ground pin. | N/A |
| 5 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 6 | DIF_1 | OUT | 0.7V differential true clock output | N/A |
| 7 | DIF_1# | OUT | 0.7V differential Complementary clock output | N/A |
| 8 | OE1# | IN | Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs | PULL UP |
| 9 | DIF_2 | OUT | 0.7V differential true clock output | N/A |
| 10 | DIF_2# | OUT | 0.7V differential Complementary clock output | N/A |
| 11 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 12 | BYPASS#_SS CG | IN | Input to select Bypass(fan-out) or SSCG (PLL) mode 0 = Bypass mode, 1 = SSCG mode | PULL UP |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. | N/A |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 3.3V tolerant. | N/A |
| 15 | PD | IN | Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped. | PULL UP |
| 16 | DIF_STOP | IN | Active High input to stop differential output clocks. | PULL UP |
| 17 | SPREAD_EN | IN | Asynchronous, active high input to enable spread spectrum functionality. | PULL UP |
| 18 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 19 | DIF_5# | OUT | 0.7V differential Complementary clock output | N/A |
| 20 | DIF_5 | OUT | 0.7V differential true clock output | N/A |
| 21 | OE6# | IN | Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs | PULL UP |
| 22 | DIF_6# | OUT | 0.7V differential Complementary clock output | N/A |
| 23 | DIF_6 | OUT | 0.7V differential true clock output | N/A |
| 24 | VDD | PWR | Power supply, nominal 3.3V | N/A |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#) | N/A |
| 26 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. | N/A |
| 27 | GNDA | PWR | Ground pin for the PLL core. | N/A |
| 28 | VDDA | PWR | 3.3V power for the PLL core. | N/A |

Absolute Max

| Symbol | Parameter | Min | Max | Units |
|-------------------|---------------------------------------|---------|-----------------------|-------|
| VDD | 3.3V Supply Voltage | | 4.6 | V |
| V _{IL} | Input Low Voltage | GND-0.5 | | V |
| V _{IH} | Input High Voltage | | V _{DD} +0.5V | V |
| T _s | Storage Temperature | -65 | 150 | °C |
| T _{case} | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | | V |

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A =Over the Specified Operating Range; V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Input High Voltage | V _{IH} | 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | 3.3 V +/-5% | GND - 0.3 | | 0.8 | V | 1 |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Operating Supply Current | I _{DD3.3OP} | Full Active, C _L = Full load; | | | 125 | mA | 1 |
| Powerdown Current | I _{DD3.3PD} | all diff pairs driven | | | 30 | mA | 1 |
| | | all differential pairs tri-stated | | | 6 | mA | 1 |
| Input Frequency | F _{IPLL} | PCIe Mode (Bypass#/PLL= 1) | 90 | 100.00 | 110 | MHz | 1 |
| | F _{IBYPASS} | Bypass Mode ((Bypass#/PLL= 0) | 33 | | 400 | MHz | 1 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except SRC_IN | 1.5 | | 5 | pF | 1 |
| | C _{INSRC_IN} | SRC_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| SS Modulation Frequency | f _{MOD} | Assuming 100 MHz input (Triangular Modulation) | 30 | 32.000 | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | cycles | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of PD# and SRC_STOP# | | | 5 | ns | 1 |
| Trise | t _R | Rise time of PD# and SRC_STOP# | | | 5 | ns | 2 |
| SMBus Voltage | V _{MAX} | Maximum input voltage | | | 5.5 | V | 1 |
| Low-level Output Voltage | V _{OL} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| Current sinking at V _{OL} | I _{PULLUP} | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | t _{FSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²See timing diagrams for timing requirements.

³Time from deassertion until outputs are >200 mV

⁴SRC_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics - Differential Clock Input Parameters

TA =Over the Specified Operating Range; VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|--|----------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | $V_{IH\text{DIF}}$ | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | $V_{IL\text{DIF}}$ | Differential inputs (single-ended measurement) | $V_{SS} - 300$ | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V_{COM} | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V_{SWING} | Peak to Peak value | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}, V_{IN} = GND$ | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J_{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through $V_{swing\ min}$ centered around differential zero

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

TA =Over the Specified Operating Range; VDD = 3.3 V +/-5%; CL =2pF, RS=33Ω, RP=49.9Ω, RREF=475Ω

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES | |
|---------------------------------|------------------------|--|------|-----|------|------------|------------|-------|
| Current Source Output Impedance | Zo ¹ | | 3000 | | | Ω | 1 | |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,2 | |
| Voltage Low | VLow | | -150 | | 150 | | | |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 | |
| Min Voltage | Vuds | | -300 | | | | | |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 | |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 | |
| Rise Time | t _r | V _{OL} = 0.175V, V _{OH} = 0.525V | 175 | | 700 | ps | 1 | |
| Fall Time | t _f | V _{OH} = 0.525V V _{OL} = 0.175V | 175 | | 700 | ps | 1 | |
| Rise Time Variation | d-t _r | | | | 125 | ps | 1 | |
| Fall Time Variation | d-t _f | | | | 125 | ps | 1 | |
| Duty Cycle | d _{i3} | Measurement from differential waveform | 45 | | 55 | % | 1 | |
| Skew, Input to Output | t _{pdBYP} | Bypass Mode, V _T = 50% | 2500 | | 4500 | ps | 1 | |
| | t _{pdPLL} | PLL Mode V _T = 50%, Spread Off | -250 | | 250 | ps | 1 | |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | | 50 | ps | 1 | |
| Jitter, Cycle to cycle | t _{jyc-cyc} | PLL mode | | | 50 | ps | 1,3 | |
| | | Additive Jitter in Bypass Mode | | | 50 | ps | 1,3 | |
| Jitter, Phase | t _{jphaseBYP} | PCIe Gen1 phase jitter (Additive in Bypass Mode) | | | 10 | ps (pk2pk) | 1,4,5 | |
| | | PCIe Gen 2 Low Band phase jitter (Additive in Bypass Mode) | | | 0.1 | ps (rms) | 1,4,5 | |
| | | PCIe Gen 2 High Band phase jitter (Additive in Bypass Mode) | | | 0.5 | ps (rms) | 1,4,5 | |
| | t _{jphasePLL} | PCIe Gen 1 phase jitter | | | | 86 | ps (pk2pk) | 1,4,5 |
| | | PCIe Gen 2 Low Band phase jitter | | | | 3 | ps (rms) | 1,4,5 |
| | | PCIe Gen 2 High Band phase jitter | | | | 3.1 | ps (rms) | 1,4,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

³ Measured from differential waveform

⁴ See <http://www.pcisig.com> for complete specs

⁵ Device driven by 932S421C or equivalent.

Clock Periods Differential Outputs with Spread Spectrum Enabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | Units | Notes |
|--------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | | |
| Signal Name | DIF 100 | 9.87400 | 9.99900 | 9.99900 | 10.00000 | 10.00100 | 10.05130 | 10.17630 | ns | 1,2,3 |
| | DIF 133 | 7.41425 | 7.49925 | 7.49925 | 7.50000 | 7.50075 | 7.53845 | 7.62345 | ns | 1,2,4 |
| | DIF 166 | 5.91440 | 5.99940 | 5.99940 | 6.00000 | 6.00060 | 6.03076 | 6.11576 | ns | 1,2,4 |
| | DIF 200 | 4.91450 | 4.99950 | 4.99950 | 5.00000 | 5.00050 | 5.02563 | 5.11063 | ns | 1,2,4 |
| | DIF 266 | 3.66463 | 3.74963 | 3.74963 | 3.75000 | 3.75038 | 3.76922 | 3.85422 | ns | 1,2,4 |
| | DIF 333 | 2.91470 | 2.99970 | 2.99970 | 3.00000 | 3.00030 | 3.01538 | 3.10038 | ns | 1,2,4 |
| | DIF 400 | 2.41475 | 2.49975 | 2.49975 | 2.50000 | 2.50025 | 2.51282 | 2.59782 | ns | 1,2,4 |

Clock Periods Differential Outputs with Spread Spectrum Disabled

| Measurement Window | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | Units | Notes |
|--------------------|---------|-------------------------|-------------------------|-------------------------|----------|-------------------|--------------------|----------|-------|-------|
| Symbol | | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | | |
| Signal Name | DIF 100 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.17630 | ns | 1,2,3 |
| | DIF 133 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.62345 | ns | 1,2,4 |
| | DIF 166 | 5.91440 | | 5.99940 | 6.00000 | 6.00060 | | 6.11576 | ns | 1,2,4 |
| | DIF 200 | 4.91450 | | 4.99950 | 5.00000 | 5.00050 | | 5.11063 | ns | 1,2,4 |
| | DIF 266 | 3.66463 | | 3.74963 | 3.75000 | 3.75038 | | 3.85422 | ns | 1,2,4 |
| | DIF 333 | 2.91470 | | 2.99970 | 3.00000 | 3.00030 | | 3.10038 | ns | 1,2,4 |
| | DIF 400 | 2.41475 | | 2.49975 | 2.50000 | 2.50025 | | 2.59782 | ns | 1,2,4 |

¹Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410B/CK505 accuracy requirements. The 9DS400/800 itself does not contribute to ppm error.

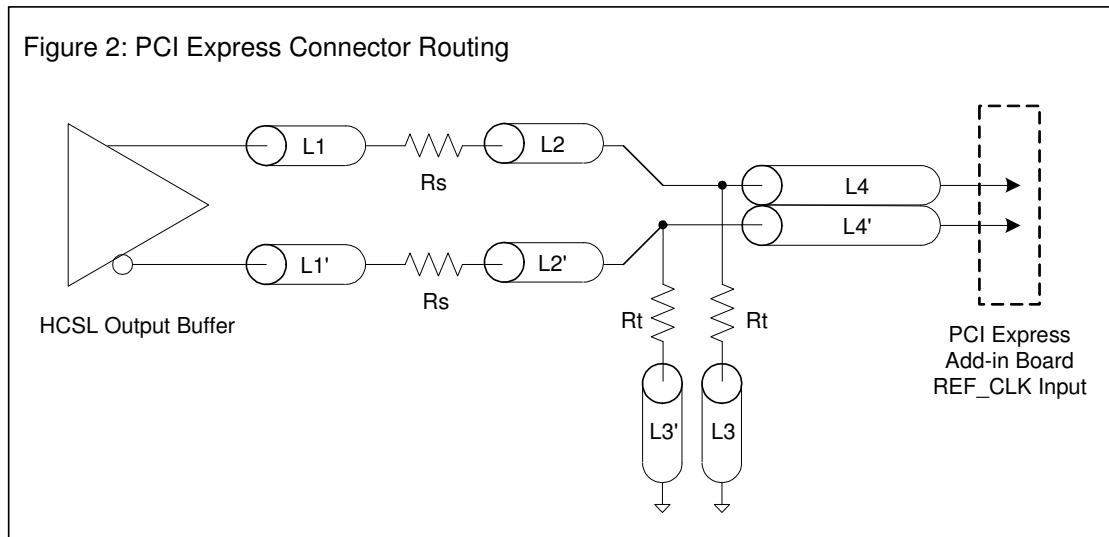
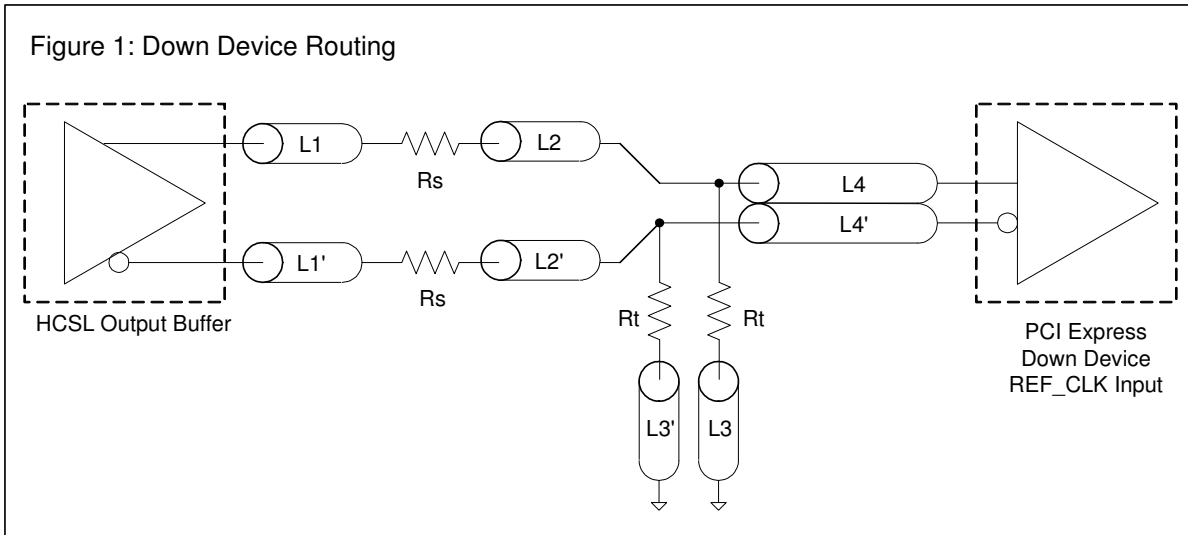
³ Driven by SRC output of main clock, PLL or Bypass mode

⁴ Driven by CPU output of CK410B/CK505 main clock, **Bypass mode only**

| SRC Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

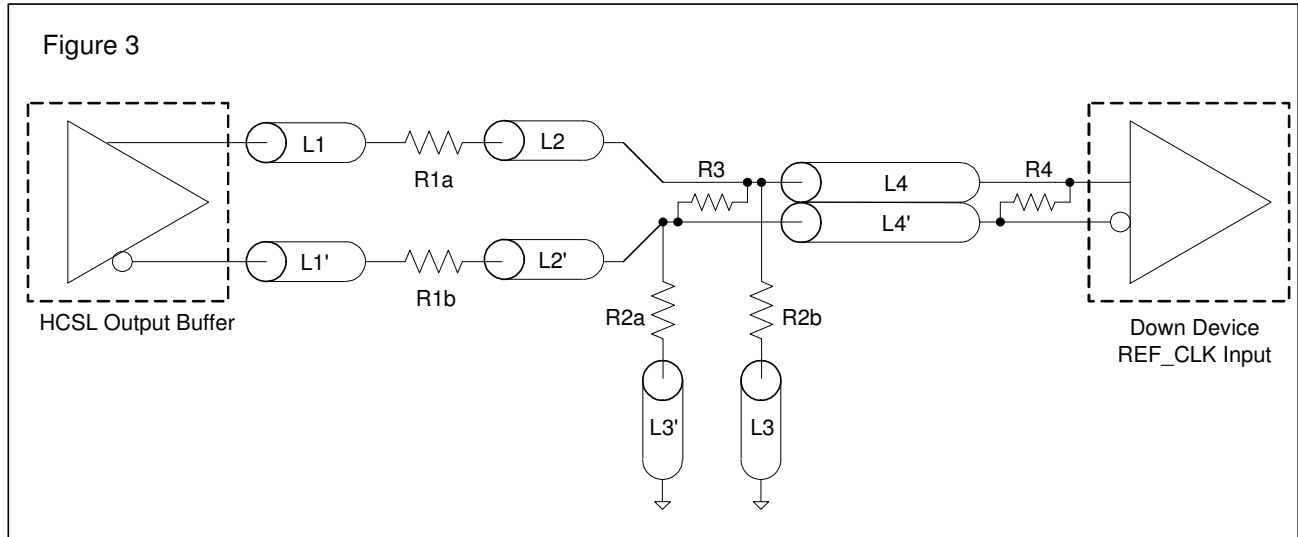
| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

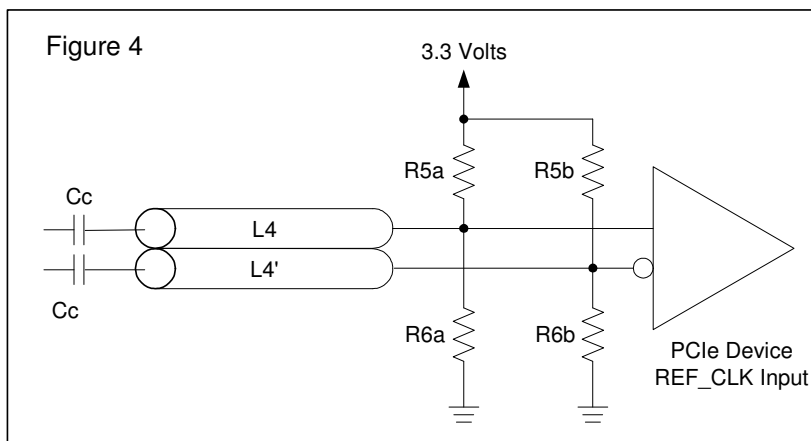


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



General SMBus serial interface information for the ICS9DS400

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D8_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D8_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D9_{(h)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(h)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D8_{(h)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | X Byte | |
| ◊ | | ACK |
| ◊ | | ◊ |
| ◊ | | ◊ |
| ◊ | | ◊ |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | | |
|----------------------------|-----------------|----------------------|------------------|
| Controller (Host) | | ICS (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address $D8_{(h)}$ | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address $D9_{(h)}$ | | | |
| RD | ReaD | | |
| | | ACK | |
| | | Data Byte Count = X | |
| ACK | | | |
| ACK | | X Byte | |
| | | | Beginning Byte N |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (D8/D9)

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default | |
|--------|-------|---------------|----------------------------------|------|-----------------------------|------------|---------|---|
| Bit 7 | - | PD_Mode | PD# drive mode | RW | driven | Hi-Z | 0 | |
| Bit 6 | - | STOP_Mode | SRC_Stop# drive mode | RW | driven | Hi-Z | 0 | |
| Bit 5 | - | Reserved | | | | | | 0 |
| Bit 4 | 1 | SPREAD_AMT(1) | Spread % MSB | RW | 00 = -0.125% 01 = -0.25% | | Latch | |
| Bit 3 | - | SPREAD_AMT(0) | Spread % LSB | RW | 10 = -0.375% 11 = -0.50% | | 1 | |
| Bit 2 | 28 | SPREAD_EN | Turns on spread | RW | SS Off | SS On | Latch | |
| Bit 1 | 22 | BYPASS# | BYPASS# SSCG | RW | fan-out | SSCG | Latch | |
| Bit 0 | - | Byte0 CONTROL | Selects control source of Byte 0 | RW | Smbus | Input Pins | 1 | |

Notes: Pins 1, 22 and 28 are latched into Byte 0 on the first power up of the device. Bits [4:1] will NOT reflect changes in these pin states after power up, even though the pins are controlling the function of the part. Setting Byte 0 bit 0 to 0 allows the SMBus to write Bits [4:1] and transfers control of the functions from the pins to SMBus. Once Byte 0 bit 0 is set to 0, the pins no longer impact Byte 0, bits [4:1] or the device function.

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|----------|--------|---------|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 6 | 22,23 | DIF_6 | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | 19,20 | DIF_5 | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | 1 |
| Bit 2 | 9,10 | DIF_2 | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | 6,7 | DIF_1 | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | 1 |

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run!

SMBus Table: OE Pin Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|--------------------------|------|----------|-----------|---------|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 6 | 22,23 | DIF_6 | DIF_6 Stoppable with OE6 | RW | Free-run | Stoppable | 0 |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 2 | - | Reserved | Reserved | RW | Reserved | | 0 |
| Bit 1 | 6,7 | DIF_1 | DIF_1 Stoppable with OE1 | RW | Free-run | Stoppable | 0 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | 0 |

SMBus Table: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | X |
| Bit 6 | | | Reserved | | | | X |
| Bit 5 | | | Reserved | | | | X |
| Bit 4 | | | Reserved | | | | X |
| Bit 3 | | | Reserved | | | | X |
| Bit 2 | | | Reserved | | | | X |
| Bit 1 | | | Reserved | | | | X |
| Bit 0 | | | Reserved | | | | X |

SMBus Table: Vendor & Revision ID Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | - | RID2 | | R | - | - | 0 |
| Bit 5 | - | RID1 | | R | - | - | 0 |
| Bit 4 | - | RID0 | | R | - | - | 0 |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBus Table: DEVICE ID

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-------------------|------|--|---|---------|
| Bit 7 | - | | Device ID 7 (MSB) | R | Device ID is 80 Hex for 9DS800 and 40 Hex for 9DS400 | | X |
| Bit 6 | - | | Device ID 6 | R | | X | |
| Bit 5 | - | | Device ID 5 | R | | 0 | |
| Bit 4 | - | | Device ID 4 | R | | 0 | |
| Bit 3 | - | | Device ID 3 | R | | 0 | |
| Bit 2 | - | | Device ID 2 | R | | 0 | |
| Bit 1 | - | | Device ID 1 | R | | 0 | |
| Bit 0 | - | | Device ID 0 | R | | 0 | |

SMBus Table: Byte Count Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

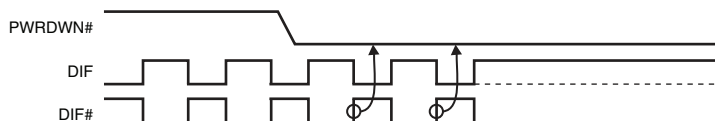
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

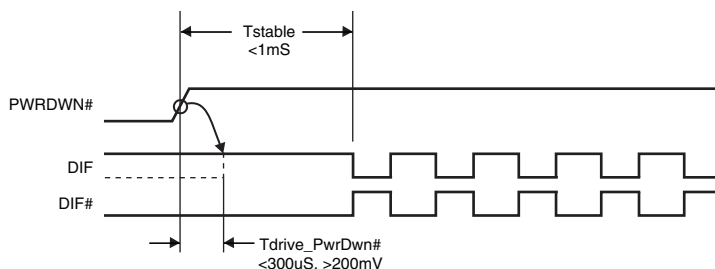
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with $2 \times I_{REF}$ and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.



DIF_STOP#

The DIF_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on DIF_IN for this input to work properly. The DIF_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

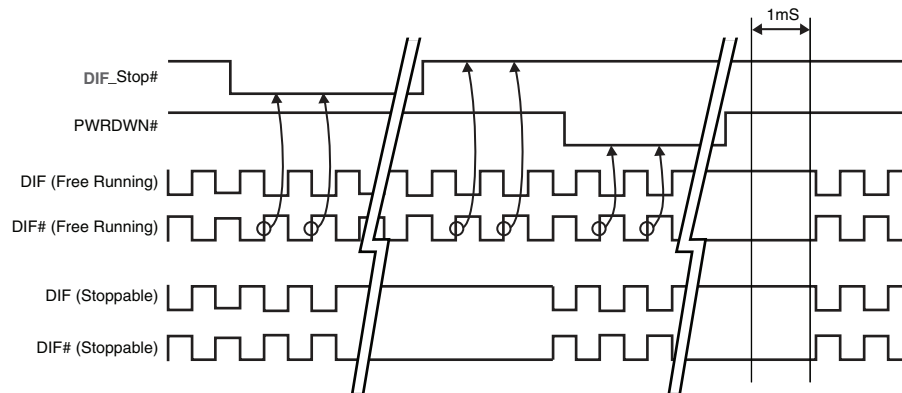
DIF_STOP# - Assertion

Asserting DIF_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the DIF_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with $6 \times I_{REF}$. DIF# is not driven, but pulled low by the termination. When the DIF_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

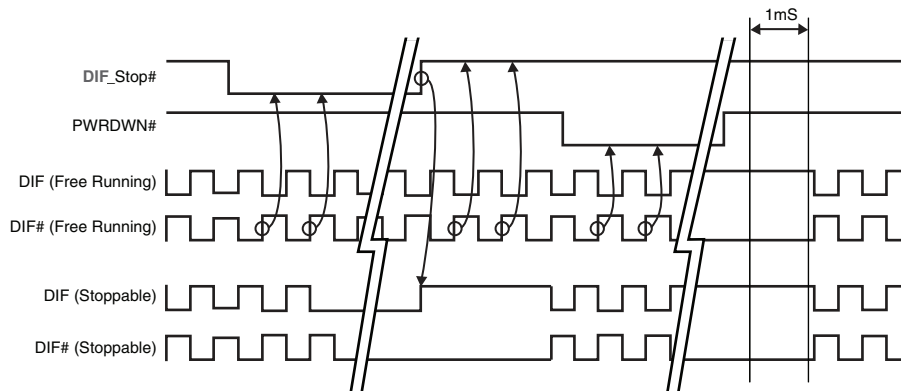
DIF_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the DIF_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

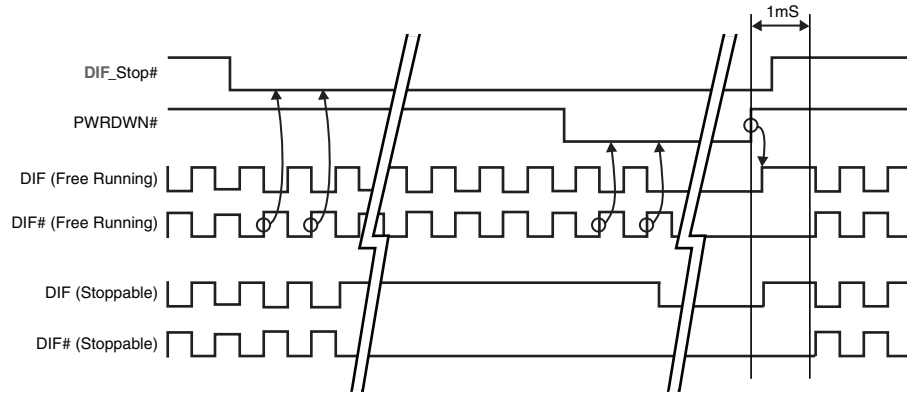
DIF_STOP_1 (DIF_Stop = Driven, PD = Driven)



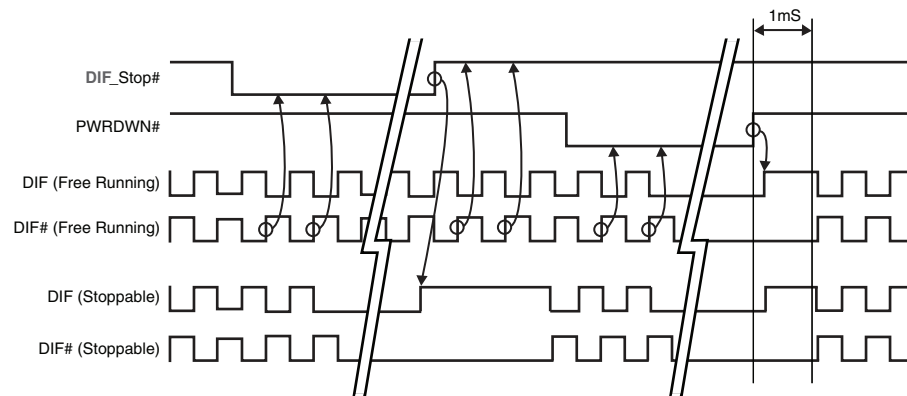
DIF_STOP_2 (DIF_Stop = Tristate, PD = Driven)



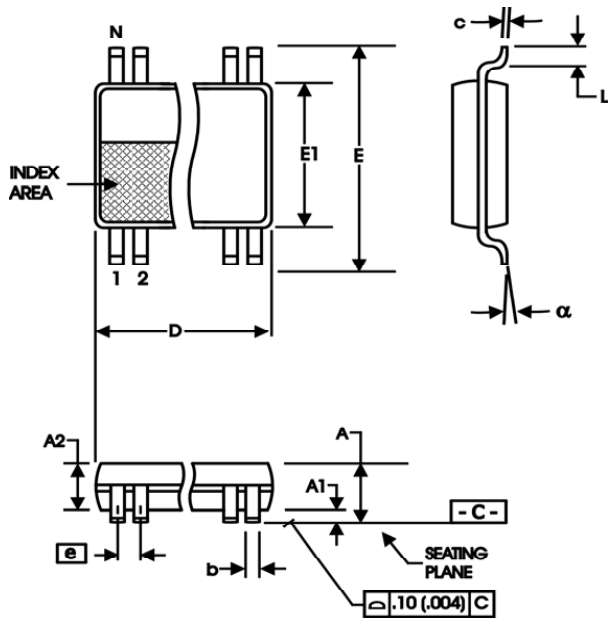
DIF_STOP_3 (DIF_Stop = Driven, PD = Tristate)



DIF_STOP_4 (DIF_Stop = Tristate, PD = Tristate)



28-pin SSOP Package Dimensions



209 mil SSOP

209 mil SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 2.00 | -- | .079 |
| A1 | 0.05 | -- | .002 | -- |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.55 | 0.95 | .022 | .037 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

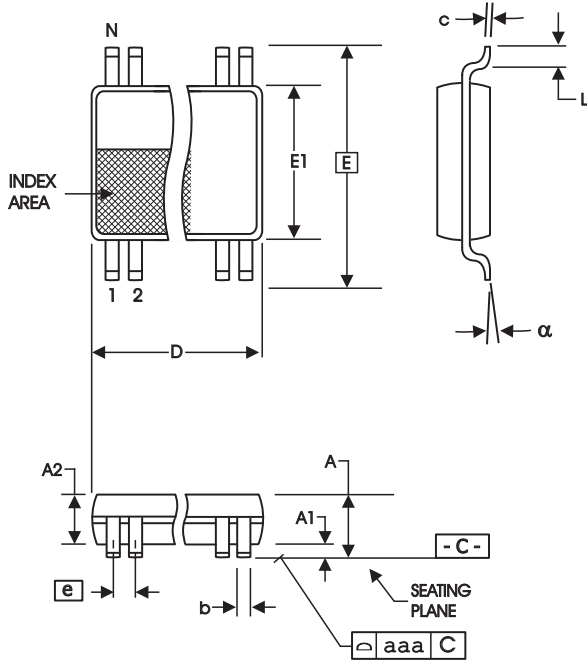
VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.90 | 10.50 | .390 | .413 |

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

28-pin TSSOP Package Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.60 | 9.80 | .378 | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

9DS400 Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Ambient Operating Temperature |
|---------------------|-------------|--------------------|--------------|-------------------------------|
| 9DS400AGLF | 9DS400AGLF | Tubes | 28-pin TSSOP | 0 to +70° C |
| 9DS400AGLFT | 9DS400AGLF | Tape and Reel | 28-pin TSSOP | 0 to +70° C |
| 9DS400AGILF | 9DS400AGILF | Tubes | 28-pin TSSOP | -40 to +85° C |
| 9DS400AGILFT | 9DS400AGILF | Tape and Reel | 28-pin TSSOP | -40 to +85° C |
| 9DS400AFLF | 9DS400AFLF | Tubes | 28-pin SSOP | 0 to +70° C |
| 9DS400AFLFT | 9DS400AFLF | Tape and Reel | 28-pin SSOP | 0 to +70° C |
| 9DS400AFILF | 9DS400AFILF | Tubes | 28-pin SSOP | -40 to +85° C |
| 9DS400AFILFT | 9DS400AFILF | Tape and Reel | 28-pin SSOP | -40 to +85° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|--------|
| 0.1 | 9/16/2009 | Initial release. | |
| 0.2 | 9/17/2009 | Updated IDD specs in Input/Supply/Common Output Parameters table | 5 |
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