

Description

The 9ZXL1232E / 9ZXL1252E are second-generation, enhanced-performance DB1200ZL differential buffers. The parts are pin-compatible upgrades to the 9ZXL1232A and 9ZXL1252A, while offering a much improved phase jitter performance and an SMBus Write Lock feature for increased system security. A fixed external feedback maintains low drift for critical QPI/UPI applications. The 9ZXL1232E and 9ZXL1252E have an SMBus Write Lockout pin for increased device and system security.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

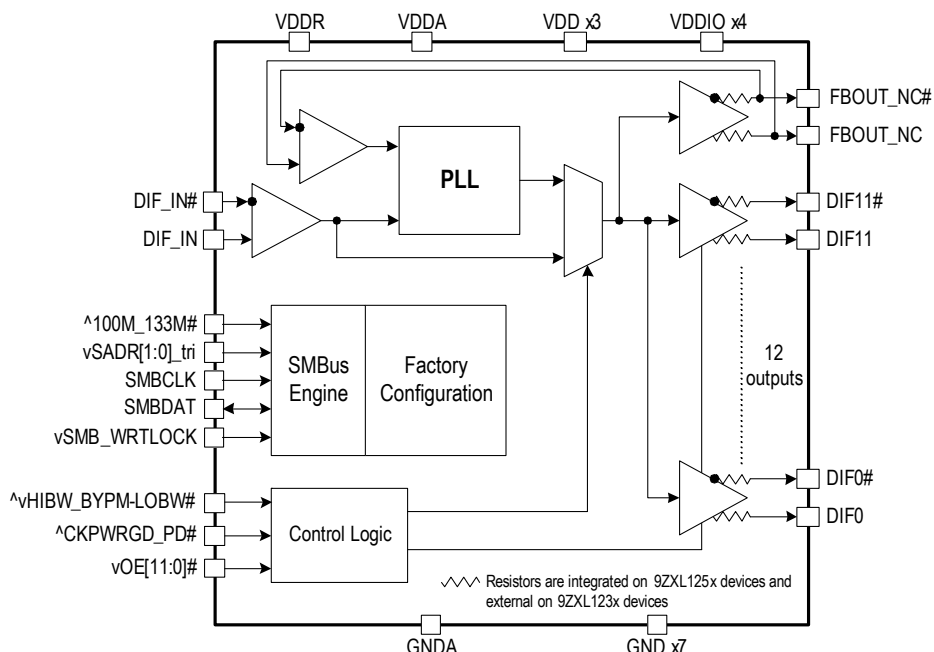
Typical Applications

- Servers
- Storage
- Networking
- SSDs

Output Features

- 12 Low-Power (LP) HCSL output pairs (1232E)
- 12 Low-Power (LP) HCSL output pairs with 85Ω Zout (1252E)

Block Diagram



Features

- SMBus write lock feature; increases system security
- LP-HCSL outputs; eliminate 24 resistors, save 41mm² of area (1232E)
- LP-HCSL outputs with 85Ω Zout; eliminate 48 resistors, save 82mm² of area (1252E)
- 12 OE# pins; hardware control of each output
- 9 selectable SMBus addresses; multiple devices can share the same SMBus segment
- Selectable PLL BW; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL bandwidth and bypass; change mode without power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- 100 and 133.33 MHz PLL mode; UPI and legacy QPI support
- 9 x 9 mm 64-QFN package; small board footprint

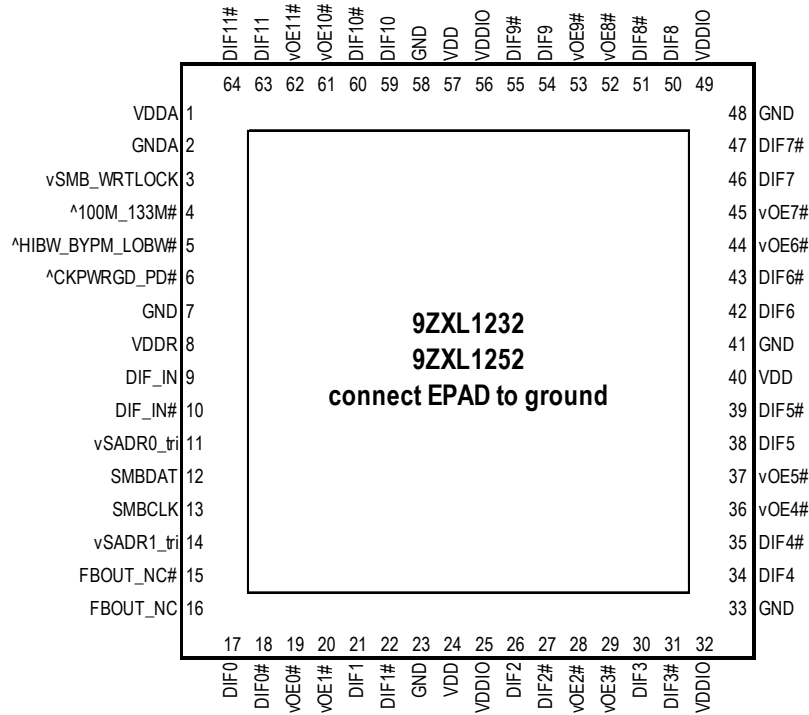
Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- Input-to-output delay: Fixed at 0ps
- Input-to-output delay variation < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: QPI/UPI ≥ 9.6GB/s < 0.2ps rms
- Phase jitter: IF-UPI < 1.0ps rms

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Pin Configuration



9 x 9 mm 64-VFQFPN

Note: Pins with ^ prefix have internal 120kohm pull-up
Pins with v prefix have internal 120kohm pull-down

Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|--------|------------------|------------|---|
| 1 | VDDA | Power | Power supply for PLL core. |
| 2 | GNDA | GND | Ground pin for the PLL core. |
| 3 | vSMB_WRTLOCK | Input | This pin prevents SMBus writes when asserted. SMBus reads are not affected. This pin has an internal 120kΩ pull-down. 0 = SMBus writes allows, 1 = SMBus writes blocked. |
| 4 | ^100M_133M# | Latched In | 3.3V input to select operating frequency. This pin has an internal 120kΩ pull-up resistor. See <i>Functionality at Power-Up</i> table for definition. |
| 5 | ^HIBW_BYPM_LOBW# | Latched In | Tri-level input to select High BW, Bypass or Low BW Mode. Has an internal 120kΩ pull-up resistor. See <i>PLL Operating Mode</i> table for details. |
| 6 | ^CKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kΩ pull-up resistor. |
| 7 | GND | GND | Ground pin. |
| 8 | VDDR | Power | Power supply for differential input clock (receiver). This V _{DD} should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. |
| 9 | DIF_IN | Input | HCSL true input. |
| 10 | DIF_IN# | Input | HCSL complementary input. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|------------|--------|---|
| 11 | vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal 120kΩ pull-down resistor. See the <i>SMBus Addressing</i> table. |
| 12 | SMBDAT | I/O | Data pin of SMBUS circuitry. |
| 13 | SMBCLK | Input | Clock pin of SMBUS circuitry. |
| 14 | vSADR1_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal 120kΩ pull-down resistor. See the <i>SMBus Addressing</i> table. |
| 15 | FBOUT_NC# | Output | Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 16 | FBOUT_NC | Output | True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay. |
| 17 | DIF0 | Output | Differential true clock output. |
| 18 | DIF0# | Output | Differential complementary clock output. |
| 19 | vOE0# | Input | Active low input for enabling output 0. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 20 | vOE1# | Input | Active low input for enabling output 1. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 21 | DIF1 | Output | Differential true clock output. |
| 22 | DIF1# | Output | Differential complementary clock output. |
| 23 | GND | GND | Ground pin. |
| 24 | VDD | Power | Power supply, nominally 3.3V. |
| 25 | VDDIO | Power | Power supply for differential outputs. |
| 26 | DIF2 | Output | Differential true clock output. |
| 27 | DIF2# | Output | Differential complementary clock output. |
| 28 | vOE2# | Input | Active low input for enabling output 2. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 29 | vOE3# | Input | Active low input for enabling output 3. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 30 | DIF3 | Output | Differential true clock output. |
| 31 | DIF3# | Output | Differential complementary clock output. |
| 32 | VDDIO | Power | Power supply for differential outputs. |
| 33 | GND | GND | Ground pin. |
| 34 | DIF4 | Output | Differential true clock output. |
| 35 | DIF4# | Output | Differential complementary clock output. |
| 36 | vOE4# | Input | Active low input for enabling output 4. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|--------|--------|---|
| 37 | vOE5# | Input | Active low input for enabling output 5. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 38 | DIF5 | Output | Differential true clock output. |
| 39 | DIF5# | Output | Differential complementary clock output. |
| 40 | VDD | Power | Power supply, nominally 3.3V. |
| 41 | GND | GND | Ground pin. |
| 42 | DIF6 | Output | Differential true clock output. |
| 43 | DIF6# | Output | Differential complementary clock output. |
| 44 | vOE6# | Input | Active low input for enabling output 6. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 45 | vOE7# | Input | Active low input for enabling output 7. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 46 | DIF7 | Output | Differential true clock output. |
| 47 | DIF7# | Output | Differential complementary clock output. |
| 48 | GND | GND | Ground pin. |
| 49 | VDDIO | Power | Power supply for differential outputs. |
| 50 | DIF8 | Output | Differential true clock output. |
| 51 | DIF8# | Output | Differential complementary clock output. |
| 52 | vOE8# | Input | Active low input for enabling output 8. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 53 | vOE9# | Input | Active low input for enabling output 9. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 54 | DIF9 | Output | Differential true clock output. |
| 55 | DIF9# | Output | Differential complementary clock output. |
| 56 | VDDIO | Power | Power supply for differential outputs. |
| 57 | VDD | Power | Power supply, nominally 3.3V. |
| 58 | GND | GND | Ground pin. |
| 59 | DIF10 | Output | Differential true clock output. |
| 60 | DIF10# | Output | Differential complementary clock output. |
| 61 | vOE10# | Input | Active low input for enabling output 10. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 62 | vOE11# | Input | Active low input for enabling output 11. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs. |
| 63 | DIF11 | Output | Differential true clock output. |
| 64 | DIF11# | Output | Differential complementary clock output. |
| 65 | EPAD | GND | Connect EPAD to ground. |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1232E / 9ZXL1252E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|--------------------|----------------------------|---------|---------|----------------------|-------|-------|
| Supply Voltage | VDDx | | | | 3.9 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins. | | | 3.9 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD Protection | ESD prot | Human Body Model. | 2500 | | | V | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

³ Not to exceed 3.9V.

Electrical Characteristics

T_A = T_{AMB}. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 3. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---------------------------|---------------------|---|---------|---------|---------------------|-------|-------|
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | |
| SMBus Output Low Voltage | V _{OLSMB} | At I _{PULLUP} . | | | 0.4 | V | |
| SMBus Sink Current | I _{PULLUP} | At V _{OL} . | 4 | | | mA | |
| Nominal Bus Voltage | V _{DD} SMB | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15V) to (Min V _{IH} + 0.15V). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15V) to (Max V _{IL} - 0.15V). | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{SMB} | SMBus operating frequency. | | | 400 | kHz | 5 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 4. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|----------------------------------|-------------|---|---------|---------|---------|---------|-------|
| Input Crossover Voltage – DIF_IN | V_{CROSS} | Cross over voltage. | 150 | | 900 | mV | 1 |
| Input Swing – DIF_IN | V_{SWING} | Differential value. | 300 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{DD}$, $V_{IN} = GND$. | -5 | | 5 | μA | |
| Input Duty Cycle | d_{tin} | Measurement from differential waveform. | 45 | | 55 | % | 1 |
| Input Jitter – Cycle to Cycle | J_{DIFIn} | Differential measurement. | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through $\pm 75mV$ window centered around differential zero.

Table 5. Input/Supply/Common Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|-------------------------------|-----------------|--|-------------|------------|----------------|-------------|-------|
| Supply Voltage | V_{DDX} | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| Output Supply Voltage | V_{DDIO} | Supply voltage for DIF outputs, if present. | 0.95 | 1.05 | 3.465 | V | |
| Ambient Operating Temperature | T_{AMB} | Commercial range (T_{COM}). | 0 | | 70 | $^{\circ}C$ | |
| | | Industrial range (T_{IND}). | -40 | 25 | 85 | $^{\circ}C$ | |
| Input High Voltage | V_{IH} | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD} + 0.3$ | V | |
| Input Low Voltage | V_{IL} | Single-ended inputs, except SMBus, tri-level inputs. | $GND - 0.3$ | | 0.8 | V | |
| Input High Voltage | V_{IH} | Tri-level inputs. | 2.2 | | $V_{DD} + 0.3$ | V | |
| Input Mid Voltage | V_{IL} | Tri-level inputs. | 1.2 | $V_{DD}/2$ | 1.8 | V | |
| Input Low Voltage | V_{IL} | Tri-level inputs. | $GND - 0.3$ | | 0.8 | V | |
| Input Current | I_{IN} | Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$. | -5 | | 5 | μA | |
| | I_{INP} | Single-ended inputs. $V_{IN} = 0V$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors. | -50 | | 50 | μA | |
| Input Frequency | F_{ibyp} | $V_{DD} = 3.3V$, Bypass Mode. | 1 | | 400 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3V$, 100MHz PLL Mode. | 98.5 | 100.00 | 102.5 | MHz | |
| | F_{ipll} | $V_{DD} = 3.3V$, 133.33MHz PLL Mode. | 132 | 133.33 | 135 | MHz | |
| Pin Inductance | L_{pin} | | | | 7 | nH | 1 |
| Capacitance | C_{IN} | Logic inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | C_{INDIF_IN} | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | C_{OUT} | Output pin capacitance. | | | 6 | pF | 1 |

Table 5. Input/Supply/Common Parameters (Cont.)

 T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------------------|-----------------|--|---------|---------|---------|---------|-------|
| Clk Stabilization | T_{STAB} | From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock. | | 1 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications (Triangular modulation). | 30 | | 33 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | t_{DRVPD} | DIF output enable after PD# deassertion. | | 49 | 300 | μ s | 1,3 |
| Tfall | t_F | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | t_R | Rise time of control inputs. | | | 5 | ns | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

Table 6. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|--------------------------|-------------|--|---------|---------|---------|-------|-------|
| Operating Supply Current | I_{DDA} | V_{DDA} , PLL Mode at 100MHz. | | 38 | 46 | mA | 1 |
| | I_{DD} | All other V_{DD} pins. | | 25 | 34 | mA | |
| | I_{DDIO} | V_{DDIO} for LP-HCSL outputs, if applicable. | | 83 | 107 | mA | |
| Power Down Current | I_{DDAPD} | V_{DDA} , CKPWRGD_PD# = 0. | | 3.3 | 4 | mA | 1 |
| | I_{DDPD} | All other V_{DD} pins, CKPWRGD_PD# = 0. | | 1.3 | 2 | mA | |

¹ Includes V_{DDR} if applicable.

Table 7. Skew and Differential Jitter Parameters

 T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------|-----------------|---|---------|---------|---------|-------|-----------|
| CLK_IN, DIF[x:0] | t_{SPO_PLL} | Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage. | -100 | -21.3 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t_{PD_BYP} | Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage. | 2 | 2.6 | 3 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DSPO_PLL} | Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature. | -50 | 0.0 | 50 | ps | 1,2,3,5,8 |

Table 7. Skew and Differential Jitter Parameters (Cont.)

 T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|------------------------|-----------------|--|---------|---------|---------|----------|-----------|
| CLK_IN, DIF[x:0] | t_{DSPO_BYP} | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, $T_{AMB} = 0$ to $70^{\circ}C$. | -250 | | 250 | ps | 1,2,3,5,8 |
| | | Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, $T_{AMB} = -40$ to $+85^{\circ}C$. | -350 | | 350 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DTE} | Random differential tracking error between two 9ZX devices in High BW Mode. | | 3 | 5 | ps (rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t_{DSSTE} | Random differential spread spectrum tracking error between two 9ZX devices in High BW Mode. | | 23 | 50 | ps | 1,2,3,5,8 |
| DIF[x:0] | t_{SKEW_ALL} | Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz. | | | 50 | ps | 1,2,3,8 |
| PLL Jitter Peaking | $j_{peak-hibw}$ | LOBW#_BYPASS_HIBW = 1. | 0 | 1.3 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | LOBW#_BYPASS_HIBW = 0. | 0 | 1.3 | 2 | dB | 7,8 |
| PLL Bandwidth | pll_{HIBW} | LOBW#_BYPASS_HIBW = 1. | 2 | 2.6 | 4 | MHz | 8,9 |
| PLL Bandwidth | pll_{LOBW} | LOBW#_BYPASS_HIBW = 0. | 0.7 | 1.0 | 1.4 | MHz | 8,9 |
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode. | 45 | 50.3 | 55 | % | 1 |
| Duty Cycle Distortion | t_{DCD} | Measured differentially, Bypass Mode at 100MHz. | -1 | 0 | 1 | % | 1,10 |
| Jitter, Cycle to Cycle | $t_{jyc-cyc}$ | PLL Mode. | | 14 | 50 | ps | 1,11 |
| | | Additive jitter in Bypass Mode. | | 0.1 | 5 | ps | 1,11 |

¹ Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

³ All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

⁴ This parameter is deterministic for a given device.

⁵ Measured with scope averaging on to find mean value.

⁶ "t" is the period of the input clock.

⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

⁸ Guaranteed by design and characterization, not 100% tested in production.

⁹ Measured at 3db down or half power point.

¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

¹¹ Measured from differential waveform.

Table 8. HCSSLP-HCSSL Outputs

 T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------|------------------|--|---------|---------|---------|----------------------|-------|-------|
| Slew Rate | dV/dt | Scope averaging on. | 2 | 2.9 | 4 | 1–4 | V/ns | 1,2,3 |
| Slew Rate Matching | Δ dV/dt | Single-ended measurement. | | 7.1 | 20 | 20 | % | 1,4,7 |
| Maximum Voltage | Vmax | Measurement on single-ended signal using absolute value (scope averaging off). | 660 | 792 | 850 | 1150 | mV | 7 |
| Minimum Voltage | Vmin | | -150 | -35 | 150 | -300 | | 7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 250 | 372 | 550 | 250–550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ -Vcross | Scope averaging off. | | 15 | 140 | 140 | mV | 1,6,7 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a \pm 150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a \pm 75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ -Vcross to be smaller than Vcross absolute.

⁷ At default SMBus settings.

Table 9. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------|--------------------|--|---------|---------|---------|----------------------|----------|-------|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen 1. | | 13.4 | 30 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Low Band. 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.2 | 0.7 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band. 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 1.0 | 1.5 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.2 | 0.4 | 1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.2 | 0.4 | 0.5 | ps (rms) | 1,2 |

Table 9. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures (Cont.)

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------------------|--------------------|--|---------|---------|---------|----------------------|----------|---------|
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen 1. | | 0.01 | 0.06 | Not Applicable | ps (p-p) | 1,2,3,4 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Low Band. 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.01 | 0.06 | | ps (rms) | 1,2,3,4 |
| | | PCIe Gen 2 High Band. 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz). | | 0.01 | 0.06 | | ps (rms) | 1,2,3,4 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.01 | 0.06 | | ps (rms) | 1,2,3,4 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz). | | 0.01 | 0.06 | | ps (rms) | 1,2,3,4 |

Table 10. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|----------------------|---|---------|---------|---------|-----------------|----------|-------|
| Phase Jitter, PLL Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2. (PLL BW of 16MHz, CDR = 5MHz). | | 0.9 | 1.1 | 2 | ps (rms) | 1,2,5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3. (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.6 | 0.65 | 0.7 | ps (rms) | 1,2,5 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2. (PLL BW of 16MHz, CDR = 5MHz). | | 0.01 | 0.05 | Not applicable | ps (rms) | 2,4,5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3. (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.01 | 0.05 | | ps (rms) | 2,4,5 |

Notes for PCIe Filtered Phase Jitter tables (CC) and (IR).

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Calculated from Intel-supplied clock jitter tool when driven by 9SQL495x or equivalent with spread on and off.

³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12} .

⁴ For RMS values, additive jitter is calculated by solving for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

⁵ IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Table 11. Filtered Phase Jitter Parameters – QPI/UPI

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|------------------------------------|-------------------------|--|---------|-------------|-------------|----------------------|-------------|-------|
| Phase Jitter, PLL Mode | t _{jphQPI_UPI} | QPI & UPI. (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI). | | 0.14 | 0.3 | 0.5 | ps (rms) | 1,2 |
| | | QPI & UPI. (100MHz, 8.0Gb/s, 12UI). | | 0.07 | 0.13 | 0.3 | | 1,2 |
| | | QPI & UPI. (100MHz, ≥ 9.6Gb/s, 12UI). | | 0.06 | 0.1 | 0.2 | | 1,2 |
| | t _{jphIF_UPI} | IF-UPI. | | 0.1 0.17 | 0.14 0.2 | 1 | | 1,4,5 |
| Additive Phase Jitter, Bypass Mode | t _{jphQPI_UPI} | QPI & UPI. (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI). | | 0.00 | 0.01 | Not applicable | ps (rms) | 1,2,3 |
| | | QPI & UPI. (100MHz, 8.0Gb/s, 12UI). | | 0.00 | 0.01 | | | 1,2,3 |
| | | QPI & UPI. (100MHz, ≥ 9.6Gb/s, 12UI). | | 0.00 | 0.01 | | | 1,2,3 |
| | t _{jphIF_UPI} | IF-UPI. | | 0.06 | 0.07 | | | 1,4 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Calculated from Intel-supplied clock jitter tool, when driven by 9SQL495x or equivalent with spread on and off.

³ For RMS values, additive jitter is calculated by solving for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

⁴ Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

⁵ Top number is when the buffer is in Low BW mode, bottom number is when the buffer is in High BW mode.

Table 12. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|------------------------------------|---------------------------|-------------------------------|---------|---------|---------|-----------------|-------------|-------|
| Phase Jitter, PLL Mode | t _{jph12k-20MHi} | PLL High BW, SSC Off, 100MHz. | | 171 | 225 | Not applicable | fs (rms) | 1,2 |
| Phase Jitter, PLL Mode | t _{jph12k-20MLo} | PLL Low BW, SSC Off, 100MHz. | | 184 | 225 | | fs (rms) | 1,2 |
| Additive Phase Jitter, Bypass Mode | t _{jph12k-20MBy} | Bypass Mode, SSC Off, 100MHz. | | 107 | 125 | | fs (rms) | 1,2,3 |

¹ Applies to all outputs when driven by Wenzel clock source.

² 12kHz to 20MHz brick wall filter.

³ For RMS values, additive jitter is calculated by solving for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and “c” is rms total jitter.

Clock Periods

Table 13. Clock Periods – Differential Outputs with Spread Spectrum Disabled

| SSC On | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|--------|----------------------|---------------------------|---------------------------------|--------------------------------|----------------------|--------------------------------|---------------------------------|---------------------------|-------|-------|
| | | 1 Clock | 1 μ s | 0.1s | 0.1s | 0.1s | 1 μ s | 1 Clock | | |
| | | -c2cjitter AbsPer Minimum | -SSC Short-Term Average Minimum | -ppm Long-Term Average Minimum | 0 ppm Period Nominal | +ppm Long-Term Average Maximum | +SSC Short-Term Average Maximum | +c2cjitter AbsPer Maximum | | |
| DIF | 100.00 | 9.94900 | — | 9.99900 | 10.00000 | 10.00100 | — | 10.05100 | ns | 1,2,3 |
| | 133.33 | 7.44925 | — | 7.49925 | 7.50000 | 7.50075 | — | 7.55075 | ns | 1,2,4 |

Table 14. Clock Periods – Differential Outputs with Spread Spectrum Enabled

| SSC On | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|--------|----------------------|---------------------------|---------------------------------|--------------------------------|----------------------|--------------------------------|---------------------------------|---------------------------|-------|-------|
| | | 1 Clock | 1 μ s | 0.1s | 0.1s | 0.1s | 1 μ s | 1 Clock | | |
| | | -c2cjitter AbsPer Minimum | -SSC Short-Term Average Minimum | -ppm Long-Term Average Minimum | 0 ppm Period Nominal | +ppm Long-Term Average Maximum | +SSC Short-Term Average Maximum | +c2cjitter AbsPer Maximum | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (± 100 ppm). The buffer itself does not contribute to ppm error.

³ Driven by SRC output of main clock, 100MHz PLL Mode or Bypass Mode.

⁴ Driven by CPU output of main clock, 133MHz PLL Mode or Bypass Mode.

Power Management

| CKPWRGD_PD# | DIF_IN | SMBus EN bit | OE[x]# | DIF[x] | PLL State if not in Bypass Mode |
|-------------|---------|--------------|--------|---------|---------------------------------|
| 0 | X | X | X | Low/Low | Off |
| 1 | Running | 0 | 0 | Low/Low | On |
| | | 0 | 1 | Low/Low | On |
| | | 1 | 0 | Running | On |
| | | 1 | 1 | Low/Low | On |

Power Connections

| Pin Number | | | Description |
|-----------------|-------------------|--------------------|--------------|
| V _{DD} | V _{DDIO} | GND | |
| 1 | | 2 | Analog PLL |
| 8 | | 7 | Analog input |
| 24,40,57 | 25,32,49,56 | 23,33,41,48, 58,65 | DIF clocks |

Functionality at Power-Up (PLL Mode)

| 100M_133M# | DIF_IN MHz | DIF[x] |
|------------|------------|--------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

PLL Operating Mode Readback

| HIBW_BYPM_LOBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW) | 0 | 0 |
| Mid (Bypass) | 0 | 1 |
| High (High BW) | 1 | 1 |

PLL Operating Mode

| HIBW_BYPM_LOBW# | Mode |
|-----------------|-------------|
| Low | PLL Low BW |
| Mid | Bypass |
| High | PLL High BW |

Note: PLL is OFF in Bypass Mode.

SMBus Addressing

| SMB_A1_tri | SMB_A0_tri | SMBus Address |
|------------|------------|---------------|
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)

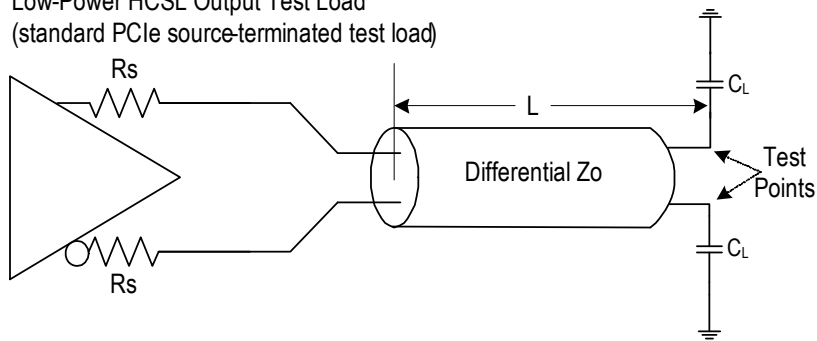


Table 15. Parameters for Low-Power HCSL Output Test Load

| Device | Rs (Ω) | Zo (Ω) | L (inches) | CL (pF) |
|-----------|-----------------|-----------------|------------|---------|
| 9ZXL123x | 27 | 85 | 10 | 2 |
| | 33 | 100 | 10 | 2 |
| 9ZXL125x* | Internal | 85 | 10 | 2 |
| | 7.5 | 100 | 10 | 2 |

* Contact factory for versions of this device with Zo = 100 Ω .

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT’s “Universal” Low-Power HCSL Outputs”](#) for termination schemes for LVPECL, LVDS, CML and SSTL.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | |
| | X Byte | ACK |
| O | | O |
| O | | O |
| O | | O |
| | | O |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| | | ACK |
| | | Beginning Byte N |
| | X Byte | O |
| | | O |
| | | O |
| | | O |
| | | O |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: PLL Mode and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|------------|------------------------------|------|---------------------------------------|---------------|---------|
| Bit 7 | 5 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback table | | Latch |
| Bit 6 | 5 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | | | Latch |
| Bit 5 | Reserved | | | | | | 0 |
| Bit 4 | Reserved | | | | | | 0 |
| Bit 3 | — | PLL_SW_EN | Enable S/W control of PLL BW | RW | HW Latch | SMBus Control | 0 |
| Bit 2 | — | PLL Mode 1 | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 1 |
| Bit 1 | — | PLL Mode 0 | PLL Operating Mode 1 | RW | | | 1 |
| Bit 0 | 4 | 100M_133M# | Frequency Select Readback | R | 133MHz | 100MHz | Latch |

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. Use the values from the *PLL Operating Mode Readback* table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. If these bits are changed, a warm reset of the system must be completed.

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---------|-----------------|---------|
| Bit 7 | 47/46 | DIF_7_En | Output Enable | RW | Low/Low | OE# Pin Control | 1 |
| Bit 6 | 43/42 | DIF_6_En | Output Enable | RW | | | 1 |
| Bit 5 | 39/38 | DIF_5_En | Output Enable | RW | | | 1 |
| Bit 4 | 35/34 | DIF_4_En | Output Enable | RW | | | 1 |
| Bit 3 | 30/31 | DIF_3_En | Output Enable | RW | | | 1 |
| Bit 2 | 26/27 | DIF_2_En | Output Enable | RW | | | 1 |
| Bit 1 | 21/22 | DIF_1_En | Output Enable | RW | | | 1 |
| Bit 0 | 17/18 | DIF_0_En | Output Enable | RW | | | 1 |

SMBus Table: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|-----------|------------------|------|---------|-----------------|---------|
| Bit 7 | Reserved | | | | | | 0 |
| Bit 6 | Reserved | | | | | | 0 |
| Bit 5 | Reserved | | | | | | 0 |
| Bit 4 | Reserved | | | | | | 0 |
| Bit 3 | 64/63 | DIF_11_En | Output Enable | RW | Low/Low | OE# Pin Control | 1 |
| Bit 2 | 59/60 | DIF_10_En | Output Enable | RW | | | 1 |
| Bit 1 | 54/55 | DIF_9_En | Output Enable | RW | | | 1 |
| Bit 0 | 50/51 | DIF_8_En | Output Enable | RW | | | 1 |

SMBus Table: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBus Table: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBus Table: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|--------------|---|---------|
| Bit 7 | — | RID3 | REVISION ID | R | E rev = 0100 | | 0 |
| Bit 6 | — | RID2 | | R | | | 1 |
| Bit 5 | — | RID1 | | R | | | 0 |
| Bit 4 | — | RID0 | | R | | | 0 |
| Bit 3 | — | VID3 | VENDOR ID | R | — | — | 0 |
| Bit 2 | — | VID2 | | R | — | — | 0 |
| Bit 1 | — | VID1 | | R | — | — | 0 |
| Bit 0 | — | VID0 | | R | — | — | 1 |

SMBus Table: Device ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------------|------------------|------|----------------------------------|---|---------|
| Bit 7 | — | Device ID 7 (MSB) | | R | 9ZXL1232E: E8h 9ZXL1252E: F8h | | 1 |
| Bit 6 | — | Device ID 6 | | R | | | 1 |
| Bit 5 | — | Device ID 5 | | R | | | 1 |
| Bit 4 | — | Device ID 4 | | R | | | x |
| Bit 3 | — | Device ID 3 | | R | | | x |
| Bit 2 | — | Device ID 2 | | R | | | x |
| Bit 1 | — | Device ID 1 | | R | | | x |
| Bit 0 | — | Device ID 0 | | R | | | x |

SMBus Table: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|------|---|------|---|---|---------|
| Bit 7 | Reserved | | | | | | 0 |
| Bit 6 | Reserved | | | | | | 0 |
| Bit 5 | Reserved | | | | | | 0 |
| Bit 4 | — | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | — | BC3 | | RW | | | 1 |
| Bit 2 | — | BC2 | | RW | | | 0 |
| Bit 1 | — | BC1 | | RW | | | 0 |
| Bit 0 | — | BC0 | | RW | | | 0 |

SMBus Table: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|------|------------------|------|---|---|---------|
| Bit 7 | Reserved | | | | | | 0 |
| Bit 6 | Reserved | | | | | | 0 |
| Bit 5 | Reserved | | | | | | 0 |
| Bit 4 | Reserved | | | | | | 0 |
| Bit 3 | Reserved | | | | | | 0 |
| Bit 2 | Reserved | | | | | | 0 |
| Bit 1 | Reserved | | | | | | 0 |
| Bit 0 | Reserved | | | | | | 0 |

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/64-vfqfpn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-615-x-615-mm-nlg64p2

Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature |
|-----------------------|---------------------------------|--|---------------|
| 9ZXL1232EKILF | 9 x 9 mm, 0.5mm pitch 64-VFQFPN | Tray | -40° to +85°C |
| 9ZXL1232EKILFT | 9 x 9 mm, 0.5mm pitch 64-VFQFPN | Tape and Reel, Pin 1 Orientation: EIA-481C | -40° to +85°C |
| 9ZXL1252EKILF | 9 x 9 mm, 0.5mm pitch 64-VFQFPN | Tray | -40° to +85°C |
| 9ZXL1252EKILFT | 9 x 9 mm, 0.5mm pitch 64-VFQFPN | Tape and Reel, Pin 1 Orientation: EIA-481C | -40° to +85°C |

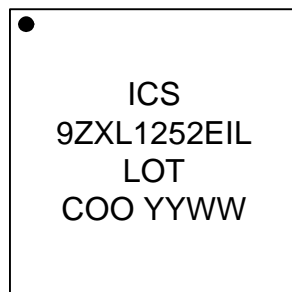
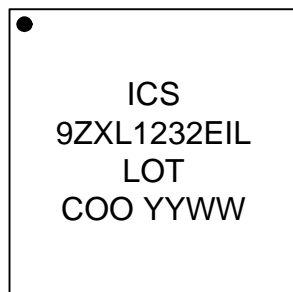
“LF” designates PB-free configuration, RoHS compliant.

“E” is the device revision designator (will not correlate with the datasheet revision).

Table 16. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|--------------|
| T | Quadrant 1 (EIA-481-C) | |

Marking Diagrams



1. “I” denotes industrial temperature range
2. “L” denotes RoHS compliant package.
3. “LOT” denotes the lot number.
4. “COO” denotes country of origin.
5. “YYWW” denotes the last two digits of the year and week the part was assembled.

Revision History

| Revision Date | Description of Change |
|--------------------|--|
| November 30, 2018 | Updated tPD_BYP minimum and maximum values to 2 and 3, respectively. |
| August 14, 2018 | Updated block diagram. |
| April 17, 2018 | Updated absolute maximum supply voltage rating and VIHSMB to 3.9V. |
| December 1, 2017 | Removed "5V tolerant" reference in pins 12 and 13 descriptions. |
| September 29, 2017 | Initial release. |



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