**General Description**

The 83947I-147 is a low skew, 1-to-9 LVCMOS/LVTTL Fanout Buffer. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 9 to 18 by utilizing the ability of the outputs to drive two series terminated lines.

Guaranteed output and part-to-part skew characteristics make the 83947I-147 ideal for high performance, 3.3V or 2.5V single ended applications.

**Features**

- Nine LVCMOS/LVTTL outputs
- Selectable CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 250MHz
- Output skew: 115ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Additive phase jitter, RMS: 0.02ps (typical) @ 3.3V
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

**Block Diagram**

![Block Diagram of 83947I-147]

**Pin Assignment**

![Pin Assignment Diagram of 83947I-147]

ICS83947I-147
32-Lead LQFP
7mm x 7mm x 1.4mm package body
Top View
### Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>2</td>
<td>CLK_SEL</td>
<td>Input</td>
<td>Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LVCMOS / LVTTL interface levels.</td>
</tr>
<tr>
<td>3, 4</td>
<td>CLK0, CLK1</td>
<td>Input</td>
<td>Reference clock inputs. LVCMOS / LVTTL interface levels.</td>
</tr>
<tr>
<td>5</td>
<td>CLK_EN</td>
<td>Input</td>
<td>Clock enable. LVCMOS / LVTTL interface levels.</td>
</tr>
<tr>
<td>6</td>
<td>OE</td>
<td>Input</td>
<td>Output enable. LVCMOS / LVTTL interface levels.</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>Power</td>
<td>Core supply pin.</td>
</tr>
<tr>
<td>10, 14, 18, 22, 27, 31</td>
<td>V_DDO</td>
<td>Power</td>
<td>Output supply pins.</td>
</tr>
<tr>
<td>11, 13, 15, 19, 21, 23, 26, 28, 30</td>
<td>Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0</td>
<td>Output</td>
<td>Q0 thru Q8 clock outputs. LVCMOS / LVTTL interface levels.</td>
</tr>
</tbody>
</table>

**NOTE:** Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_PD</td>
<td>Power Dissipation Capacitance</td>
<td>(per output)</td>
<td></td>
<td></td>
<td>12</td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td></td>
<td>51</td>
<td></td>
<td>KΩ</td>
</tr>
<tr>
<td>R_OUT</td>
<td>Output Impedance</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

### Table 3. Output Enable and Clock Enable Function Table

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE</td>
<td>CLK_EN</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$ OR $2.5V \pm 5\%$, $TA = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Input Supply Current</td>
<td></td>
<td></td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td></td>
<td></td>
<td>9</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$ | 4.6V |
Inputs, $V_i$ | -0.5V to $V_{DD} + 0.5V$ |
Outputs, $V_o$ | -0.5V to $V_{DDO} + 0.5V$ |
Package Thermal Impedance, $\theta_{ja}$ | 47.9°C/W (0 Ifpm) |
Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $TA = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>CLK0, CLK1, OE, CLK_SEL, CLK_EN</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current</td>
<td></td>
<td>-100</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$I_{OH} = -20mA$</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$I_{OL} = 20mA$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, 3.3V Output Load Test Circuit Diagram.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $TA = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>CLK0, CLK1, CLK_SEL, CLK_EN</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input High Current</td>
<td></td>
<td>&amp; -0.3</td>
<td>1.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td></td>
<td>&amp; -0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td></td>
<td>$V_{DD} = V_{IN} = 2.625V$</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Input Low Current</td>
<td></td>
<td>$V_{DD} = 32.625V$, $V_{IN} = 0V$</td>
<td>&amp; -150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{DD} = 3.3V$, $V_{IN} = 0V$</td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, 2.5V Output Load Test Circuit Diagram.
### TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V ± 0.3V$, $TA = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td></td>
<td></td>
<td>250</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay, NOTE 1</td>
<td>$f \leq 250$ MHZ</td>
<td>2</td>
<td>4.2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 5</td>
<td>Measured on rising edge @ $V_{DDO}/2$</td>
<td></td>
<td>115</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(pp)}$</td>
<td>Part-to-Part Skew; NOTE 3, 5</td>
<td>Measured on rising edge @ $V_{DDO}/2$</td>
<td></td>
<td>500</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{jit(O)}$</td>
<td>Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section</td>
<td>(12KHz to 20MHz)</td>
<td></td>
<td>0.2</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{p} / t_{f}$</td>
<td>Output Rise/Fall Time</td>
<td>0.8V to 2.0V</td>
<td>0.2</td>
<td>1</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PW}$</td>
<td>Output Pulse Width</td>
<td>$f &gt; 133$ MHz</td>
<td>$t_{Period}/2 - 1$</td>
<td>$t_{Period}/2 + 1$</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dc}$</td>
<td>Output Duty Cycle</td>
<td>$f \leq 133$ MHz</td>
<td>40</td>
<td>60</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Output Enable Time; NOTE 4</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Output Disable Time; NOTE 4</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{S}$</td>
<td>Clock Enable Setup Time</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H}$</td>
<td>Clock Enable Hold Time</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

All parameters measured at frequencies less than or equal to 250MHz unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

### TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V ± 5\%$, $TA = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td></td>
<td></td>
<td>250</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay, NOTE 1</td>
<td>$f \leq 250$ MHZ</td>
<td>2.4</td>
<td>4.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 5</td>
<td>Measured on rising edge @ $V_{DDO}/2$</td>
<td></td>
<td>130</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(pp)}$</td>
<td>Part-to-Part Skew; NOTE 3, 5</td>
<td>Measured on rising edge @ $V_{DDO}/2$</td>
<td></td>
<td>600</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{jit(O)}$</td>
<td>Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section</td>
<td>(12KHz to 20MHz)</td>
<td></td>
<td>0.1</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{p} / t_{f}$</td>
<td>Output Rise/Fall Time</td>
<td>20% - 80%</td>
<td>300</td>
<td>800</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{PW}$</td>
<td>Output Pulse Width</td>
<td>$t_{Period}/2 - 1.2$</td>
<td>$t_{Period}/2 + 1.2$</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>OutputEnable Time; NOTE 4</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Output Disable Time; NOTE 4</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{S}$</td>
<td>Clock Enable Setup Time</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H}$</td>
<td>Clock Enable Hold Time</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

All parameters measured at frequencies less than or equal to 250MHz unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the dBc Phase Noise. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a dBc value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.
PARAMETER MEASUREMENT INFORMATION

3.3V OUTPUT LOAD AC TEST CIRCUIT

2.5V OUTPUT LOAD AC TEST CIRCUIT

PART-TO-PART SKEW

OUTPUT SKEW

PROPAGATION DELAY

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

3.3V OUTPUT RISE/FALL TIME

2.5V OUTPUT RISE/FALL TIME
APPLICATION SCHEMATIC EXAMPLE

Figure 1 shows an example of 83947I-147 application schematic. In this example, the device is operated at $V_{CC}=3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVCMOS driver.

For the LVCMOS output drivers, only one termination example is shown in this schematic. Additional termination approaches are shown in the LVCMOS Termination Application Note (refer to ICS website).

**Figure 1. 83947I-147 Schematic Layout**
RELIABILITY INFORMATION

TABLE 6. $\theta_{JA}$ vs. AIR FLOW TABLE FOR 32 LEAD LQFP

<table>
<thead>
<tr>
<th>$\theta_{JA}$ by Velocity (Linear Feet per Minute)</th>
<th>0</th>
<th>200</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-Layer PCB, JEDEC Standard Test Boards</td>
<td>67.8°C/W</td>
<td>55.9°C/W</td>
<td>50.1°C/W</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>47.9°C/W</td>
<td>42.1°C/W</td>
<td>39.4°C/W</td>
</tr>
</tbody>
</table>

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 83947I-147 is: 1040
TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION
ALL DIMENSIONS IN MILLIMETERS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>BBA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MINIMUM</td>
</tr>
<tr>
<td>N</td>
<td>32</td>
</tr>
<tr>
<td>A</td>
<td>--</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
</tr>
<tr>
<td>b</td>
<td>0.30</td>
</tr>
<tr>
<td>c</td>
<td>0.09</td>
</tr>
<tr>
<td>D</td>
<td>9.00 BASIC</td>
</tr>
<tr>
<td>D1</td>
<td>7.00 BASIC</td>
</tr>
<tr>
<td>D2</td>
<td>5.60 Ref.</td>
</tr>
<tr>
<td>E</td>
<td>9.00 BASIC</td>
</tr>
<tr>
<td>E1</td>
<td>7.00 BASIC</td>
</tr>
<tr>
<td>E2</td>
<td>5.60 Ref.</td>
</tr>
<tr>
<td>e</td>
<td>0.80 BASIC</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
</tr>
<tr>
<td>ccc</td>
<td>--</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MS-026
<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>83947AYI-147LF</td>
<td>ICS947AI147L</td>
<td>Lead-Free, 32 Lead LQFP</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>83947AYI-147LFT</td>
<td>ICS947AI147L</td>
<td>Lead-Free, 32 Lead LQFP</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
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</tbody>
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### REVISION HISTORY SHEET

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>T8</td>
<td>10</td>
<td>Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.</td>
<td>8/12/10</td>
</tr>
<tr>
<td>A</td>
<td>T8</td>
<td>10</td>
<td>Ordering Information Table - added lead-free ordering information. Deleted non-lead-free ordering information. Deleted tape &amp; reel count.</td>
<td>2/27/13</td>
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<tr>
<td>A</td>
<td></td>
<td></td>
<td>Removed ICS from part numbers where needed. Updated header and footer.</td>
<td>3/18/16</td>
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