General Description

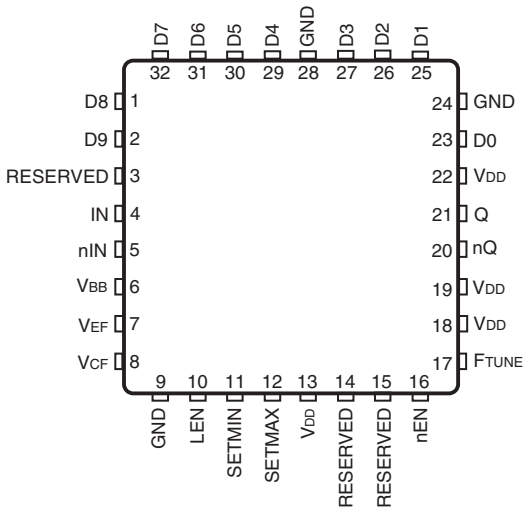
The ICS854S296I-33 is a high performance LVDS Programmable Delay Line. The delay can vary from 2.2ns to 12.5ns in 10ps steps. The ICS854S296I-33 is characterized to operate from a 3.3V power supply and is guaranteed over industrial temperature range.

The delay of the device varies in discrete steps based on a control word. A 10-bit long control word sets the delay in 10ps increments. Also, the input pins IN and nIN default to an equivalent low state when left floating. The control register can accept CMOS or TTL level signals.

Features

- One LVDS level output
- One differential clock input pair
- Differential input clock (IN, nIN) can accept the following signaling levels: LVPECL, LVDS, CML
- Maximum frequency: 1.2GHz
- Programmable Delay Range: 2.2ns to 12.5ns in 10ps steps
- D[9:0] can accept LVPECL, LVCMOS or LVTTL levels
- Full 3.3V supply voltages
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

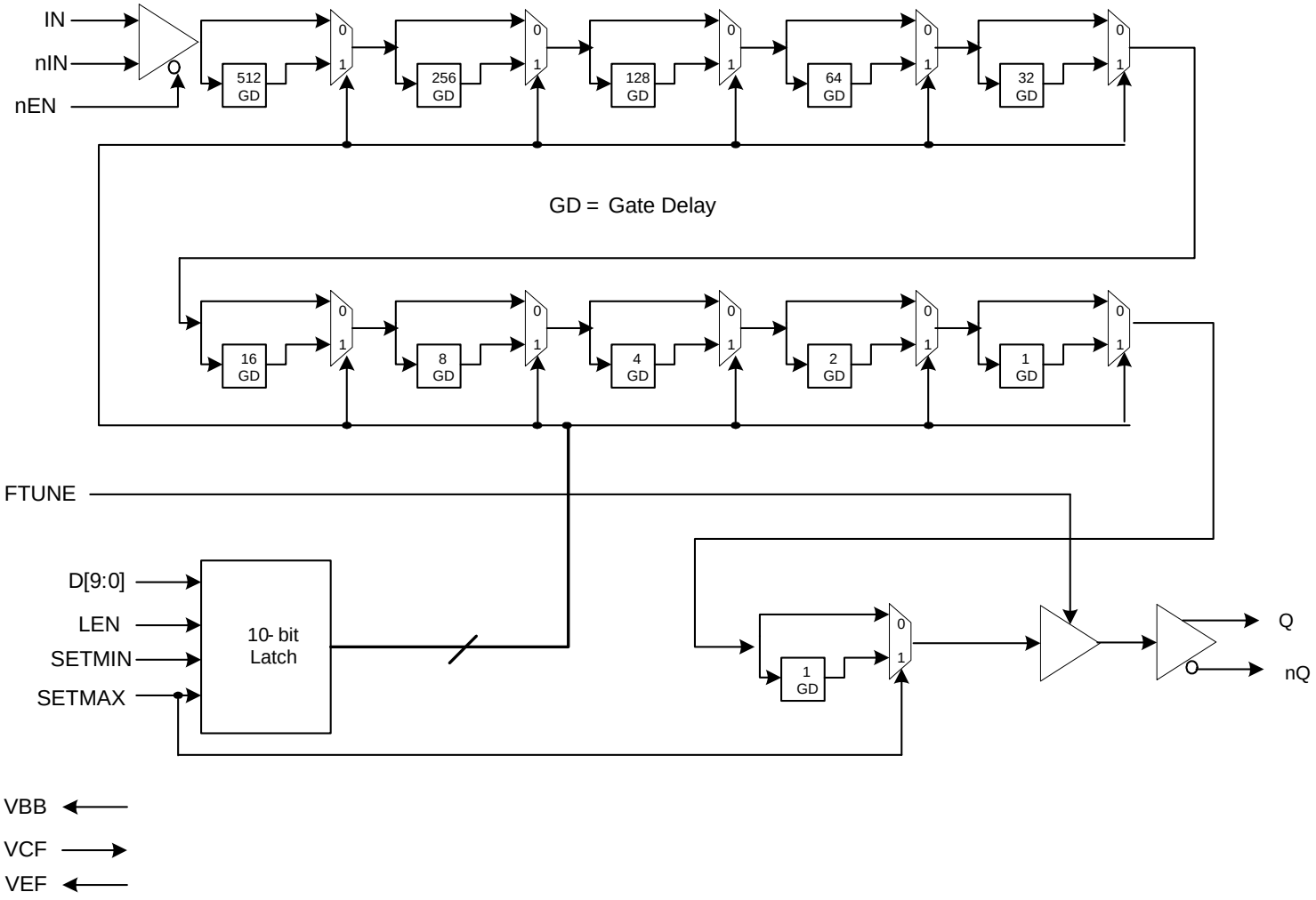
Pin Assignment



ICS854S296I-33

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm EPad
K Package
Top View

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

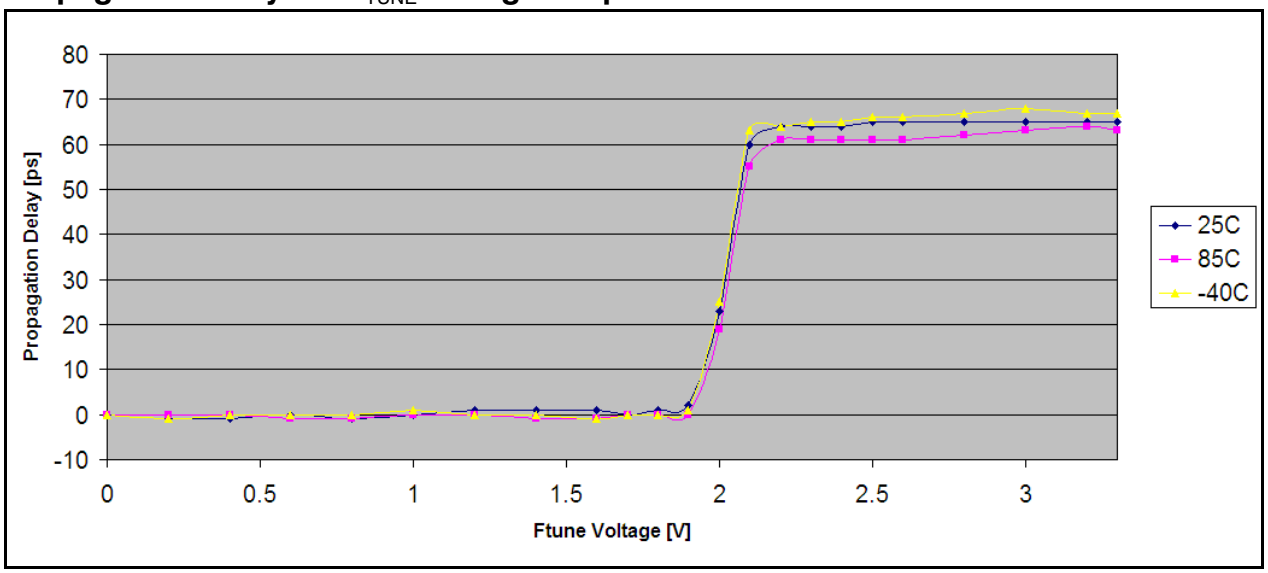
Number	Name	Type		Description
1, 2, 23, 25, 26, 27, 29, 30, 31, 32	D8, D9, D0, D1, D2, D3, D4, D5, D6, D7	Input	Pulldown	Parallel data input D[9:0]. Single-ended LVCMOS, LVTTL, LVPECL interface levels.
3, 14, 15	RESERVED	Reserved		Reserved pins.
4	IN	Input	Pulldown	Non-inverting LVPECL differential input.
5	nIN	Input	Pullup/ Pulldown	Inverting LVPECL differential input.
6	V_{BB}	Output		Reference voltage output. This pin can be used to rebias AC-coupled inputs to IN and nIN. When used, de-couple to V_{DD} using a 0.01μF capacitor. If not used, leave floating.
7	V_{EF}	Output		Reference voltage output. See Table 3C.
8	V_{CF}	Input		Reference voltage input. The voltage driven on V_{CF} sets the logic transition threshold for D[9:0].
9, 24, 28	GND	Power		Power supply ground
10	LEN	Input	Pulldown	D inputs LOAD and HOLD control input. When HIGH, latches the D[9:0] bits. When LOW, the D[9:0] latches are transparent. Single-ended LVPECL interface levels. See Table 3B.
11	SETMIN	Input	Pulldown	Minimum delay set logic input. When HIGH, D[9:0] registers are reset. When LOW, the delay is set by SETMAX or D[9:0]. Default is LOW when left floating. Single-ended LVPECL interface levels. See Table 3D.
12	SETMAX	Input	Pulldown	Maximum delay set logic input. When SETMAX is set HIGH and SETMIN is set LOW, D[9:0] = 1111111111. When SETMAX is LOW, the delay is set by SETMIN or D[9:0]. Default is low when left floating. Single-ended LVPECL interface levels. See Table 3D.
13, 18, 19, 22	V_{DD}	Power		Positive supply pins.
16	nEN	Input	Pulldown	Single-ended control enable pin. When LOW, Q is delayed from IN. When HIGH, Q is a differential LOW. Default is LOW when left floating. Single-ended LVPECL interface levels. See Table 3A.
17	F_{TUNE}	Analog Input		Fine tune delay control input. By varying the input voltage, it provides an additional delay finer than the 10ps digital resolution.
20, 21	nQ, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ

Propagation Delay vs. F_{TUNE} Voltage Graph



Function Tables

Table 3A. Delay Enable

nEN	Q, nQ
0 (default)	IN, nIN delayed
1	Q = LOW, nQ = HIGH

Table 3B. Digital Control Latch

LEN	Latch Action
0 (default)	Pass Through D[9:0]
1	Latched D[9:0]

Table 3C. V_{CF} Connection for D[9:0] Logic Interface

Input	V_{CF} Connection	D[9:0] Logic Interface
V_{CF}	V_{EF} (NOTE 1)	LVPECL
V_{CF}	No Connect	LVCMOS
V_{CF}	1.5V source	LVTTL

NOTE 1: Short V_{CF} (pin 8) to V_{EF} (pin 7).

Table 3D. Theoretical Delta Delay Values

D[9:0] Value	SETMIN	SETMAX	Programmable Delay[NOTE 1] (ps)
XXXXXXXXXX	H	L	0
0000000000	L	L	0 (default)
0000000001	L	L	10
0000000010	L	L	20
0000000011	L	L	30
0000000100	L	L	40
0000000101	L	L	50
0000000110	L	L	60
0000000111	L	L	70
0000001000	L	L	80
0000010000	L	L	160
0000100000	L	L	320
0001000000	L	L	640
0010000000	L	L	1280
0100000000	L	L	2560
1000000000	L	L	5120
1111111111	L	L	10230
XXXXXXXXXX	L	H	10240

NOTE 1: Fixed minimum delay not included.
NOTE: Refer to Table 6, *AC Characteristics*, for typical Step Delay values.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	39.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	No load, max V_{DD}			150	mA

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	D[9:0]	$V_{DD} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	D[9:0]	V_{DD} = 3.6V, V_{IN} = 0V	-10			µA

Table 5C. LVPECL Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	IN, nIN	$V_{DD} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	IN	V_{DD} = 3.6V, V_{IN} = 0V	-10			µA
		nIN	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Range; NOTE 1			GND + 1.2		V_{DD}	V
V_{BB}	Output Voltage Reference			V_{DD} – 1.55	V_{DD} – 1.35	V_{DD} – 1.15	V
V_{EF}	Mode Connection			V_{DD} – 1.40	V_{DD} – 1.30	V_{DD} – 1.20	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 5D. LVPECL Single-Ended DC Characteristics, V_{DD} = 3.3V ± 0.3V, GND = 0V, T_A = -40°C to to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage; NOTE 1	IN, nIN, LEN, D[9:0], nEN, SETMIN, SETMAX		V_{DD} – 1.3		V_{DD} – 0.940	V
V_{IL}	Input Low Voltage; NOTE 1	IN, nIN, LEN, D[9:0], nEN, SETMIN, SETMAX		V_{DD} – 1.870		V_{DD} – 1.45	V
I_{IH}	Input High Current	IN, nIN, LEN, D[9:0], nEN, SETMIN, SETMAX	V_{DD} = V_{IN} = 3.6V			150	µA
I_{IL}	Input Low Current	SETMIN, SETMAX, IN, LEN, D[9:0], nEN	V_{DD} = 3.6V, V_{IN} = 0V	-10			µA
		nIN	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA

NOTE 1: To enable LVPECL interface levels on pins D[9:0], pin 7 must be shorted to pin 8. See Table 3C.

Table 5E. LVDS DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		350		650	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.10		1.30	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

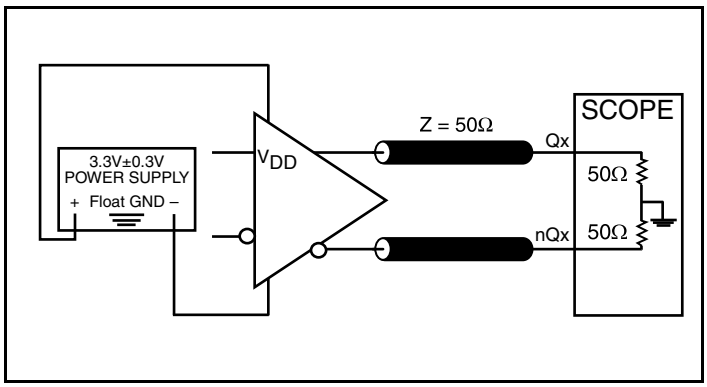
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

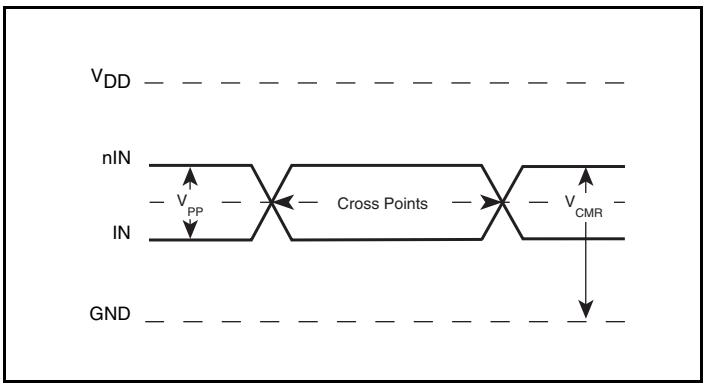
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					1.2	GHz
t_{PD}	Propagation Delay	IN to Q, nQ	Dx = 0	1800	2200	2700	ps
		IN to Q, nQ	Dx = 1023	10000	12500	15000	ps
		nEN to Q, nQ	Dx = 0	1900	2200	2700	ps
t_{PD_RANGE}	Programmable Propagation Range		$t_{PD\_MAX} - t_{PD\_MIN}$	8200			ps
Δt	Step Delay		D0 = HIGH		15		ps
			D1 = HIGH		25		ps
			D2 = HIGH		45		ps
			D3 = HIGH		85		ps
			D4 = HIGH		165		ps
			D5 = HIGH		330		ps
			D6 = HIGH		645		ps
			D7 = HIGH		1270		ps
			D8 = HIGH		2540		ps
			D9 = HIGH		5075		ps
			D[9:0] = HIGH		10135		ps
INL	Integral Non-Linearity; NOTE 1				±10		ps
t_S	Setup Time	D to LEN			-185		ps
		D to IN, nIN			-200		ps
		nEN to IN, IN			-360		ps
t_H	Hold Time	LEN to D			-275		ps
		IN, nIN to nEN			-875		ps
t_R	Release Time	nEN to IN, nIN			465		ps
		SETMAX to LEN			735		ps
		SETMIN to LEN			775		ps
t_R / t_F	Output Rise/Fall Time	Q, nQ	20% to 80% at 100MHz	70		300	ps
odc	Output Duty Cycle		$f_{OUT} \leq$ 625MHz	40		60	%

NOTE: Characterized up to f_{OUT} = 1.2GHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Deviation from a linear delay (actual Min. to Max.) in the 1024 programmable steps.

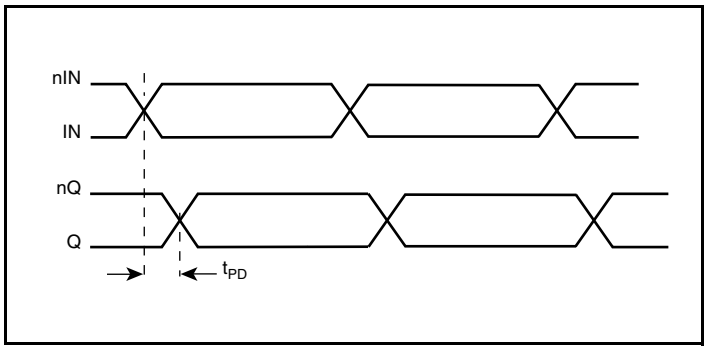
Parameter Measurement Information



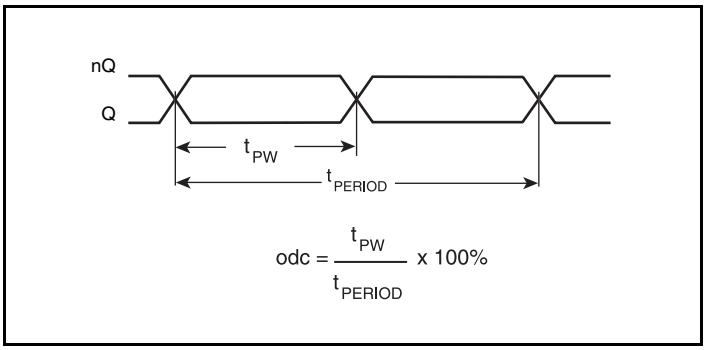
LVDS Output Load Test Circuit



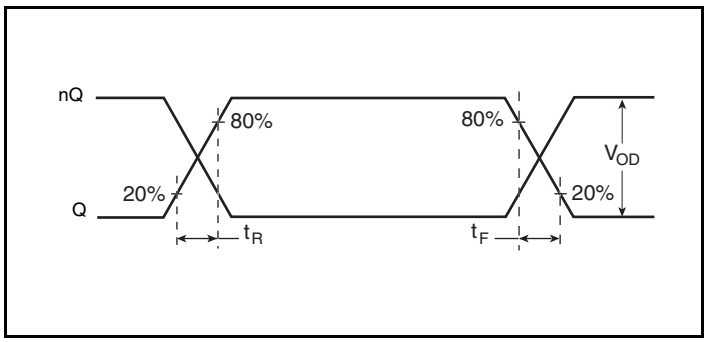
Differential Input Level



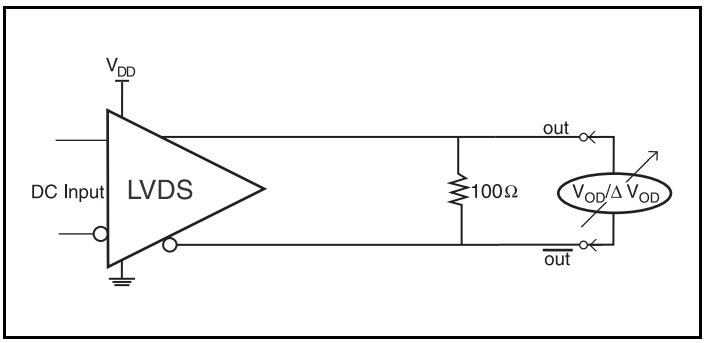
Propagation Delay



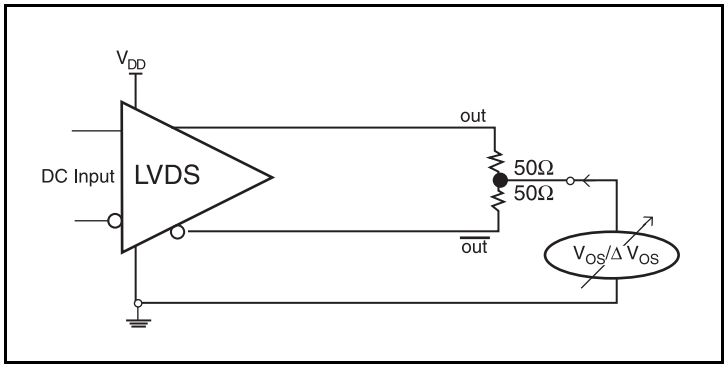
Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

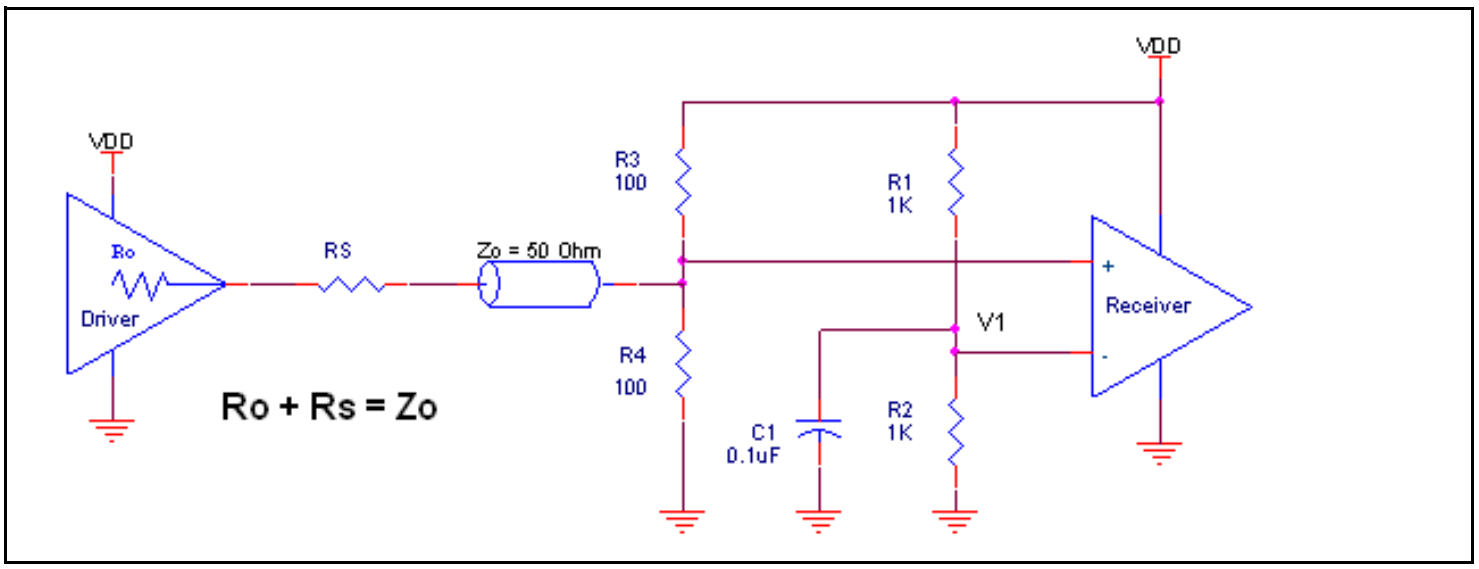


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

LVPECL Clock Input Interface

The IN/nIN accepts LVPECL, CML, LVDS and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the IN/nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

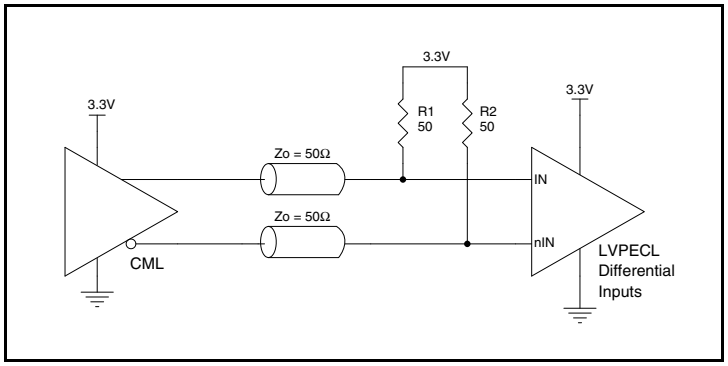


Figure 2A. IN/nIN Input Driven by a CML Driver

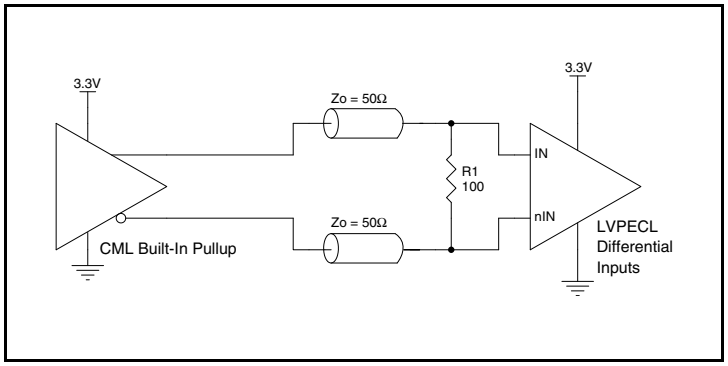


Figure 2B. IN/nIN Input Driven by a Built-In Pullup CML Driver

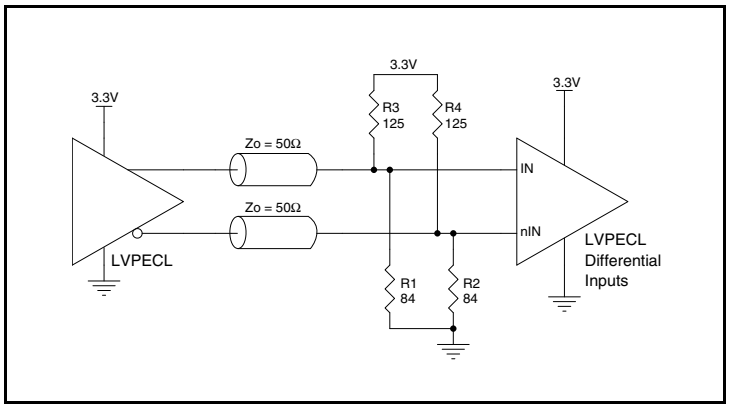


Figure 2C. IN/nIN Input Driven by a 3.3V LVPECL Driver

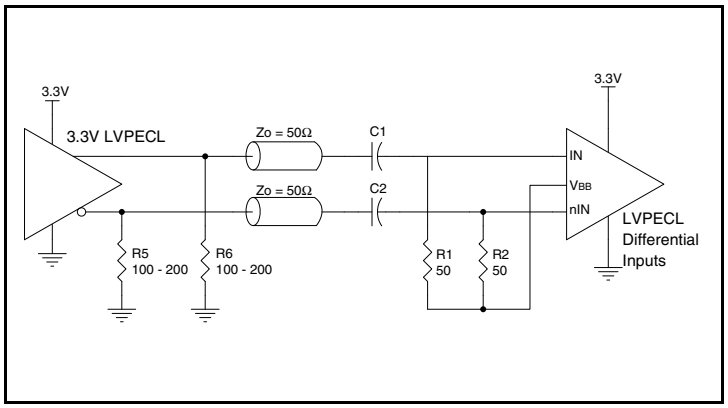


Figure 2D. IN/nIN Input Driven by a 3.3V LVPECL Driver with AC Couple

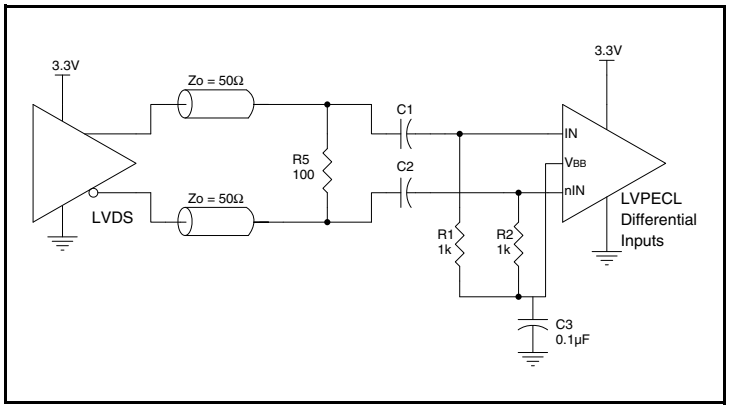


Figure 2E. IN/nIN Input Driven by a 3.3V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

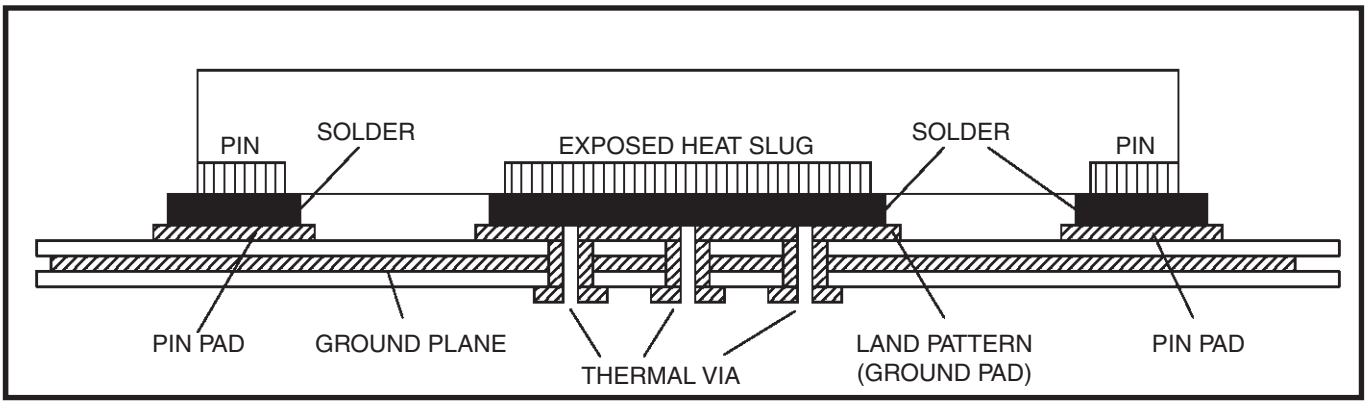


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

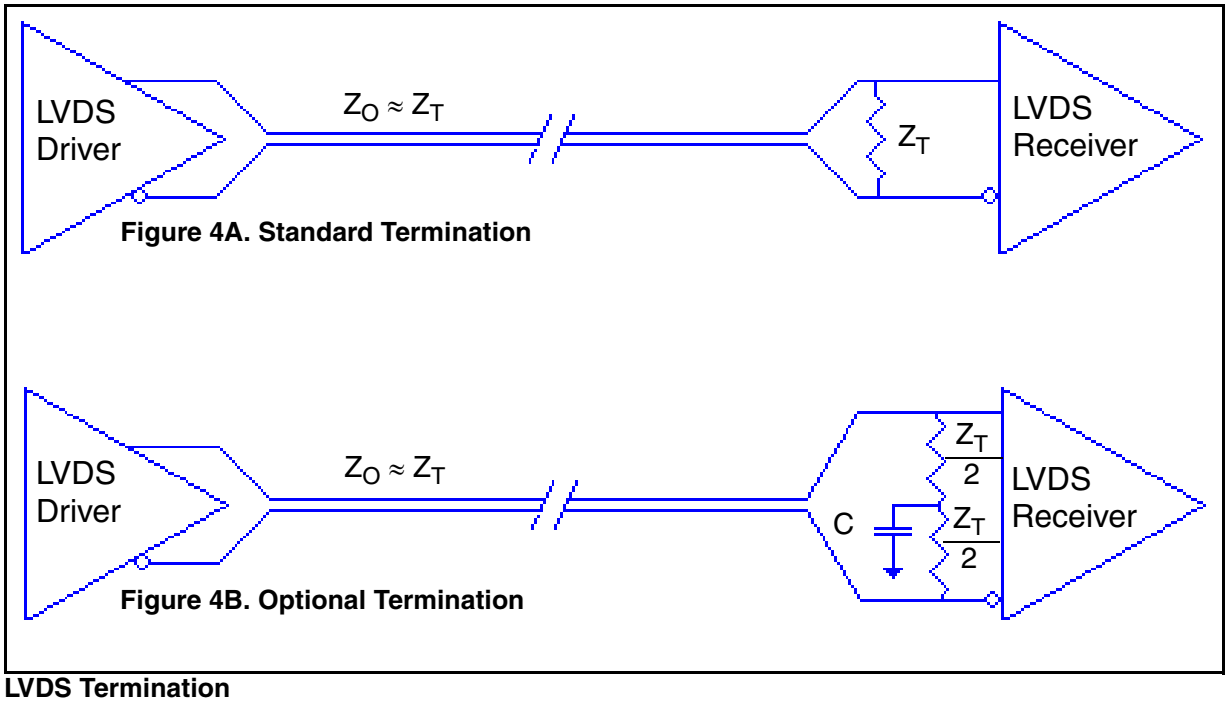


Figure 4A. Standard Termination

Figure 4B. Optional Termination

LVDS Termination

Schematic Layout

Figure 5 (next page) shows an example ICS854S296I-33 application schematic. The schematic focuses on functional connections and is not configuration specific. Input and output terminations shown are intended as examples only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

In this example schematic, the input is driven by a 3.3V LVPECL driver but HCSL or LVDS inputs will work as well. V_{CF} is depicted as a No Connect, which selects LVCMOS levels for pins D[9:0]. D[9:0], nEN, LEN, SETMIN and SETMAX are set by pull up and pull down resistors for compensation of a static delay, the most common application. LEN can hardwired to a logic low so that D[9:0] pin values are not latched, but instead directly set the internal logic values. This allows pin strapping to avoid the need for an external control of the LEN latch pin.

All the control pins can be defined with an FPGA, rather than pull up and pull down resistors as shown in the schematic, if the delay is determined after board fabrication or if the delay requirement is dependant on the exact system configuration. Note that nEN, LEN, SETMIN, SETMAX are LVPECL levels by design but can be overdriven by LVCMOS input levels, as is done with the external pull ups and pull downs in this example.

FTUNE allows for interpolation of the total path delay between the resolution of the D[9:0] step size for higher frequency clocks. This pin has an RC low pass filter to suppress any noise coupled onto F_{TUNE}. F_{TUNE} can also be set with a voltage divider if the required delay is known beforehand, but use of a DAC, as shown in the schematic allows for finer control of the delay. For lower frequency clocks this pin can instead be pulled to ground to set the analog delay to zero.

To achieve optimum jitter performance, device power supply isolation from the board supply is required. The ICS854S296I-33 provides separate V_{DD} and GND pins for optimum power filtering across the device.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors directly connected to the power and FTUNE pins be placed on the device side of the PCB as close to their corresponding pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uf and 0.1uF capacitor connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

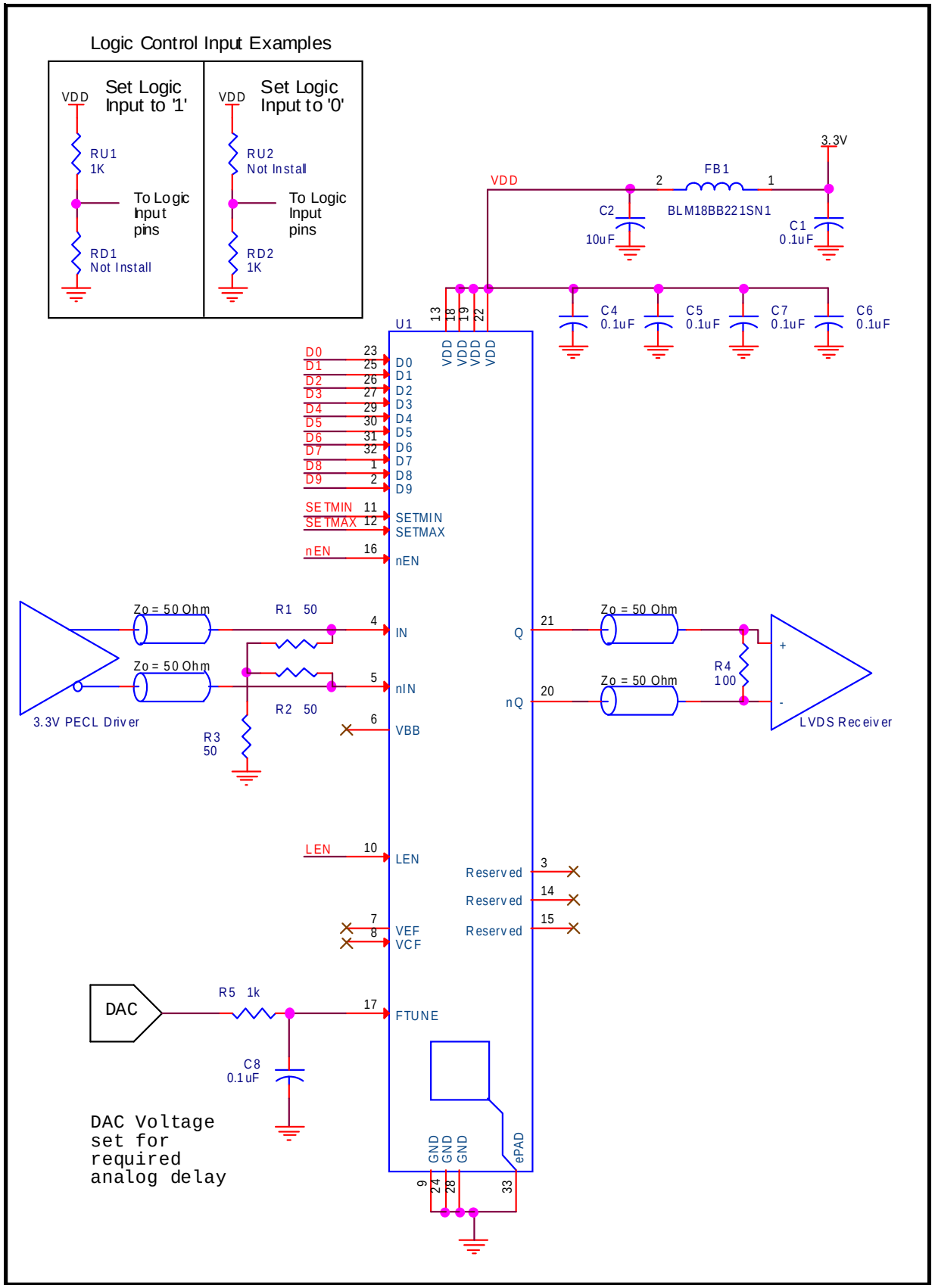


Figure 5. ICS854S296I-33 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S296I-33.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S296I-33 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 150mA

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.6V * 150mA = **540mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.540W * 39.5°C/W = 106.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

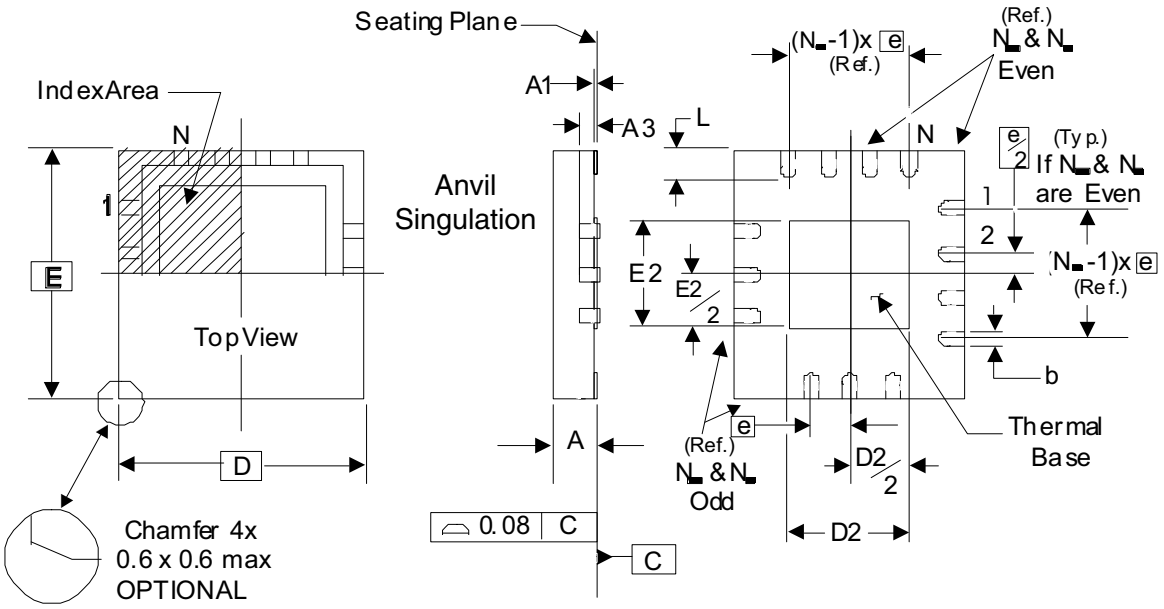
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

Transistor Count

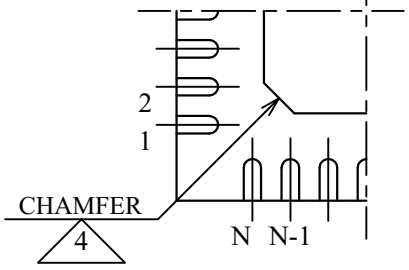
The transistor count for ICS854S296I-33 is: 8686

Package Outline and Package Dimensions

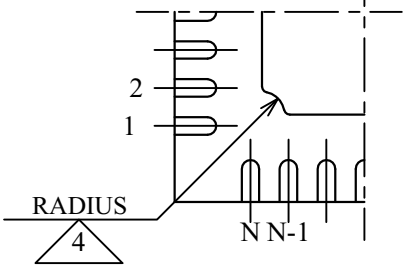
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The mechanical package drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S296DKI-33LF	ICS296DI33L	Lead-Free, 32 Lead VFQFN	Tray	-40°C to +85°C
854S296DKI-33LFT	ICS296DI33L	Lead-Free, 32 Lead VFQFN	Tape & Reel	-40°C to +85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T1 T5D	3 6	Pin Description Table, corrected Pin 6, V_{BB} description. LVPECL Single-ended DC Characteristics Table - deleted Note 2.	1/15/2014

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