IDT82V3280 Device Errata

Notes

Supplemental Information

This errata supplements the datasheet. It provides information regarding an IDT82V3280 locking status of the IN14 if this input reference selector is set for Force Select to IN14 and MFRSYNC_2K output of the master and slave devices synchronization to each other in pulse mode.

Description

The IDT82V3280 T0 and T4 PLL will always stay in holdover mode if the reference selector is set for Force Select to IN14.

Work-Around: The software must place IDT82V3280 IN14 in Auto Select mode and set IN14 at the highest priority valid clock [or Register 2Ch, Bit 7-4 IN14_SEL_PRIORITY[3:0]= '0001'] among the valid input references and the switch mode is set to 'revertive mode' [or Register 09h, bit 0 = '1'], then the IDT82V3280 will always lock to IN14. If there is only one valid input reference at IN14, then other input references can be changed to in-valid by setting the 'remote-valid' bit to '1' [or Register 4Ch and Register 4Dh bits set to all '1' except Register 4D bit 5 = '0'].

This known discrepancy is fixed in the new silicon IDT82V3280A revision.

Description

In master-slave configurations where both MFRSYNC_2K and FRSYNC_8K must be synchronized, the slave EX_SYNC1 must be connected to the master MFRSYNC_2K. If MFRSYNC_2K is placed in pulsed mode, then the master MFRSYNC_2K pulse and slave MFRSYNC_2K will not synchronize to each other after the slave is reset or after the slave is reset and the slave registers are reloaded.

Work-Around: The IDT82V3280 master MFRSYNC_2K must be in clock mode [or Register 74h bit 0 = '0'] in order for the slave MFRSYNC_2K to sync to the master MFRSYNC_2K. The FRSYNC_8K will synchronize in both clock mode and pulse mode.

This known discrepancy is fixed in the new silicon IDT82V3280A revision.