

Notes

Introduction

This document provides general guidelines to help design IDT's 89PES4T4QFN PCI Express 4-port switch (PES4T4QFN) and also applies to the PES3T3QFN. This document describes the following switch interfaces and provides appropriate board design related recommendations:

- 1) 2.5Gbps high-speed differential pairs
- 2) Clocking
- 3) Footprint example
- 4) Power and decoupling
- 5) Boot Configuration Vector (BCV)
- 6) Reset scheme
- 7) SMBus
- 8) GPIO and JTAG
- 9) QFN Layout Recommendation

The PES4T4QFN is a four port transparent switch that contains 4 PCI Express lanes. Each of the four ports is statically allocated 1 lane with ports labeled as 0, 2, 3, and 4. Port 0 is always the upstream port while ports 2, 3, and 4 are always downstream ports. Optional initialization from a serial EEPROM is selected via the Switch Mode (SWMODE[2:0]) inputs, part of the Boot Configuration Vector (BCV).

During link training, link width is automatically negotiated. Each PES4T4QFN port is capable of independently negotiating to x1 width.

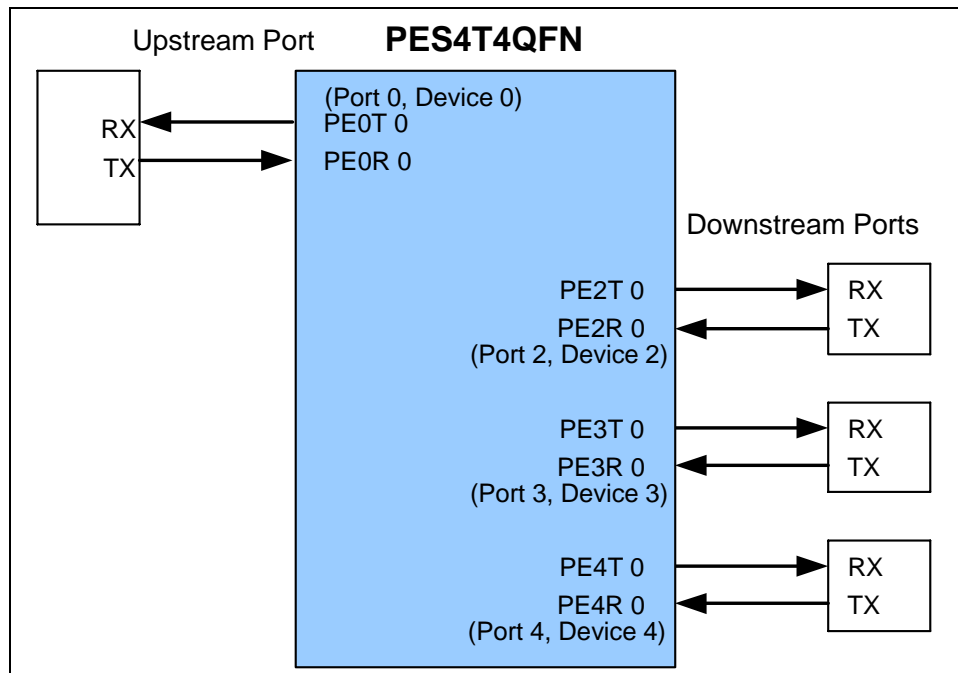


Figure 1 Port Numbering and Device Numbering

2.5Gbps Differential Pairs

- The PES4T4QFN includes 50 Ohm resistor on-die terminations on both transmit and receive pins so that no external termination is required per PCIe specifications.
- Minimal vias should be considered in addition to those needed for IC pads or a connector.
- The PES4T4QFN Transmit and Receive differential pairs could be routed on the top side of the board to take advantage of the switch pinout, to facilitate decoupling and to reduce the number of vias. 5 mil wide microstrip spaced 11 mils apart (center-to-center) is the general guideline to yield a differential impedance of 100 Ohms. However, for a given trace impedance, the trace width may vary depending on which layer the trace resides or the overall board thickness/stackup and material selected (please consult with the PCB manufacture for exact dimensions).
- Individual traces within a given differential pair (positive and negative) must be matched in length to a tolerance of 5 mils.
- In addition, the spacing between different pairs of the 2.5G Serial Link differential pairs (transmit as well as receive) must be at least 20 mils edge-to-edge to prevent crosstalk.
- It should be noted that trace length matching among pairs is not required as the PCIe specifications allow up to 20ns of skew among differential pairs.
- AC coupling capacitors are associated with the Tx differential pairs and should be located symmetrically on the top or bottom layer between the PES4T4QFN and the PCIe connectors, as shown to Figure 1. Values between 75nF and 200nF are appropriate, per the PCI Express specification. For example, 100nF in 0402 size capacitors are used on the PES4T4QFN evaluation board.

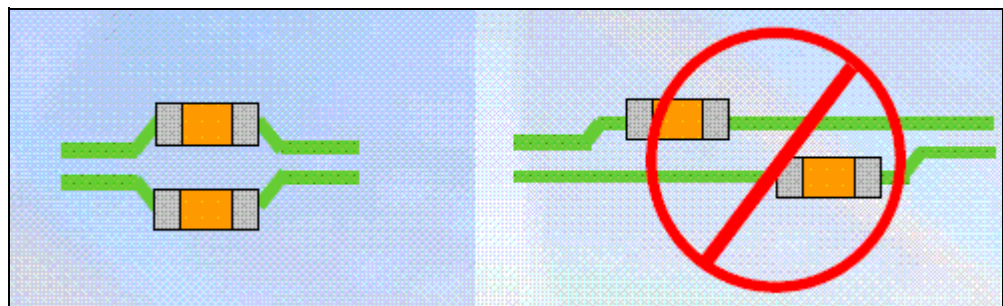


Figure 2 AC Decoupling Capacitor Layout

Avoid 90-degree bends or turns on traces. Whenever possible, the number of left and right bends should be matched as closely as possible. Alternating left and right turns helps to minimize length skew differences between each signal of a differential pair.

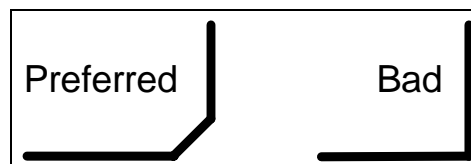


Figure 3 Acceptable Bends and Unacceptable Bends

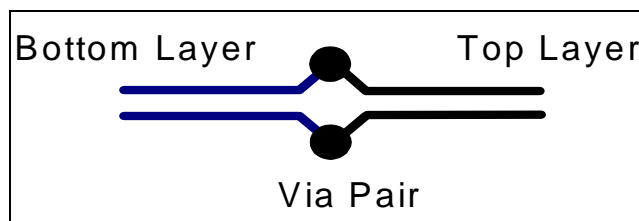


Figure 4 Via Placement

- Vias should be avoided as much as possible on the PCIe differential pairs (as described above) since they can result in up to a 0.25 dB loss per via.
- When a via is required, its pad size should be less than 25 mils, its hole size should be 14 mils or less and its anti-pads less or equal to 35 mils.
- Depending on the system topology and the maximum targeted trace length, regular FR4 material is appropriate dielectric material. In the case of a backplane type of application, higher quality, lower loss material, such as Nelco 4000-13, may be needed.
- Simulations are recommended and IDT provides an Hspice development kit.

Polarity inversion is automatically supported to facilitate the ease of routing:

- Each lane of the PES4T4QFN supports automatic polarity inversion as required by the PCIe Base specification 1.1. Polarity inversion is a function of the receiver to detect when an inversion occur but not the transmitter. Polarity inversion is a lane and not a link function.

Clocking

- Clock lines must be kept at least 25 mils away from other signals.
- Minimize extra via in addition to those needed for IC pads.
- If an inner signal layer is used, the clock line should stay on this layer except when it connects to the IC pads.
- Individual traces within a given differential pair (positive and negative) must be matched in length to a tolerance of 5 mils.
- The clock lines are differential pairs and they should be routed according to the restrictions of this section as well as the 2.5Gbps Differential Pairs section. Please refer to the manufacture's datasheet of the selected clock buffer or generator for additional recommendations.
- Any termination should be implemented so as to minimize the trace stubs.
- The PES4T4QFN input clock buffers support 100MHz clock frequency as well as SSC as defined by PCI Express specifications Rev 1.1.
- The PES4T4QFN input clock buffers support LVDS, LVPECL, CML, and HSTL clock signaling. An AC-coupled interface is required so that only the AC information of the clock source is transmitted to the inputs. A 0402 0.1µF capacitor is appropriate.

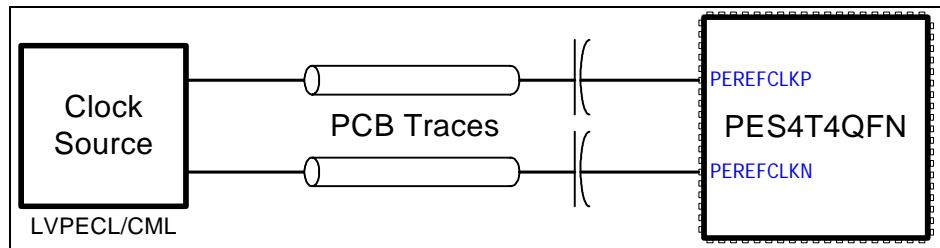


Figure 5 LVPECL / CML Clock Source Circuit Implementation

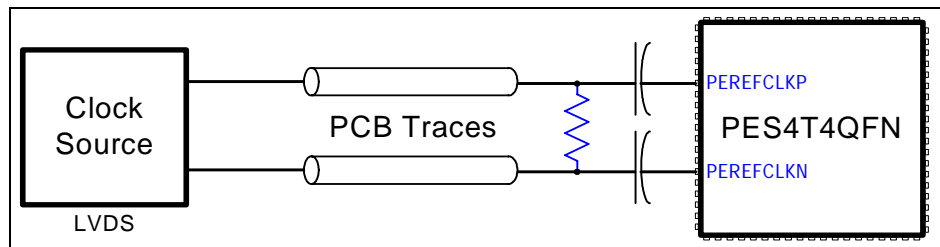


Figure 6 LVDS Clock Source Circuit Implementation

LVDS clock source requires a DC termination path. A 2K common mode resistor must be inserted before the capacitors and between the differential pair as shown in Figure 6. This resistor should be placed close to the clock source.

Please refer to the datasheet of the selected clock generator or buffer for implementation and additional requirements.

Footprint Example

The footprint view of the PES4T4QFN chip is shown in Figures 7 and 8. There are many other possible implementations. These are only given as an example.

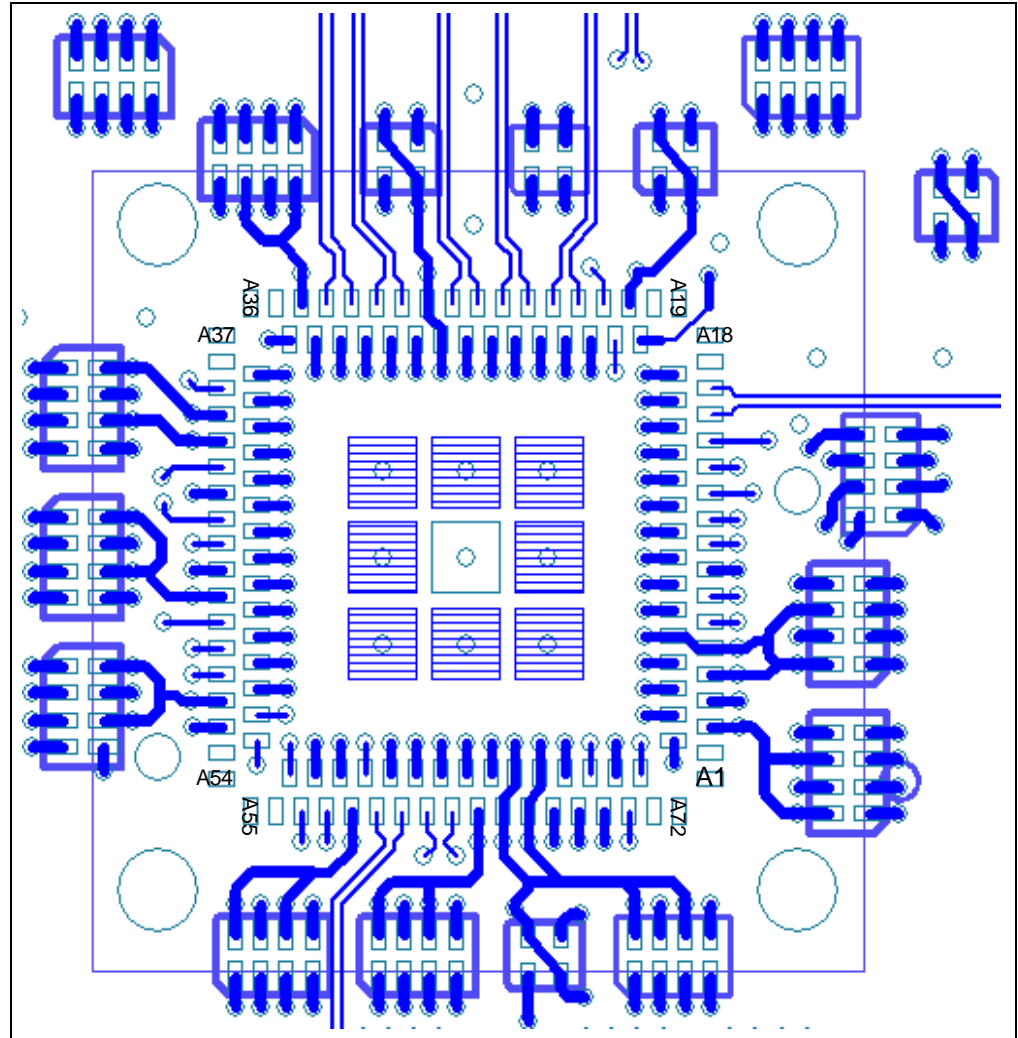


Figure 7 89PES4T4QFN Footprint Example (Top Layer)

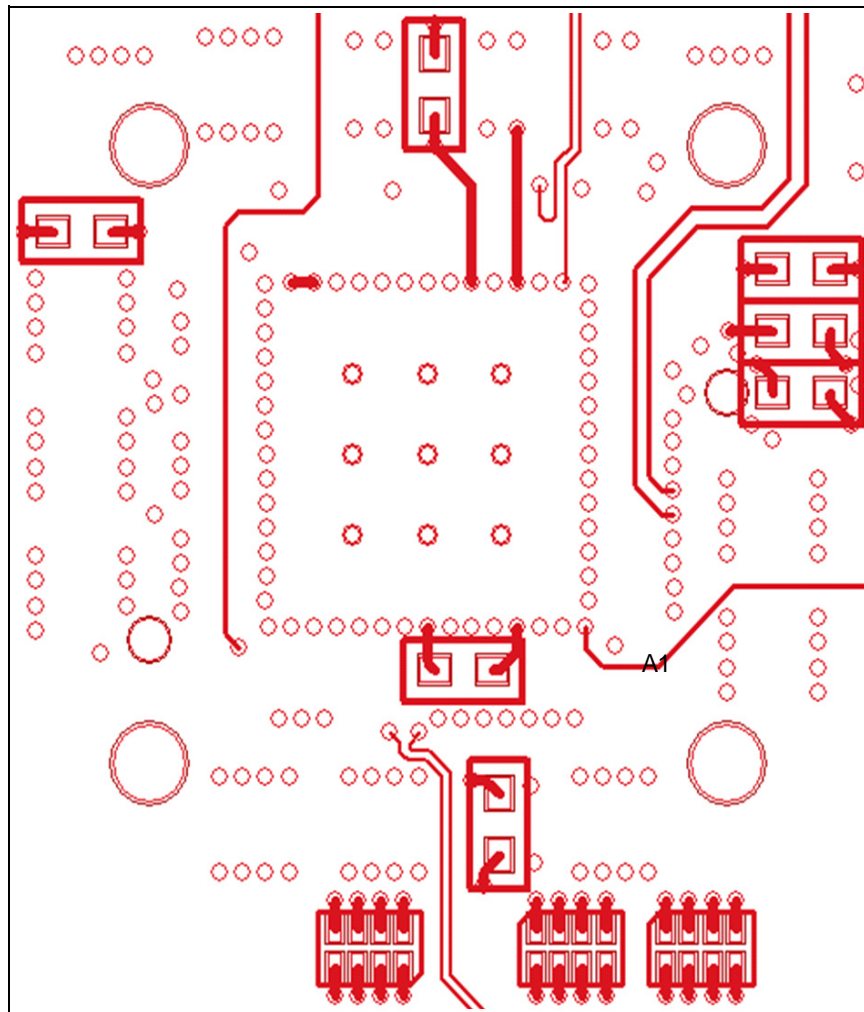


Figure 8 89PES4T4QFN Footprint Example (Bottom Layer)

Power and Decoupling Scheme

The PES4T4QFN has five different power supplies pins:

- $V_{DD}Core$ powers the digital core of the switch.
- $V_{DD}PE$ powers the SERDES core and the receive clock recovery logic.
- $V_{DD}APE$ powers analog circuits such as PLL and bias generator.
- $V_{TT}PE$ is the termination voltage used on the SERDES TX lines. V_{tt} can be adjusted to modify the TX common mode voltage as well as the voltage swing.
- $V_{DD}IO$ powers the low speed IOs of the switch.

The respective standard and maximum power consumption are listed in the 89PES4T4QFN Data Sheet. Bulk capacitors should be used to filter out low frequency noise. Because capacitors can be located around the chip, they do not represent any specific design challenge.

A total of 2x 0.1 μ F and 2x 0.01 μ F capacitors are recommended as the minimum number of bypass capacitors for each $V_{DD}PE$, $V_{DD}APE$, and $V_{TT}PE$ supply and one 0.1 μ F per $V_{DD}Core$ pin.

Note the following:

- 0402 package ceramic capacitors are recommended for 0.1 μ F and 0.01 μ F capacitors
- Some of the vias can be shared in order to create space by stack capacitors on top/bottom layers and placing them close to a pin.
- Capacitors are placed based on space availability, however capacitor arrays (2/4-element) are used in the reference design to demonstrate the additional space saving.
- Larger 1 μ F and 47 μ F ceramic capacitors should be added around the part to filter out low-frequency noise. Two (one minimum) bulk capacitors per voltage supply are appropriate. One option is to spread them out around the chip at four corners, top, and bottom layers of the PCB.
- Prioritize the bypass capacitors in the following order for each supply (1 - most important, 5 - least critical):
 1. $V_{DD}Core$
 2. $V_{DD}PE$
 3. $V_{DD}APE$
 4. $V_{TT}PE$
 5. $V_{DD}IO$
- $V_{DD}Core$, $V_{DD}PE$, and $V_{DD}APE$ can be generated from the same voltage source provided that appropriate bypass and filter networks are implemented for $V_{DD}APE$ and that the voltage source current rating meets the chip maximum requirement without exceeding its own thermal limitations.
- $V_{TT}PE$ will require its own voltage source, preferably adjustable since its value may be subject to change if bigger voltage swings are required. Refer to the 89PES4T4QFN Data Sheet for more details on the termination voltage requirements.
- Depending on whether switching or linear regulators are used, a total of two or three voltage sources will be required: one for $V_{DD}Core$ due to its current need, one for $V_{DD}PE$ and $V_{DD}APE$, and one for $V_{TT}PE$. All voltages should have a common V_{SS} reference at board level.

A ferrite bead can be used to attenuate the power noise and improve the analog circuit performance in a noisy environment. The following three parameters should be considered when you select a ferrite bead for power rails:

- 1) very low DC resistance
- 2) impedance of 50 - 120 ohms at 100MHz
- 3) provides enough DC current

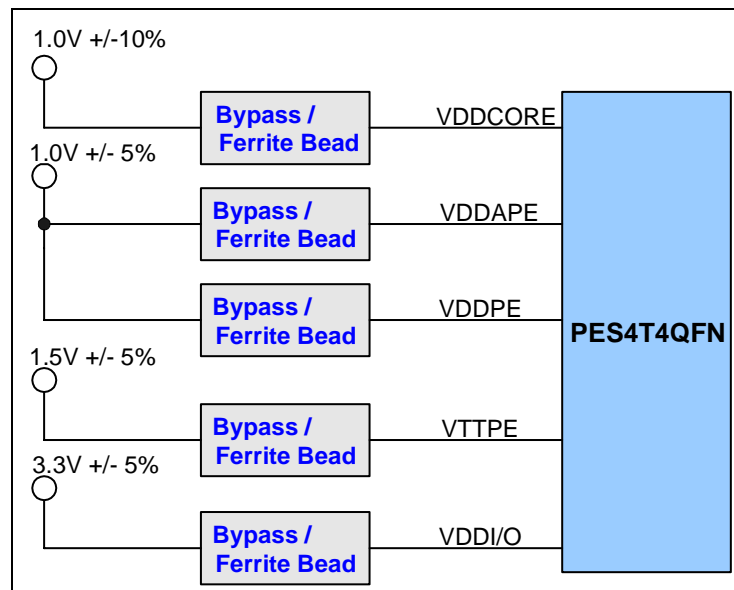


Figure 9 Board Power Supply Arrangement

Power-Up/Power-Down Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES4T4QFN, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels.

The power-down sequence must be in the reverse order of the power-up sequence.

Power Consumption

The typical and maximum power consumption can be found in the appropriate switch data sheet (see Reference Documents at the end of this guide).

Boot Configuration Vector (BCV)

A boot configuration vector consisting of the signals listed in Table 1 is sampled by the PES4T4QFN during a fundamental reset when PERSTN is negated. The boot configuration vector defines essential parameters for switch operation.

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. Please refer to the Clock Operation section in the device user manual on the clock mode implementation for the application.
CCLKUS	I	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. Please refer to the Clock Operation section in the device user manual on the clock mode implementation for the application.
PERSTN	I	Fundamental Reset. Assertion of this signal resets all logic inside the PES4T4QFN and initiates a PCI Express fundamental reset.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES4T4QFN executes the reset procedure and remains in a reset state with the Master SMBuses active. This allows the configuration of the internal registers via an EEPROM before system starts to enumerate the device. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register by via SMBus master.

Table 1 Boot Configuration Vector Signals (Page 1 of 2)

Signal	Type	Name/Description
SWMODE[2:0]	I	Switch Mode. These configuration pins determine the PES4T4QFN switch operating mode. <i>0x0 - Transparent mode</i> <i>0x1 -Transparent mode with serial EEPROM initialization</i>
APWRDISN	I	Auxiliary Power Disable. If this signal is tied to logic '0' at the bootup time then the device is disabled to use auxiliary power and the associated logic on the chip is disabled. All the FRSticky bit values are reset to the default values.
WAKEN	I/O	Wake Input/Output. The WAKEN signal is an input or output. The WAKEN signal input/output selection can be made through WAKEDIR bit setting in the WAKEUPCNTL register. The WAKEN sideband signal is selected as an input by default at the time of power-on reset. The WAKEN signal is automatically disabled when Auxiliary Power is disabled.

Table 1 Boot Configuration Vector Signals (Page 2 of 2)

Pull-up and pull-down resistors directly connected to these signals are appropriate. For debugging purposes, dip-switches provide greater flexibility.

Reset Scheme

PCI Express defines two reset categories: fundamental reset and hot reset. This section will focus on the former, which is implemented through side band signals. For more information on the PES4T4QFN reset characteristics, please refer to the 89HPES4T4QFN PCI Express Switch User Manual.

There are two sub-categories of fundamental reset: cold reset and warm reset. A cold reset occurs following a device being powered on and assertion of PERSTN. A warm reset is a fundamental reset that occurs without removal of power.

The PES4T4QFN implements a reset input pin:

- PERSTN: this is the Fundamental input Reset pin. Assertion of this signal reset all logic inside the PES4T4QFN and initiates a PCI Express fundamental reset.

Figure 10 shows one possible reset implementation where the downstream endpoints can independently have a fundamental reset. This reset scheme should be used if Hot-Plug support on either one of the downstream ports is required.

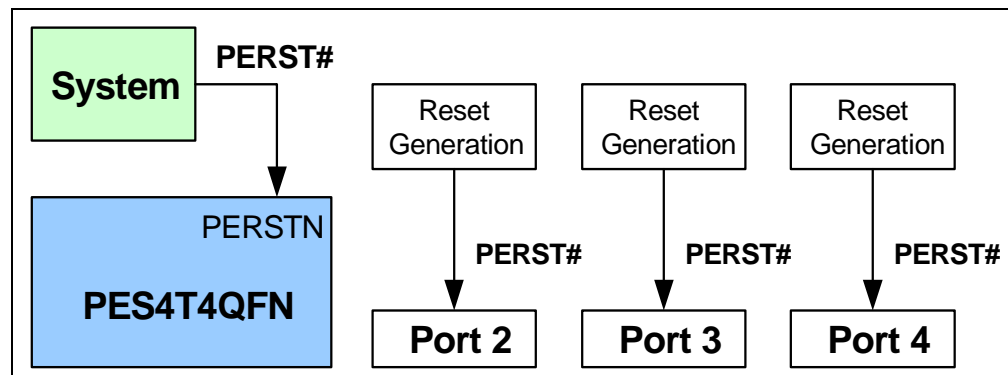


Figure 10 Reset Scheme for Hot Plug Support

If Hot Plug support is not required, the reset circuit can be simplified and connected as shown in Figure 11.

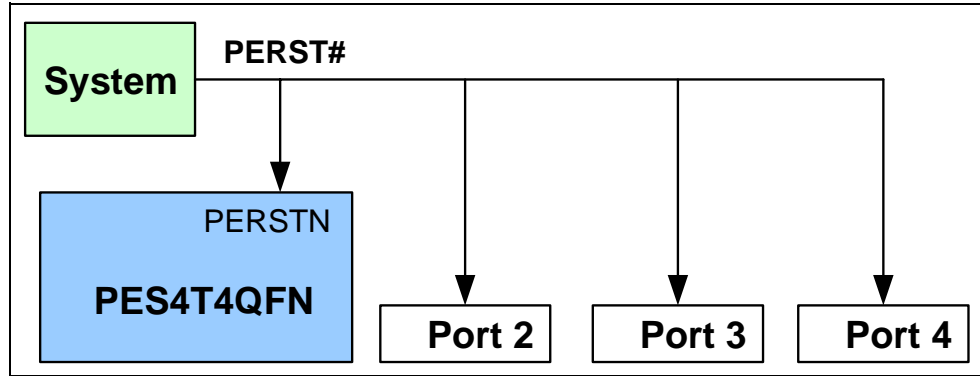


Figure 11 Simplified Reset Scheme

Another way to generate the reset for downstream ports is by using the GPIO pins of the switch, if hot-plug support is required. The GPIO_00, GPIO_01, and GPIO_09 pins can be configured to be the reset signals for the downstream ports by programming the GPIO Function (GPIOFUNC) register via an EEPROM. When a fundamental Reset occurs, all of the GPIO pins default to GPIO inputs. Therefore, the downstream port resets are tri-stated. System designers should use a pull-down on these GPIO pins to ensure that these signals are asserted low before programming GPIOFUNC register. Figure 12 displays the appropriate reset circuit.

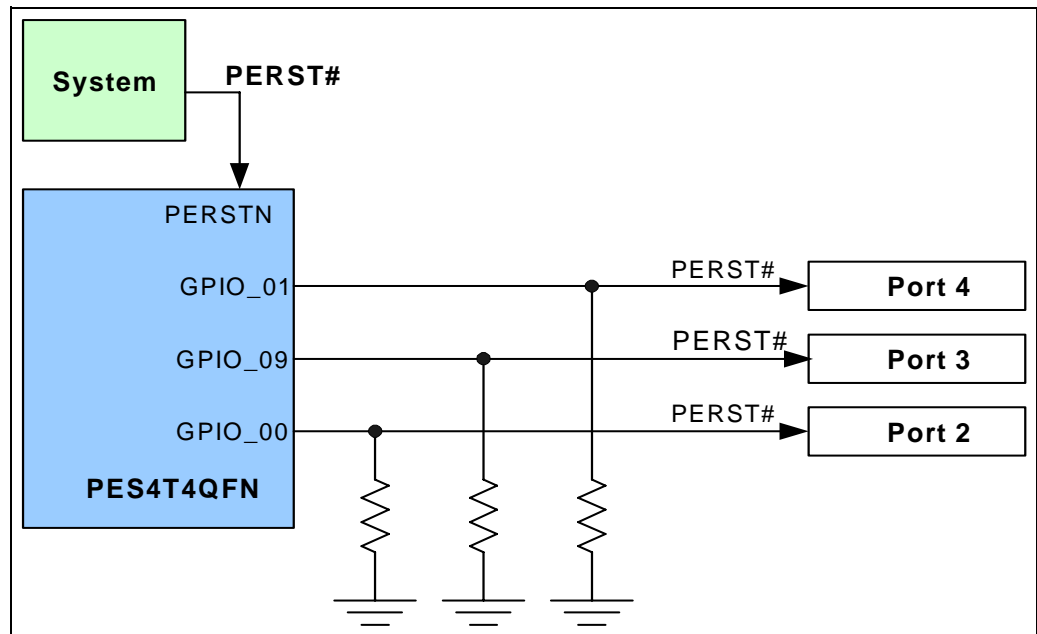


Figure 12 Reset Scheme for Hot Plug Support

RSTHALT

When this signal is asserted high during a PCI Express fundamental reset, the switch continuously returns Configuration Request Retry Completion Status (CRS) to Configuration Requests during the enumeration process. This allows system BIOS to wait until the configuration of switch internal register completed via EEPROM/Master SMBus before normal device operation begins. The device exits the RSTHALT state when the RSTHALT bit is cleared in the SWCTL register by EEPROM/Master SMBus.

This RSTHALT mode is not required in most applications. The RSTHALT pin should be pulled down externally if the application does not use a SMBus master to initialize internal registers.

SMBus

The PES4T4QFN contains one SMBus interface. The Master SMBus interface provides connection for an optional external serial EEPROM used for initialization and an optional I/O expander used for hot-plug signals.

Figure 13 provides a possible implementation involving all the SMBus devices that can connect to the PES4T4QFN Master SMBus interfaces.

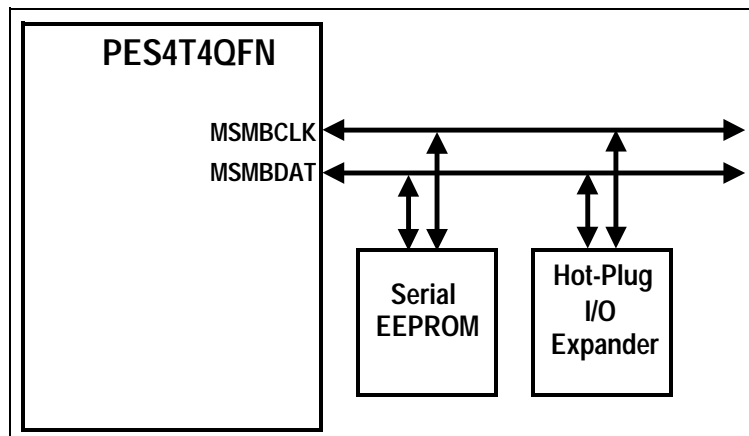


Figure 13 SMBus Configuration

The SMBus interface consists of two signals, clock and data, and 2K pull-up resistors are required on the clock and data lines.

Master SMBus Interface/EEPROM

During a fundamental reset, an optional serial EEPROM may be used to initialize any software visible register in the device.

Serial EEPROM loading occurs if the Switch Mode (SWMODE [2:0]) field selects an operating mode that performs serial EEPROM initialization (e.g., Normal switch mode with serial EEPROM initialization).

Note that the master SMBus clock will be in the active state during loading of the EEPROM contents or while accessing the IO Expanders. Once the operation is completed, the master SMBus clock will be in the inactive state, which is high.

The address used by the SMBus interface to access the serial EEPROM is set to a default value of 1010000b.

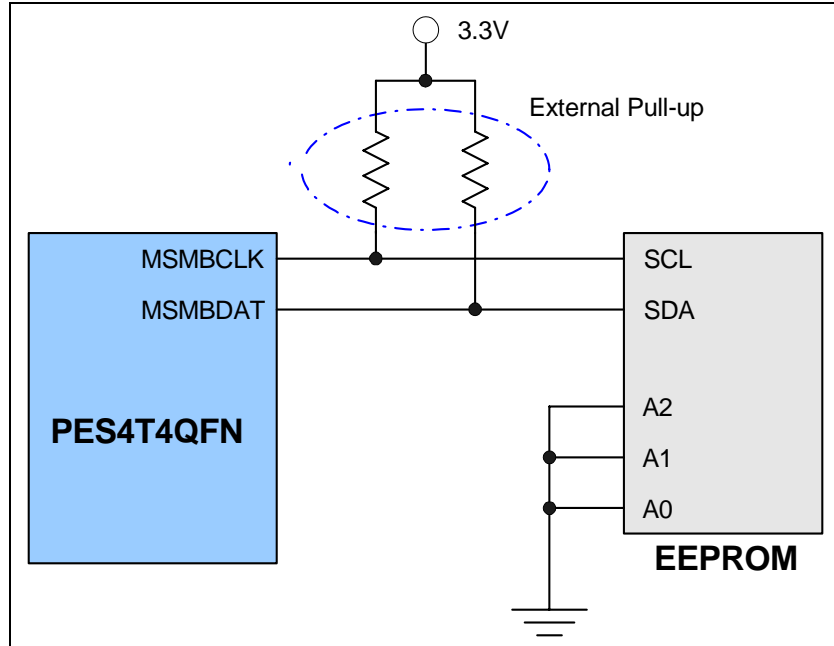


Figure 14 Example of EEPROM Address Configuration for 0b1010_000

Any serial EEPROM compatible with those listed in Table 2 may be used to store PES4T4QFN initialization values. Because some of these devices are larger than the total available PCI configuration space that can be initialized in the PES4T4QFN, EEPROM space may not be fully utilized.

Serial EEPROM	Size
24C32	4 KB
24C64	8 KB
24C128	16 KB
24C256	32 KB
24C512	64 KB

Table 2 PES4T4QFN Compatible Serial EEPROMs

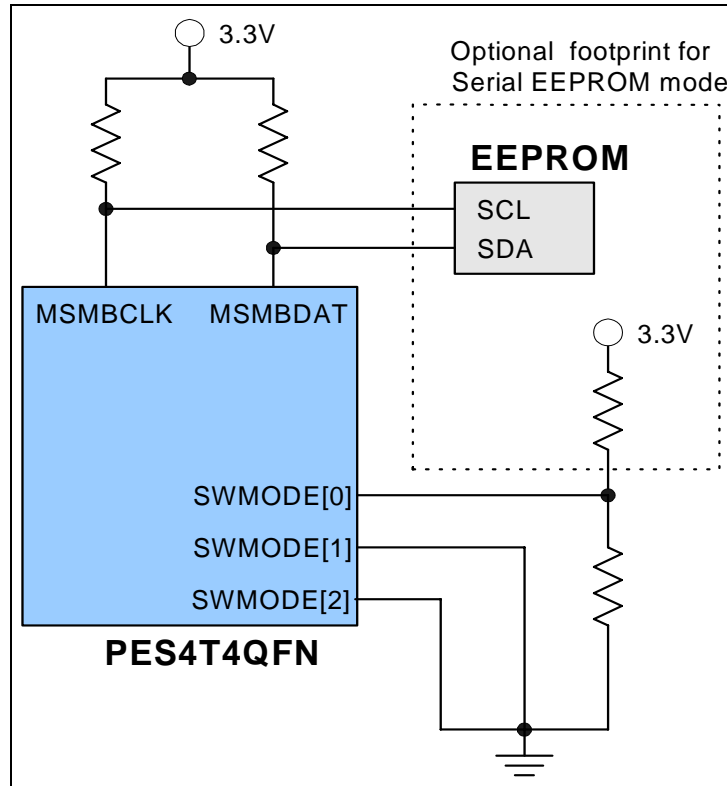


Figure 1 A Typical Implementation for SWMODE Selection and EEPROM Interface

Configuring the I/O Expander Address

The switch utilizes external SMBus/I²C-bus I/O expanders connected to the master SMBus interface for hot-plug and port status signals. The switch is designed to work with Phillips PCA9555 compatible I/O expanders (i.e., PCA9555, PCA9535, and PCA9539 or MAX7311). See the Phillips PCA9555 data sheet for details on the operation of this device.

The switch supports up to four external I/O expanders numbered 0, 1, 2, and 4.

- I/O expanders 0 and 1: hot-plug I/O signals
- I/O expander 2: power good inputs
- I/O expander 4: link status and activity LED control

During switch initialization the SMBus/I²C-bus address allocated to each I/O expander used in that system configuration should be written to the corresponding I/O Expander Address (IOE[0,1,2,4]ADDR) field. The IOE[0,1,2]ADDR fields are contained in the I/O Expander Address 0 (IOEXPADDR0) register while the IOE[4]ADDR fields are contained in the SMBus I/O Expander Address 1 (IOEXPADDR1) register.

Hot-plug outputs and I/O expanders may be initialized via serial EEPROM. Since the I/O expanders and serial EEPROM both utilize the master SMBus, no I/O expander transactions are initiated until serial EEPROM initialization completes.

Note that the interrupt output pin of I/O expander 0, 1 and 2 are connected to GPIO[2]. The I/O expander interrupt outputs are multiplexed when GPIO[2] pin is configured as alternate function input.

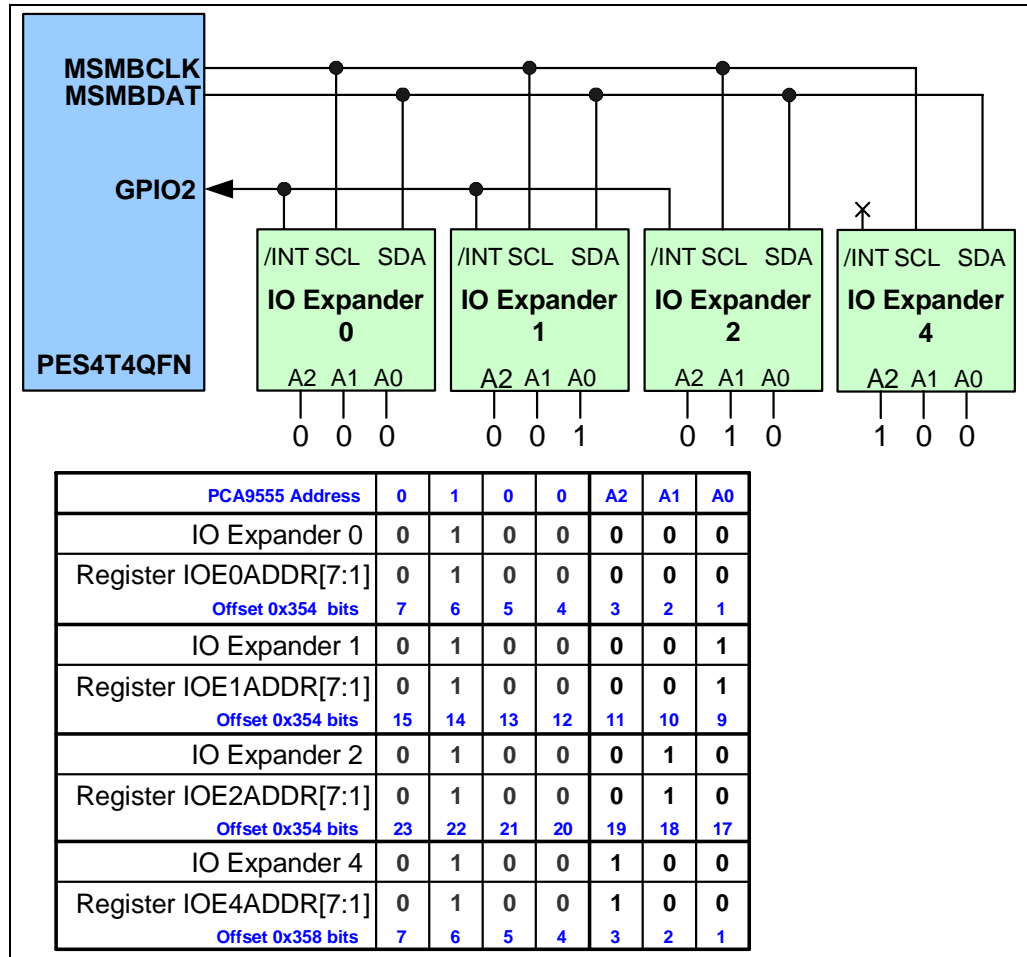


Figure 2 Example of I/O Expander Interface

GPIO and JTAG pins

GPIO pins

The switch has a number of General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. GPIO pins are controlled by the General Purpose I/O Function (GPIOFUNC), General Purpose I/O Configuration (GPIOCFG), and General Purpose I/O Data (GPIOD) registers in the upstream port's PCI configuration space. Please refer to the device datasheet for additional details.

The internal pull-up resistors value for the GPIO pins under typical condition is about 92K ohm.

JTAG pins

The switch provides the JTAG Boundary Scan interface to test the interconnections between integrated circuit pins after they have been assembled onto a circuit board. For details of the interface, please refer to the appropriate switch user manual (see Reference Documents below).

The JTAG_TRST_N pin must be asserted low when the switch is in normal operation mode (i.e. drive this signal low with an external pull-down or control logic on the board if the JTAG interface is not used).

Layout Recommendation

The QFN Footprint is shown in Figure 15. There are total of 132 leads and the four leads on the four corners of row A are not connect (solid black pads in the figure). The center is the thermal pad to ground.

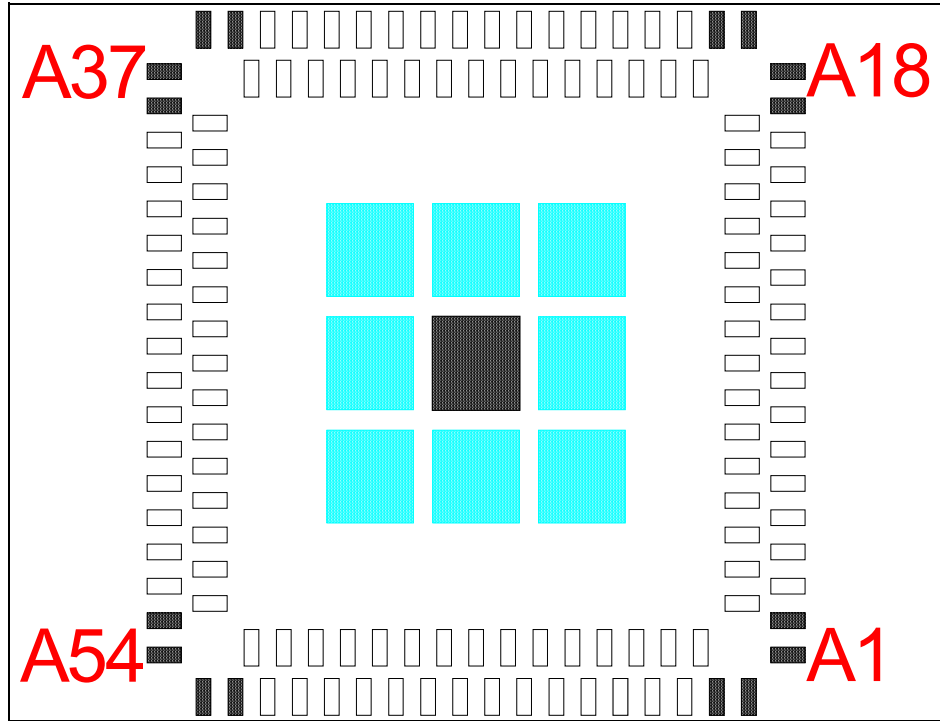


Figure 15 QFN Footprint

QFN Pad/Via Dimension

The package lead dimension is 9 mils x 16 mils. It is recommended to extend the pad length of the inner row leads by 2.5 mils from the center on both sides and 5 mils outward on the outer row to increase solder joint reliability as shown in Figure 16.

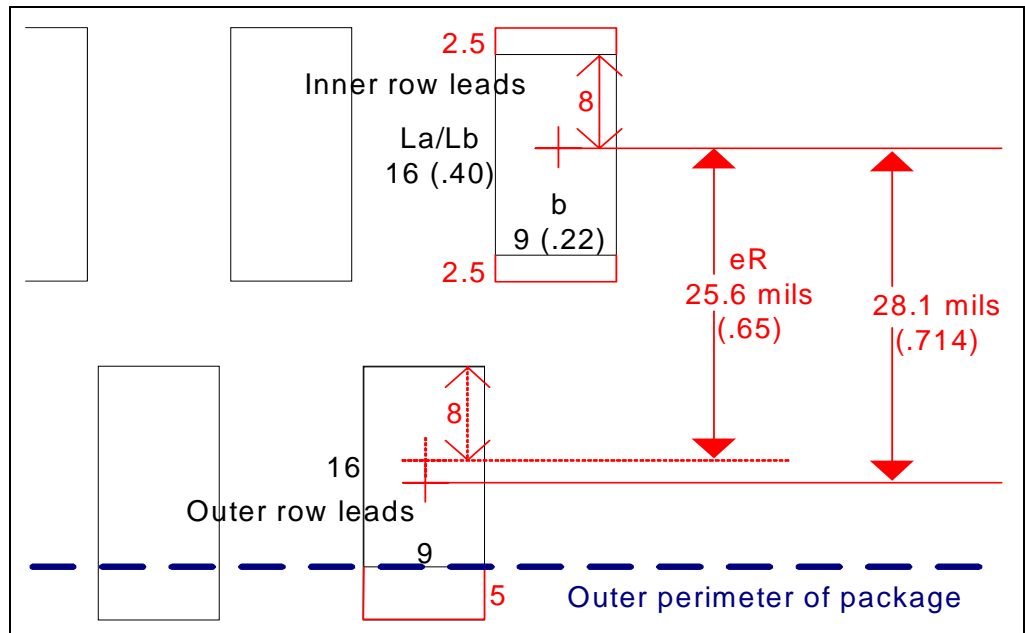


Figure 16 QFN Pad Dimension for Solder Joint Reliability

The dimension of via, pad, and solder mask for the reference design is shown in Figure 17. The pad size is 10 x 21 mils with solder mask of 13 x 25 mils on the reference design. The space between the inner row leads and the thermal pad allows enough room to fit a single row of standard 14 mils Via pad with 8 mils of Via drill to access the inner row pads and avoid the Vias to be in contact with QFN package thermal pad and short to ground.

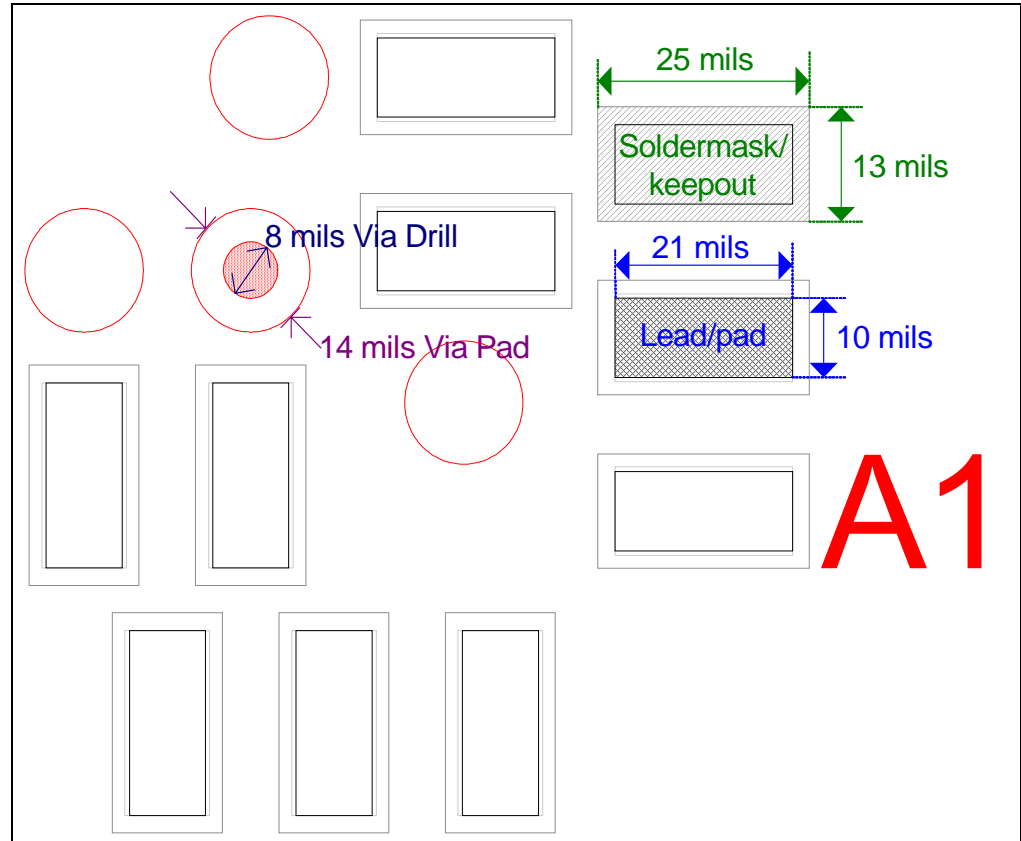


Figure 17 QFN PCB Pad and Via Dimension

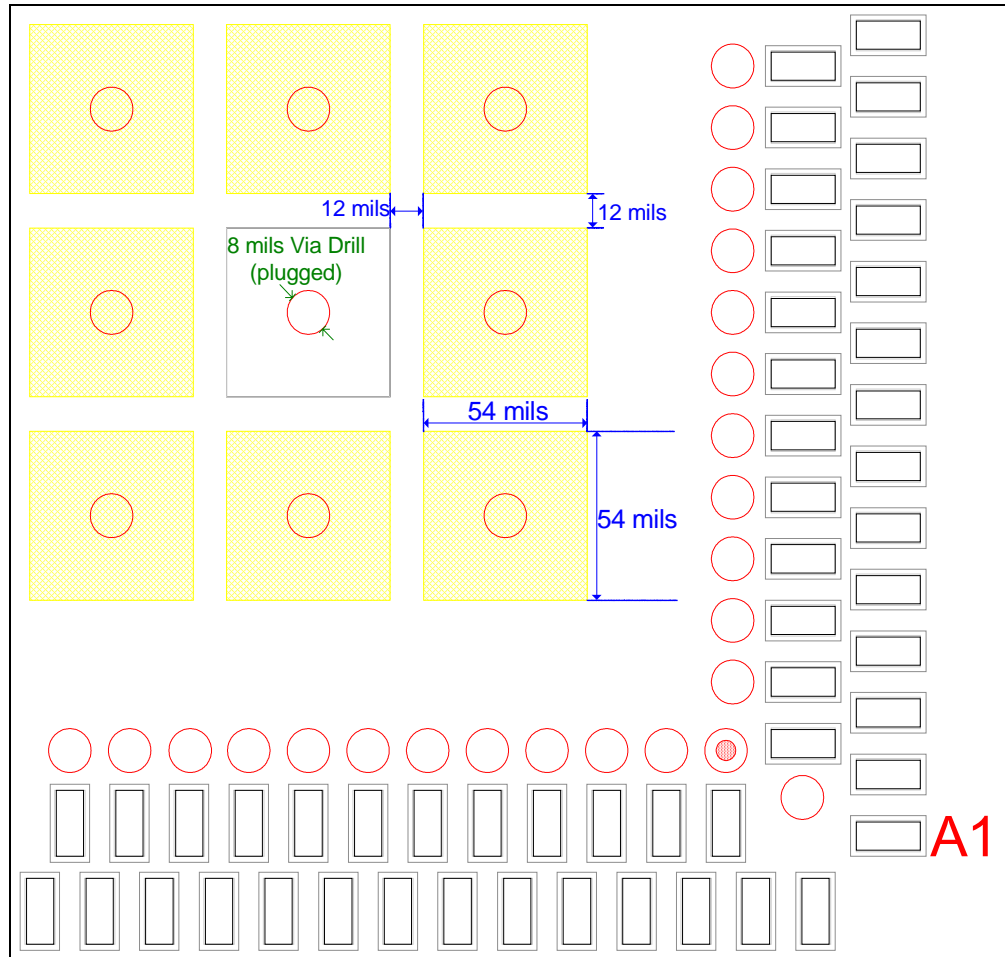


Figure 18 QFN Thermal Pad Dimension

QFN Thermal Pad

Thermal pad size is 6.5mm². However, multiple squares are used as the stencil design for the Thermal Pad to prevent out gassing which may occur during the reflow process and which may cause defects (splatter, solder balling) if the solder paste coverage is too big. The Via must be plugged to further avoid out gassing through Via.

It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the thermal pad region. This will typically result in 50 to 80% solder paste coverage. Shown in Figure 18 are one of the ways to achieve these levels of coverage by nine 54 x 54 mils squares with 12 mils of spacing in between.

Note, the thermal pad connects to Vss/Ground and it is assigned as pin C1 in the reference schematics for layout purpose, however it is optional.

Trace Routing

Routing high speed signals between pads should be avoided to prevent possible shorts as shown in .Figure 19. The high speed differential signal pads can be routed and via to other PCB layer for access as shown in Figure 20 a routing example used in the reference layout.

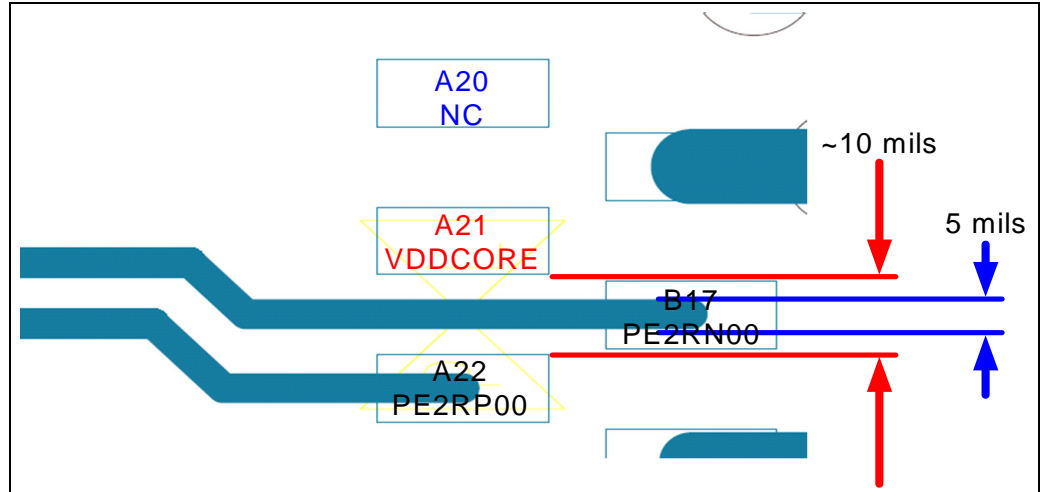


Figure 19 Routing Between Pads

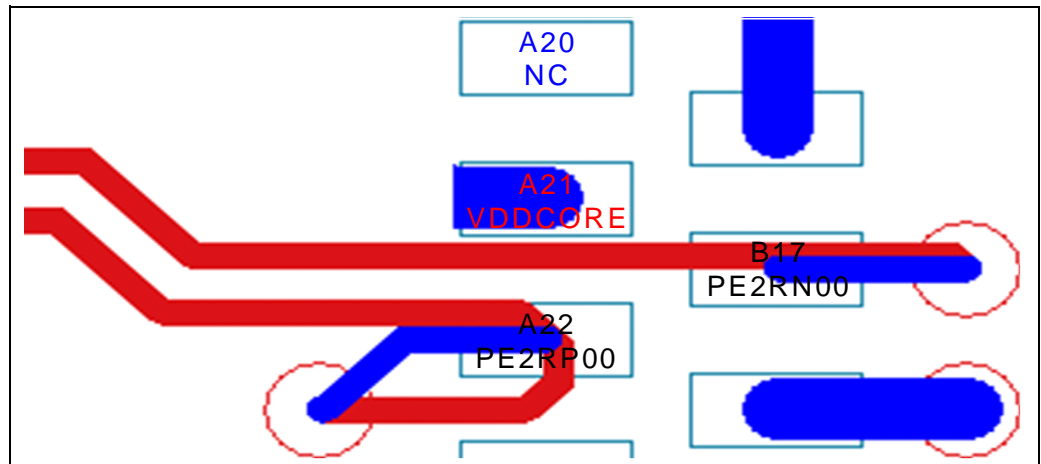


Figure 20 High Speed Differential Routing

Reference Documents

PES4T4 Data Sheet

PES4T4 User Manual

PCI Express Base Specification, Revision 1.1, PCI-SIG

PCI Express Card Electromechanical Specification Revision 1.1, PCI-SIG

PCI to PCI Bridge Architecture Specification, Revision 1.2, PCI-SIG

SMBus Specification, Revision 2.0

Intel PCI Express Electrical Interconnect Design

Revision History

April 18, 2008: Initial publication.

April 21, 2008: Page 15 - 17 are corrected with additional dimension and detail.

June 04, 2008: Added a note in Page 17 explaining C1 pin on the reference schematics.

July 25, 2008: Remove text related to Slave SMBus interface as it is not available to the device. Added high speed differential trace routing guideline.