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# 1. Introduction

The P9221-R Wireless Power Receiver (Rx) is an integrated circuit (IC) consisting of multiple high-power blocks and noise-sensitive circuits controlled by a microprocessor. When implementing the application circuit on a printed circuit board (PCB), there are often tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed on the circuit board based on circuit function to guarantee best performance. The thermal management of the P9221-R is also important to the product's performance and should be optimized when designing the PCB. The following guidance should be used in order to place the components in order of priority based on operation.

There are three main categories of circuitry:

- Power circuits
- Sensitive circuits
- Non-sensitive circuits

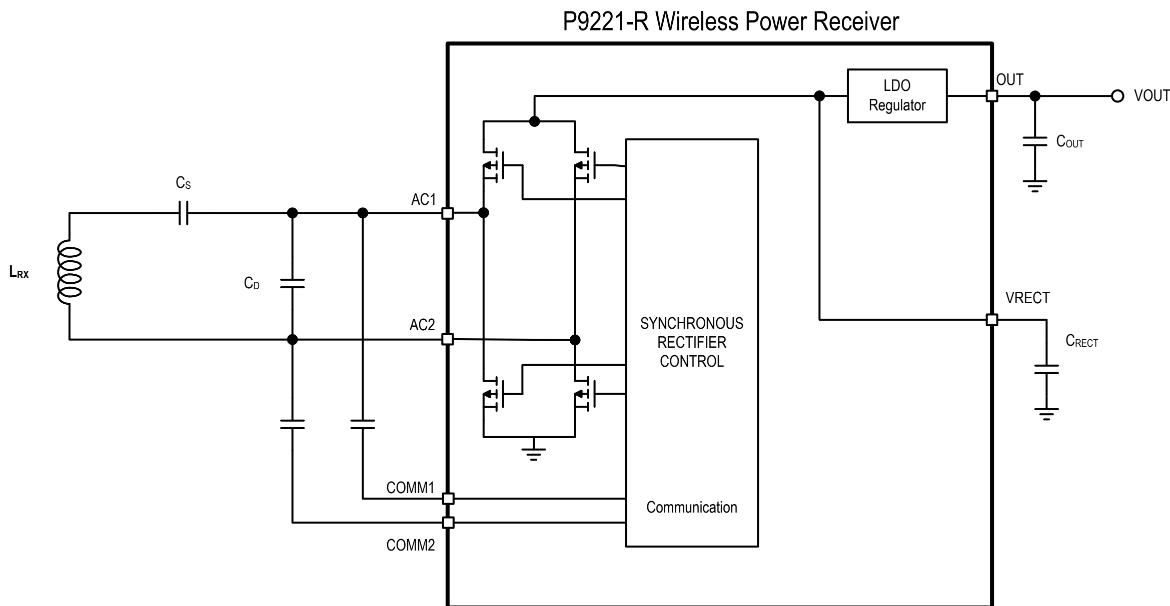
## 1.1 Key Points for Optimal Layout

- Route the power connections wide and on the same side of the PCB as the P9221-R (≥ 100mils).
- Use the layer under the P9221-R side of the board as a solid ground plane.
- Connect all 8 GND pins to the ground plane(s) using via-in-pads. Add a thermal tab for the J-row GND pins.
- Avoid unnecessary layer transitions of the AC power connections (LC node and the VRECT, AC1, AC2, and GND pins).
- Place the P9221-R as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9221-R, including pins that do not carry high current.
- Place components in the following order: Resonance capacitors refer to Figure 1, VRECT pin capacitors, BST pin capacitors, OUT pin capacitors, VDD18 pin capacitors, and VDD5V pin capacitors.
- Use minimal trace-to-trace separation for all traces and planes connected to and within 10mm of the P9221-R.
- Use low ESR resonance capacitors (Cs/Cd) to decrease losses in the LC and AC1 current path (C0G preferred).
- Follow the placement and routing suggestions outlined in the remainder of this document for the specific types of circuits. Refer to the schematics in section 5 for the location of components.

## 2. Rx Power Circuits

The main power circuits of the IDTP9221-R device are the resonance tank, the synchronous bridge rectifier/inverter, and the low drop-out (LDO) linear regulator. Secondary power circuits are the VDD5V and VDD18 regulators.

**Figure 1. P9221-R Power Block**




Recommendation: Once the final shape of the production or development PCB has been determined and the connection points for the power transfer coil ($L_{RX}$) have been chosen, place the P9221-R on the board as close to the center of the PCB as possible, taking into consideration the mechanical requirements of the system under design. Its orientation should be determined based on the ability to route connections and place the required components in the following order of priority: resonance capacitors (refer to Figure 1), VRECT pin capacitors, BST pin capacitors , OUT pin capacitors, communication capacitors, VDD18 pin capacitors, and VDD5V pin capacitors. The main power current path is considered to be the connection from the $L_{RX}$ coil to the AC2 pin and the resonance capacitors to the AC1, GND, VRECT, and VOUT connections. The trace for the power connections should be wide and on the same side of the PCB as the P9221-R (recommended width is ≥ 100mils).The optimal P9221-R orientation relative to the $L_{RX}$ coil and output connector physical locations are shown in Figure 3.

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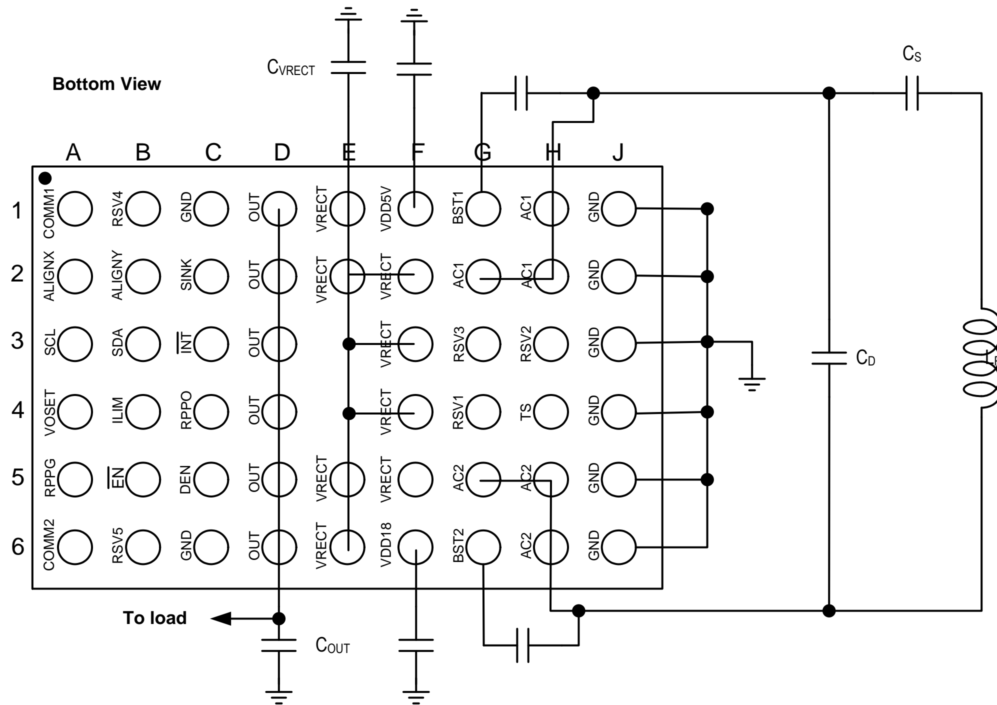
**Figure 2. Recommended Orientation for the P9221-R WLCSP Package**

Note: Not all necessary connections are shown in this figure. Refer to section 5 for a complete diagram of recommended connections. Trace widths not to scale. All GND pins should be connected to GND.




## 2.1 VRECT and OUT Pin Capacitors

Place the VRECT output capacitors close to the pin, since they are subjected to high current charging and power transmission currents at the operating frequency of the power transfer. The power transfer switching results in dV/dt voltage steps high enough for consideration as noise generating signals at the AC1 and AC2 nodes and high current surges during normal operation.

The VRECT capacitors (C21, C22, C23, and C33) and OUT bypass capacitors (C10, C11, and optional C12) must be placed as close as possible to the associated pins. The small 0201 0.1µF capacitor should be placed first, followed by the larger bulk capacitors. It is important to keep the area of the current loop that conducts the AC current from the synchronous bridge rectifier to the VRECT capacitors and GND to a minimum to avoid noise. The copper planes should be as wide as possible for the connections for VRECT from the P9221-R to the capacitors and back to GND.

**Figure 3. P9221-R-EVK Evaluation Board (Top Layer)**

The heat management of the P9221-R design is critical to performance, and from the thermal perspective, it is recommended to route the main power connections as directly as possible to the device. This allows optimal electrical and thermal performance. The main power connections are VRECT, AC1, AC2, VOUT, the Rx coil node (LC node), and GND. These connections should be routed on the same side of the PCB as the P9221-R for maximum thermal benefit (excluding GND, which should be on the closest internal layer and the outer layer opposite to the P9221-R). These traces should avoid multiple layer changes in order to reduce voltage drops and thermal resistance induced by thin via walls. If these traces need to transfer layers, it should be accomplished using multiple vias that have enough spacing such that they do not block the current path leading up to the via.

The copper shape with 22 thermal vias is an important connection and layout improvement because it assists with current conduction and dramatically improves the P9221-R thermal performance as shown in Figure 3. Vias-in-pad for GND pins and the thermal tab are recommended for all layouts.

**Figure 4. P9221-R-EVK Evaluation Board (Second Layer)**

**Figure 5. P9221-R-EVK Evaluation Board (3rd Layer)**

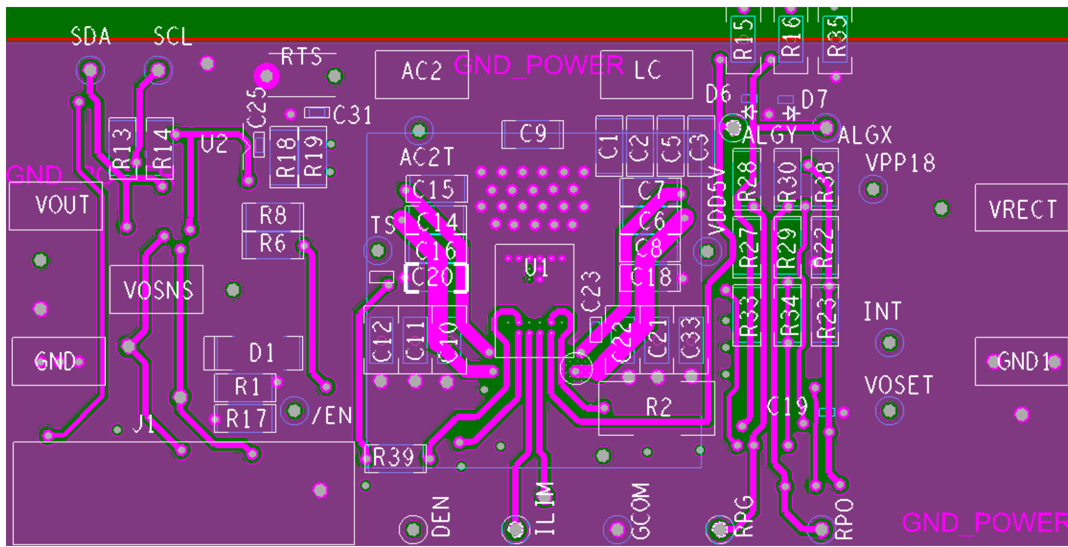
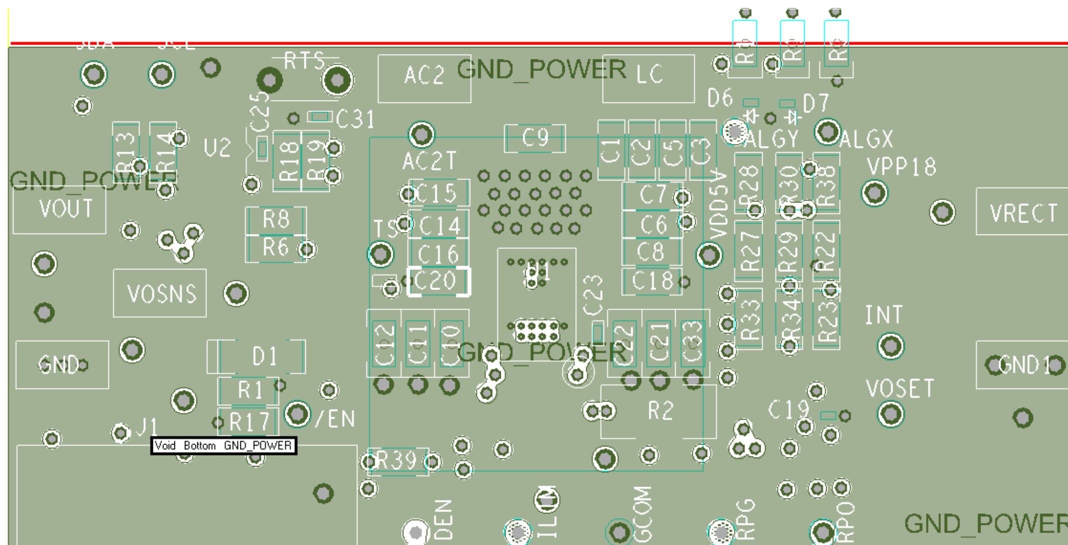



**Figure 6. P9221-R-EVK Evaluation Board (Bottom layer)**




The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. Spreading the heat into internal layers is also effective for lowering the operating temperature since the thickness of the PCB allows the thermal resistance of the FR-4 material to have fairly small resistance to heat flow along the z-axis. Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being close to the same temperature; however, in order to obtain this result, all board layers should have planes that are fairly continuous and in direct contact with the P9221-R via-in-pads. A single internal layer should be selected for routing the majority of the inner row/column pins to the rest of the PCB. The third layer is preferred for this purpose. The required nodes for connecting heat spreading planes are GND, VRECT, AC1, AC2, and OUT. The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9221-R.

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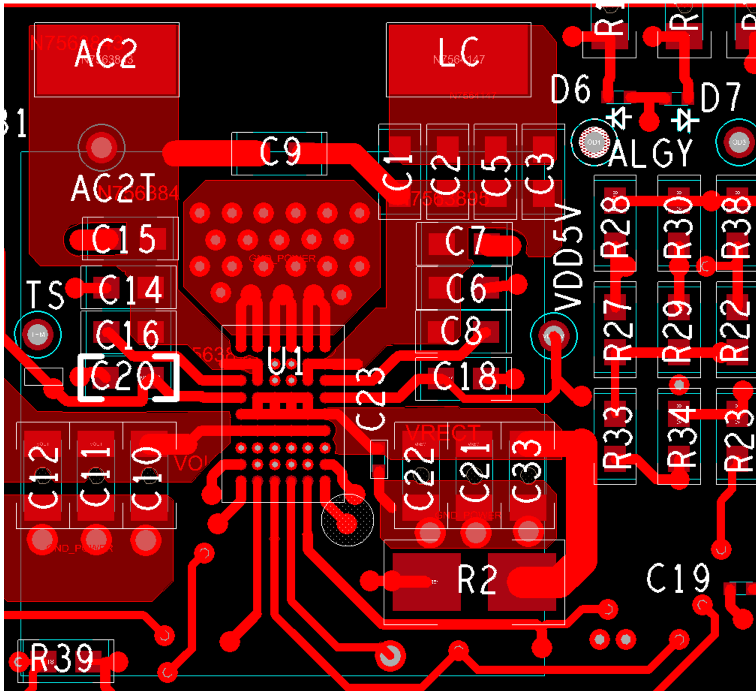
## 2.2 Communication and Resonance Capacitors

The communication capacitors (C6, C14), and resonance capacitors (C1, C2, C3, C5, C9) should be placed on the same layer as P9221-R. The resonance capacitors should be close to the P9221-R and have fairly direct connections to the respective pins (route 12 to 20 mils wide). The resonance capacitors should have wide copper planes connected to them (at least 50 mils) and be in-line from the P9221-R to the Rx coil. The C0G type capacitors will offer the highest performance and are highly recommended. The X7R and X5R type capacitors can be substituted. However, low-ESR capacitors should be utilized. Since all the load current and the current required to charge the VRECT/VOUT capacitors flows through the resonance capacitors, the heat developed within the resonance capacitors (Class II only) should be given opportunity to spread into large copper planes.

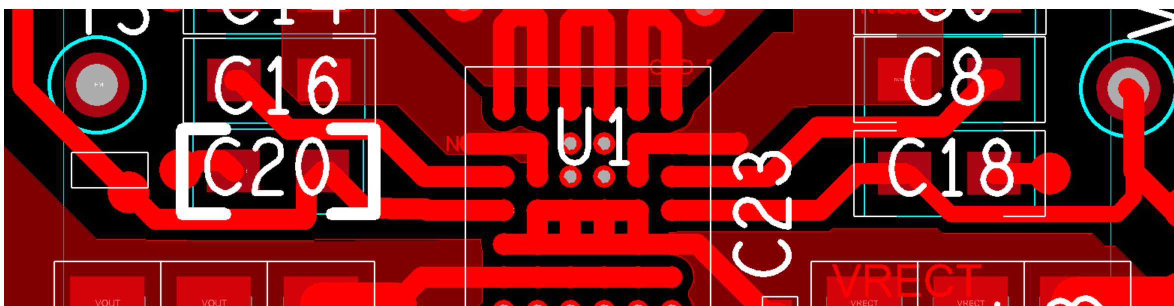
**Figure 7. Communication and Resonance Capacitors**




## 2.3 VDD18 and VDD5V Pin Capacitors

The VDD5V and VDD18 pin capacitors (C20 and C18) are used to stabilize the internal linear regulators. These capacitors must be located close to the P9221-R.

**Figure 8. VDD18 and VDD5V Pin Capacitors**

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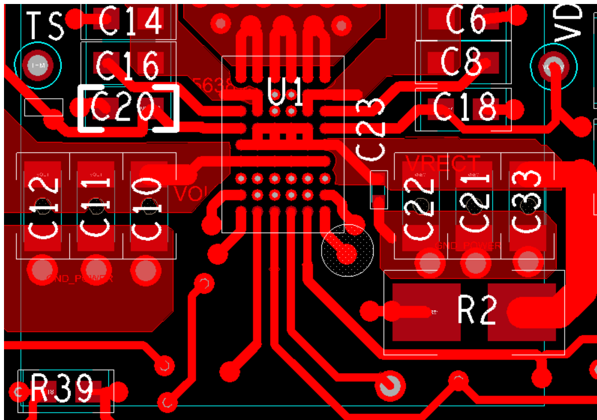
## 2.4 SINK

The SINK connection to the VRECT node is used to provide DC clamping of the rectifier output voltage during transient events. A 1/2W, 36Ω resistor (R2) must be located close to the P9221-R. Optimal placement is directly connected to the VRECT node and routed to the SINK pin using a trace width of at least 12mils. This is the primary VRECT clamping mechanism and must be connected at all times.

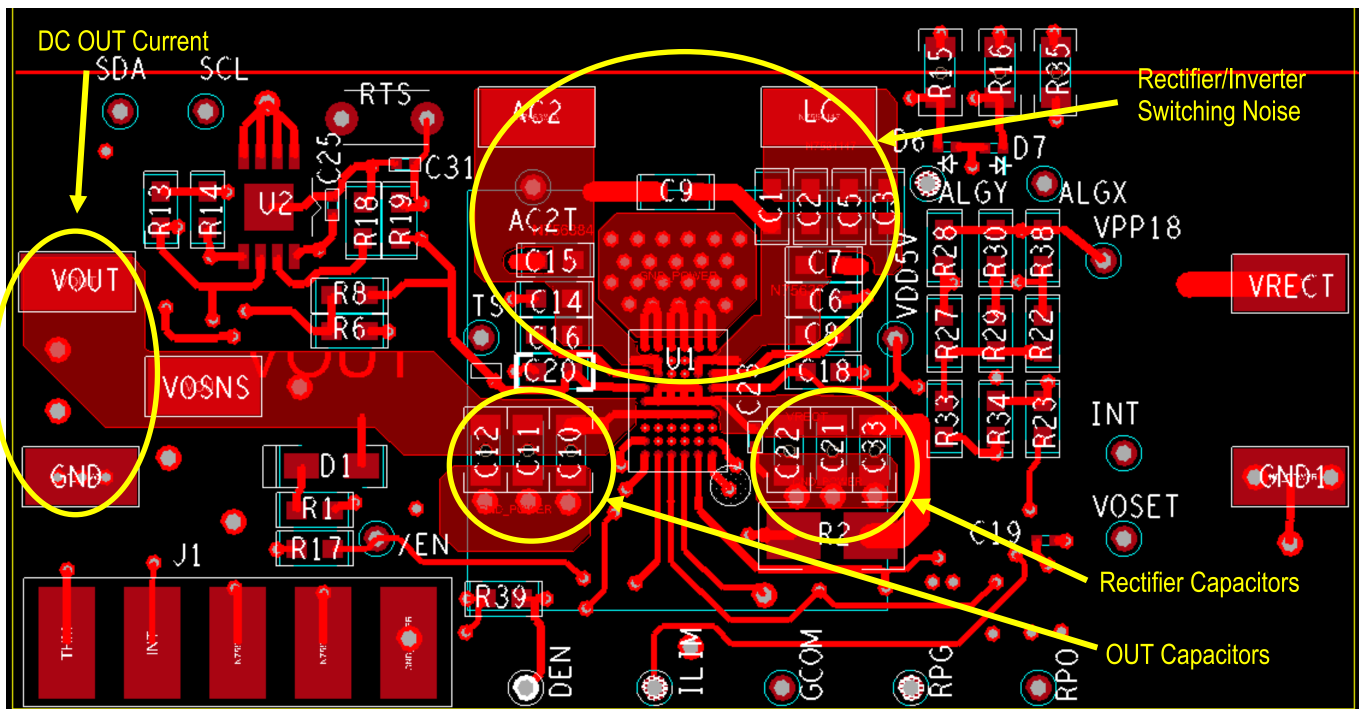
**Figure 9. SINK Connection to VRECT**




## 2.5 Sensitive Circuits

The term “sensitive circuits” refers to noise-sensitive circuits that should be referenced to GND in the “quiet” ground area; see Figure 10. AC coupling, the thermistor bypass capacitors, and other capacitors are for decoupling noise. In order to optimize the signal-to-noise performance, it is recommended that the OUT pin capacitors be placed on the side of the P9221-R closest to the OUTPUT/INPUT voltage connector and that the rectifier capacitors be placed on the opposite side of the P9221-R. The rectifier and resonance nodes generate the highest harmonic noise, which must be filtered with decoupling capacitor.

**Figure 10. IDTP9221 Typical GND Noise Areas**

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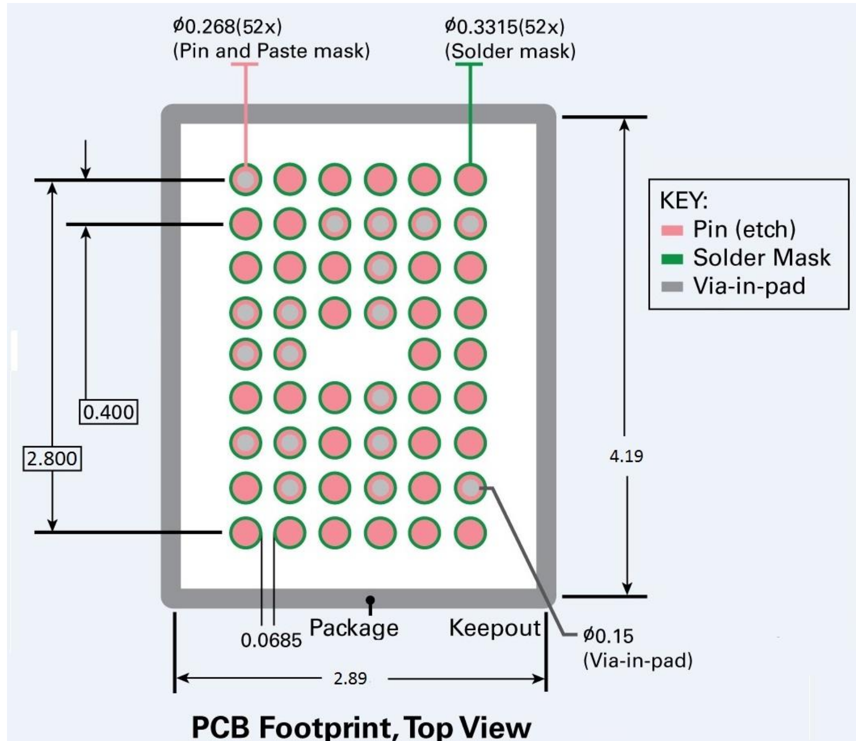
# 3. PCB Footprint Design

The P9221-R package is a fine-pitch WLCSP package. Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin-to-board connections. In order to minimize the risk of such events, it is recommended that the PCB pin pads and via-in-pads be designed using the following guidance. Non-solder mask defined pins are recommended, and solder paste should be applied with stencil openings of 0.127mm to 0.268mm (recommendation: 0.19mm typical) based on stencil thickness and solder paste selected. The pin diameter should be set to 0.268mm, the solder mask should be 0.3315mm, and via-in-pads should be 0.127mm diameter holes.

**Figure 11. P9221-R Recommended PCB Footprint Dimensions**



# 4. Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. Some of the sources of the audible noise have been identified to be: the rectifier capacitors, the Rx coil ferrite and communication capacitors. Typically, the rectifier capacitors are the biggest culprit of the audible noise. This is due to the WPC communication signals being generating in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB. The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions, contact IDT technical support (see last page for contact information).

# 5. Schematics, Bill of Materials (BOM), and Board Layout

**Figure 12. Application Schematics**

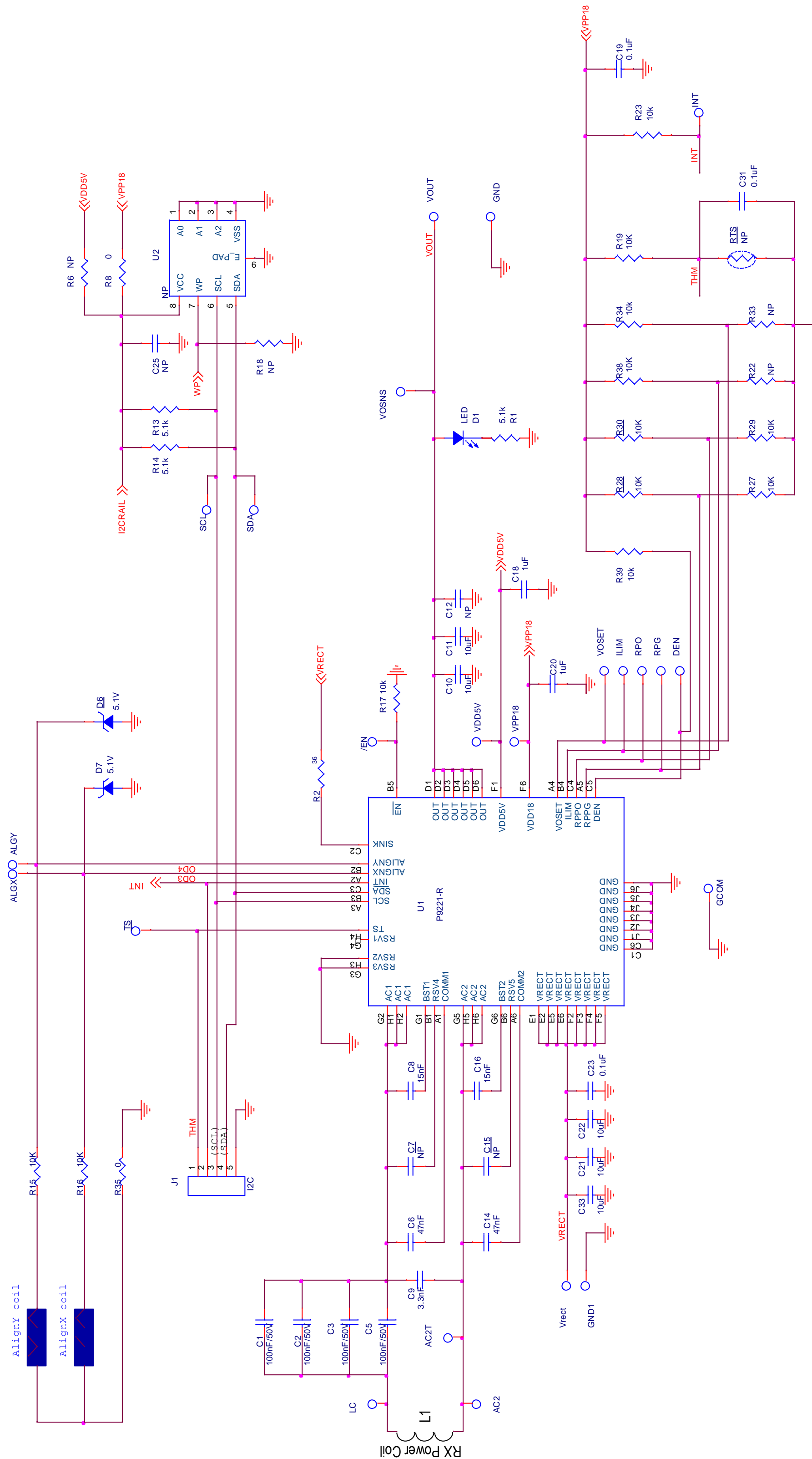


**Table 1. Application Board Bill of Materials (BOM)**

| Item | Reference | Quantity | Value | Description | Part Number | PCB Footprint |
|---|---|---|---|---|---|---|
| 1 | AC2T, VDD5V, VPP18, VOSET, TS, SDA, SCL, RPO, RPG, /INT, ILIM, GCOM, DEN, ALGY, ALGX, /EN | 16 | PTH_TP | Test Pad | | 10MIL_35PAD |
| 2 | AC2, LC | 2 | NP | Test Point | | test_pt_sm_135x70 |
| 3 | C1, C2, C3, C5 | 4 | 100nF/50V | CAP CER 0.1UF 50V X5R 0402 | GRM155R61H104KE19D | 402 |
| 4 | C6, C14 | 2 | 47nF | CAP CER 0.047UF 50V X7R 0402 | C1005X7R1H473K050BB | 402 |
| 5 | C7, C15 | 2 | NP | CAP CER 0.047UF 50V X7R 0402 | C1005X7R1H473K050BB | 402 |
| 6 | C8, C16 | 2 | 15nF | CAP CER 0.015UF 50V X7R 0402 | GRM155R71H153KA12J | 402 |
| 7 | C9 | 1 | 3.3nF | CAP CER 3300PF 50V X7R 0402 | CL05B332KB5NNNC | 402 |
| 8 | C10, C11, C21, C22, C33 | 5 | 10µF | CAP CER 10UF 25V X5R 0603 | CL10A106MA8NRNC | 603 |
| 9 | C12 | 1 | NP | CAP CER 10UF 25V X5R 0603 | CL10A106MA8NRNC | 603 |
| 10 | C18 | 1 | NP | CAP CER 1UF 10V X5R 0402 | GRM155R61A105KE15D | 402 |
| 11 | C20 | 1 | 1µF | CAP CER 1UF 10V X5R 0402 | GRM155R61A105KE15D | 402 |
| 12 | C19, C25, C31 | 3 | 0.1µF | CAP CER 0.1UF 10V X5R 0201 | C0603X5R1A104K030BC | 201 |
| 13 | C23 | 1 | 0.1µF | CAP CER 0.1UF 25V X5R 0201 | CL03A104KA3NNNC | 201 |
| 14 | D1 | 1 | LED | LED GREEN CLEAR 0603 SMD | 150060GS75000 | 0603_diode |
| 15 | D6,D7 | 2 | 5.1V | DIODE ZENER 5.1V 100MW 0201 | CZRZ5V1B-HF | 201 |
| 16 | GND1, VRECT, VOUT, VOSNS, GND | 5 | Test Point | TEST POINT PC MINIATURE SMT | 5015 | test_pt_sm_135x70 |
| 17 | L1 | 1 | RX coil | AMOTECH, Rx Power Coil | ASC-504060M22-S00 | 10MIL_35PAD |
| 18 | J1 | 1 | NP | HEADER_1X5_0P1PITCH60P42D | 68002-205HLF | header_1x5_0p1Pitch60p42d |
| 19 | RTS | 1 | NP | | | NTC2 |
| 20 | R1, R13, R14 | 3 | 5.1k | RES SMD 5.1K OHM 5% 1/16W 0402 | MCR01MRTJ512 | 402 |
| 21 | R2 | 1 | 36 | RES SMD 36 OHM 5% 1/2W 0805 | ERJ-P06J360V | 805 |
| 22 | R6 | 1 | NP | RES SMD 0.0OHM 1/10W 0402 | ERJ-2GE0R00X | 402 |
| 23 | R8 | 1 | 0 | RES SMD 0.0OHM 1/10W 0402 | ERJ-2GE0R00X | 402 |
| 24 | R15, R16 | 2 | 10K | RES SMD 10KOHM 1% 1/10W 0603 | RC0603FR-0710KL | 603 |
| 25 | R17, R19, R23, R27, R28, R29, R30, R34, R38, R39 | 10 | 10k | RES SMD 10K OHM 5% 1/10W 0402 | ERJ-2GEJ103X | 402 |
| 26 | R18, R22, ,R33 | 3 | NP | RES SMD 10K OHM 5% 1/10W 0402 | ERJ-2GEJ103X | 402 |
| 27 | R35 | 1 | 0 | RES SMD 0.0OHM JUMPER 1/10W 0603 | MCR03EZPJ000 | 603 |
| 28 | U1 | 1 | P9221-R | Wireless power receiver | P9221-R | csp52_2p64x3p94_0p4mm |
| 29 | U2 | 1 | NP | IC EEPROM 128KBIT 400KHZ 8TDFN | 24AA128T-I/MNY | TDFN08 |

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**Figure 13. Silkscreen – Top of Board**

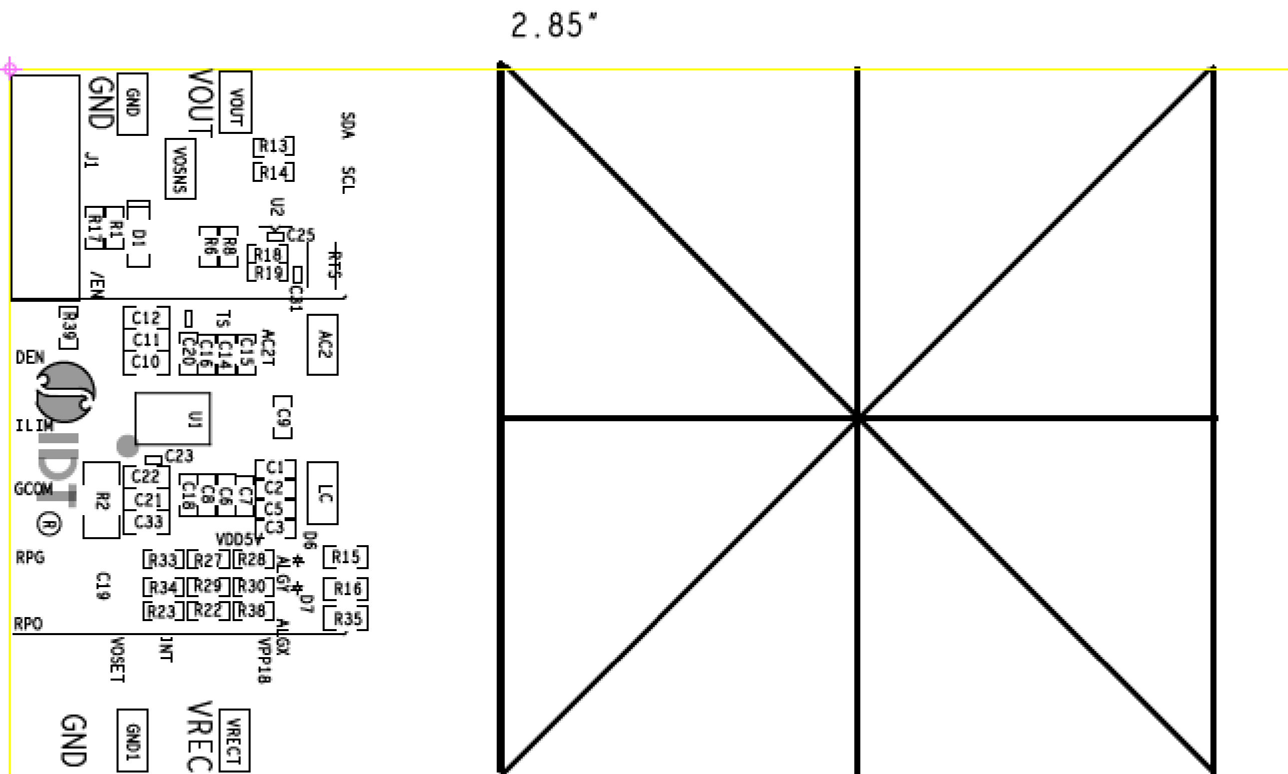



**Figure 14. Silkscreen – Bottom of Board**

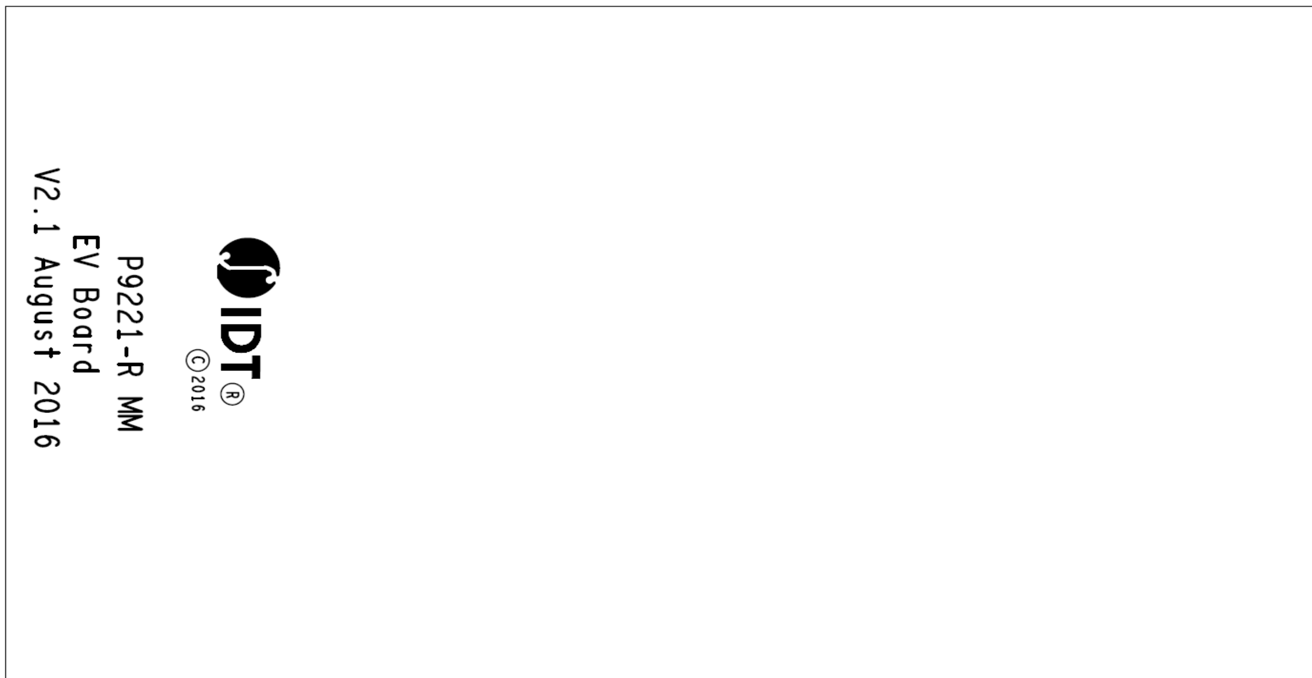


**Figure 15. Copper – Top Layer**

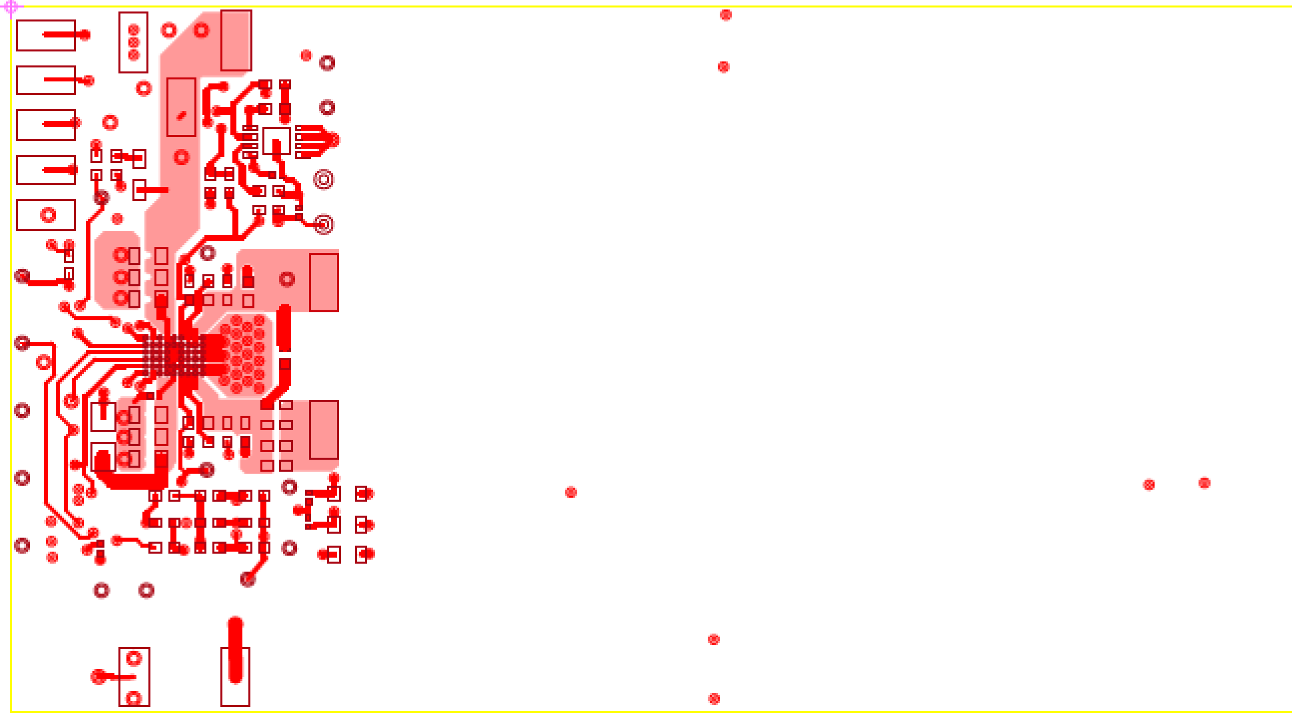


**Figure 16. Copper L2 Layer**

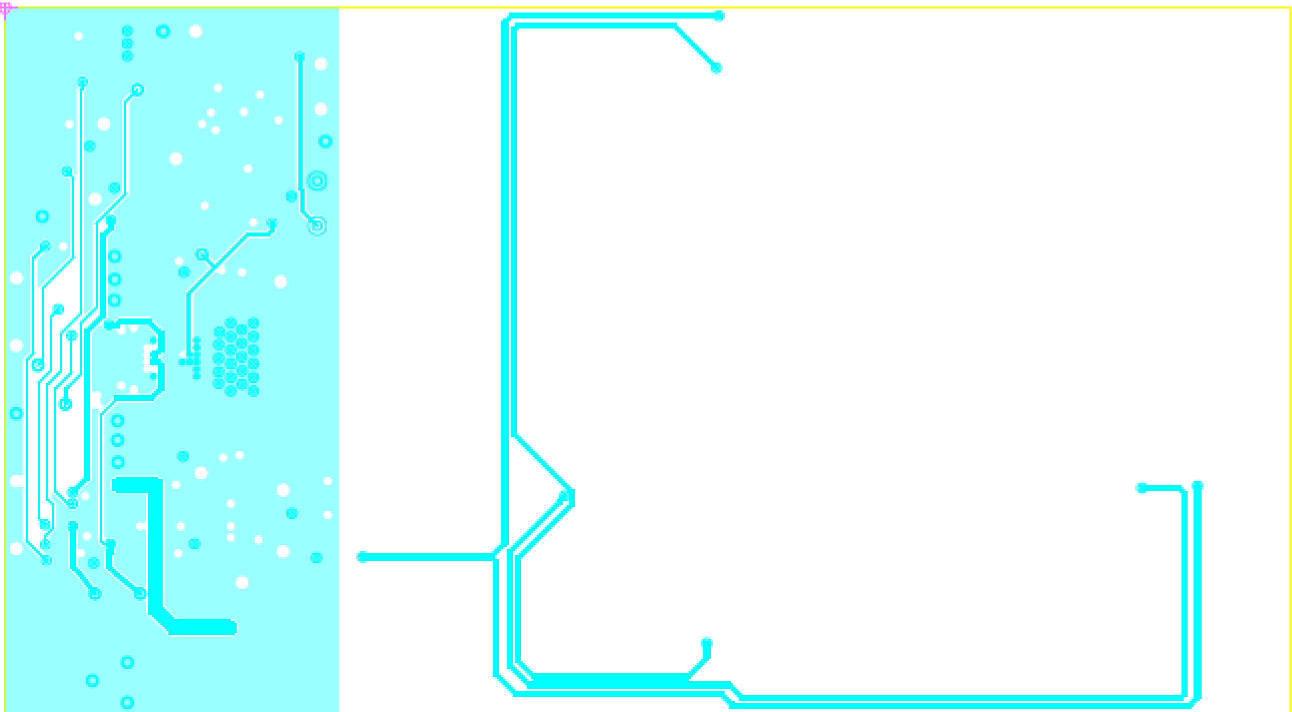


**Figure 17. Copper L3 Layer**

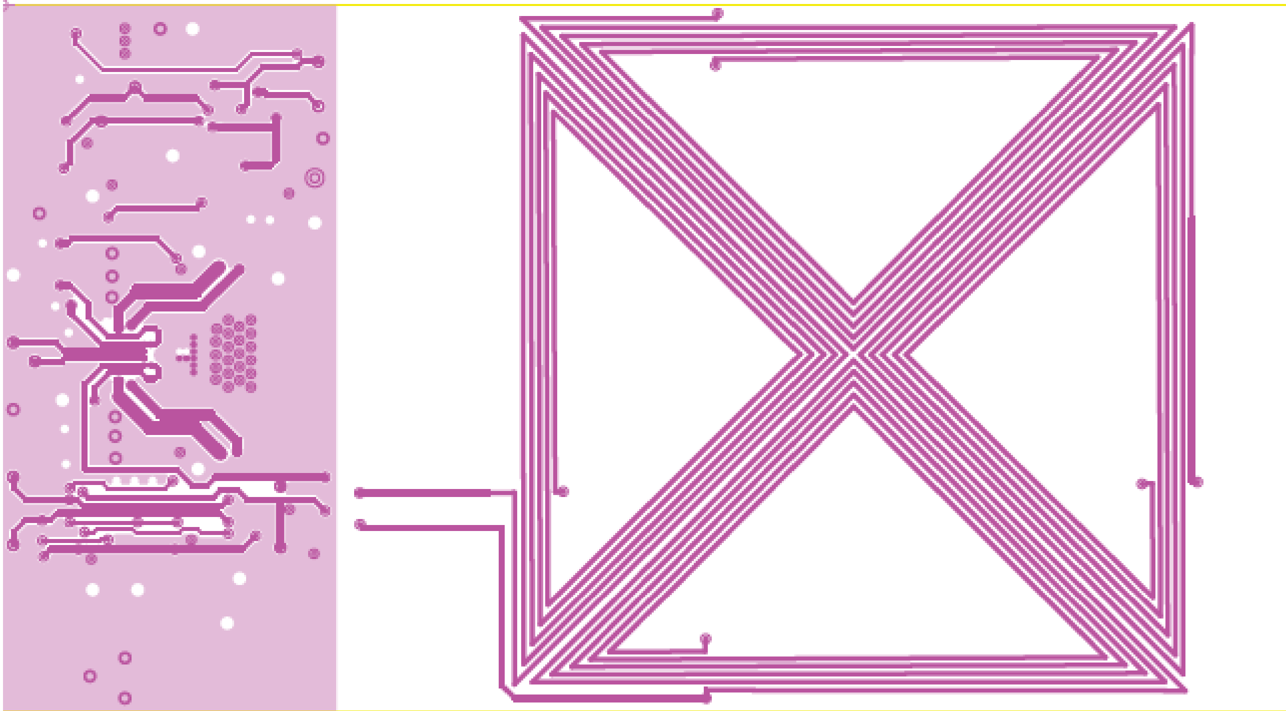
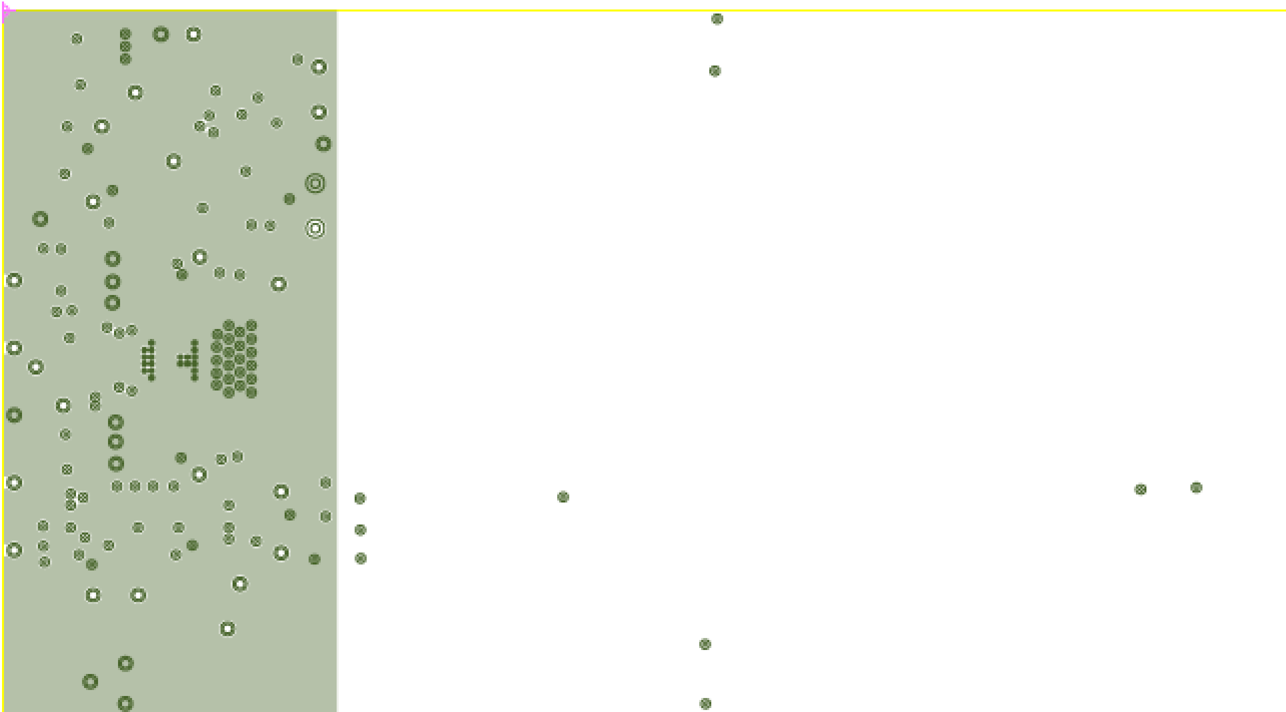


**Figure 18. Copper Bottom**



# 6. Revision History

| Revision Date | Description of Change |
|---|---|
| December 22, 2016 | Initial release of document. |

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