P9242-R Layout Guidelines

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1. Introduction

The P9242-R Wireless Power Receiver (Tx) is an integrated circuit (IC) consisting of multiple high-power blocks and noise-sensitive circuits controlled by a microprocessor. When implementing the application circuit on a printed circuit board (PCB), there are often tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed on the circuit board based on circuit function to guarantee best performance. The thermal management of the P9242-R is also important to the product’s performance and should be optimized when designing the PCB. The following guidance should be used in order to place the components in order of priority based on operation.

There are three main categories of circuitry:
- Power circuits
- Sensitive circuits
- Non-sensitive circuits

1.1 Key Points for Optimal Layout

- Route the power connections wide and on the same side of the PCB as the P9242-R (≥ 100mils).
- Use the layer under the P9242-R side of the board as a solid ground plane.
- Connect the exposed thermal pad (EP) in the center of the P9242-R to all other layers with an array of 4x5 10 mil vias.
- Avoid unnecessary layer transitions of the AC power connections (LC node, LC tank driving FETs, and GND).
- Place the P9242-R as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9242-R, including pins that do not carry high current.
- Use low ESR resonance capacitors (Cs/Cd) to decrease losses in the LC and AC1 current path (C0G preferred).
- Place components in the following order:
  - POWER CIRCUITS – NON H BRIDGE POWER STAGE:
    - CIN, CBOOST: Place all IC pin input voltage capacitors and boost capacitors close to their related pins (VIN, LDO33, LDO18, VDDIO, BST_BRG1, BST_BRG2, DRV_VIN, VBRG_IN).
    - Buck Regulator L, Cout: Place the inductor as close as possible to the switch node pin to reduce the switching noise of that node. Place the buck regulator inductance and output capacitance such that they form the smallest possible current loop to minimize EMI transmissions.
  - SENSITIVE CIRCUITS – VOLTAGE AND CURRENT MEASUREMENT:
    - Current Sense: Place the bridge input current sense resistor directly in the current path to the tank FET drivers. Place the filtering components close to the sense resistor and tightly together.
    - Current Demodulation: Place the current demodulation circuit components tightly together and close to their related IC pins (ISNS_OUT, IDEMI).
    - Voltage Demodulation: Place the voltage demodulation circuit components tightly together and close to their related IC pin (VDEM1).
    - Q Measurement: This circuit lowers the voltage to the LC tank during Q measurement (for FOD detection purposes). The circuit consists of the resistor divider R45, R33 which reduce the Vin and Q6. Q6 shorts out the Vin-to-LC-tank resistor during normal operation. Place the R45, the top of the resistor divider, directly above the FET it is connected to (Q2). Place R33 directly below the FET. Make these traces wide and short to avoid corrupting the Q measurement.
  - POWER CIRCUITS – H BRIDGE POWER STAGE:
    - H Bridge: Place H bridge FETs (Q1, Q4) and LC tank capacitance (C20, C23, C24, C25) close to each other, to form a small current loop, to avoid EMI emissions.
    - H Bridge Cin: Place the V_BRG FET-H-Bridge capacitors such that the traces are short. This is the large DC and AC current path.
  - SENSITIVE CIRCUITS – FET GATE DRIVER COMPONENTS:
    - Gate driver circuit: Place the Low Side FET Gate and High Side Gate Rs close to their respective pins (GH_BRG1, 2, GL_BRG1, 2) and connect the Output RC Snubbers directly onto their respective the H Bridge switch nodes.
    - Gate driver traces: Running under the H Bridge switch nodes should be avoided. Run these traces under the relatively quiet VBRG node instead. Place a ground layer between these traces and the top signal level. Surround these traces with the ground plane to provide a tight loop AC signal return path to avoid EMI noise.
2. Tx Power Circuits

The main power circuit of the P9242-R device includes the current sense resistor, the four FETs of the H bridge resonant tank driver, and the resonant tank. Secondary power circuits are the VCC5V, LDO33, and LDO18 regulators.

Figure 1. Schematic with Main Power Path (Orange) and Main (Noisy) AC Power Loops (Red)
Recommendation: Once the final shape of the production or development PCB has been determined and the connection points for the power transfer coil (L_Tx) have been chosen, place the P9242-R on the board as close to the center of the PCB as possible, taking into consideration the mechanical requirements of the system under design. Its orientation should be determined based on the ability to route connections and place the required components in the following order of priority. First place the input and boost capacitors as close to their respective pins in this order of priority: VIN, LDO33, LDO18, BST_BRG1, BST_BRG2, DRV_VIN, and VBRG_IN. The main power current path the connection from VIN through the sense resistor (R_SNS), through 1 of the two half bridge power FETs (FETH_BRG1,1B), through the tank capacitor (Ctank), through the Tx coil (Coil Assembly) and out through 1 of the other half bridge power FETs (FETH_BRG2,2B). The above figure represents the optimal orientation of the P9242-R relative to the other main components. Not all necessary connections are shown in this figure. For a complete diagram of the recommended connections, see the schematic in Section 5. Trace widths are not to scale.
Figure 3. Actual Placement for the P9242-R EVK. Select Critical Components are Circled in Yellow

There are many things to take note of on this top layer with respect to creating an optimal layout (notes refer to the listing embedded in Figure 3):

- Closeness of Cin and Cboost caps to their respective pins (notes 1,6,15)
- Tight (small) AC loops of FETs in relation to the LC tank (notes 9-12)
- Tight loops of the FETs in relation to the H bridge Cin capacitors (notes 9,10)
- Closeness of current and voltage demodulation to the IC (notes 5,13)
Closeness of H bridge FET gate driver resistors to the IC (note 14)
Tight loop of LC of 5V switching regulator for low loop inductance/noise (note 2)
Closeness of L to its respective switching node for minimum noise (note 2)
The H bridge FETs produce the most heat. Therefore, FET GND pads are connected to GND with the maximum number of 10mil vias for the best thermal performance.

Figure 4. P9242-R Physical Layout from P9242-R-EVK Evaluation Board (2nd Layer (L1)), Solid GND Plane with Minimal Connections, Direct Contact to GND Plane 10mil Vias for Thermal Transfer

Note: The ground layer (L1) is between the top layer signal plane and layer 3 (second middle layer - L2) gate drive signal layer below.
Figure 5. P9242-R Physical Layout from P9242-R-EVK Evaluation Board of 3rd Layer (L2), Gate Driver Traces under Vin, GND Planes (Quiet Planes), Thick Power Traces, and Ground Plane with Minimal Traces especially around the P9242-R

Note: Routing of the FET gate driver lines away from switching nodes as much as possible (note 1). The traces are routed under the Vin and GND planes (electrically quite areas). Also note the thick 30mil traces for the supply voltages (5V-note 2,4; LDO33-note 5) and for the step down switching regulator’s switch node (note 3). These thick traces prevent voltage drops when delivering the power, increasing reliability and efficiency.
The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. Spreading the heat into internal layers is also effective for lowering the operating temperature. Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being close to the same temperature; however, in order to obtain this result, all board layers should have planes that are fairly continuous and in direct contact with the P9242-R thermal vias.

A single internal layer should be selected for routing the majority of the inner row/column pins to the rest of the PCB. The third layer is preferred for this purpose. The required nodes for connecting heat spreading planes are GND, the Vin sources to the H bridge (V_BRIDGE, drain of Q2), and the switch nodes (VLX1, VLX2). The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9242-R.
2.1 Resonance Capacitors

Next, the resonance components should be placed. The C20, C23, C24, C25, and C9 capacitors should have wide copper planes connected to them and be in-line from the P9242-R to the Tx coil. CGG capacitors will offer the highest performance and are recommended. X7R and X5R can be substituted, but low-ESR components should be used. Since all the load current and the current required to transmit energy to the receiver flows through the resonance capacitors, the heat developed within the resonance capacitors (Class II only) should be given opportunity to spread into large copper planes.

Figure 7. Resonance Capacitors
2.2 VCC5V VIN, VCC5V, LDO33, LDO18, VBRG_IN, and DRV_VIN Pin Capacitors

The VCC5V node, VIN, LDO33, LDO18, VBRG_IN, and DRV_VIN pin capacitors (C5, C4, C15, C14, C16, C21, C6, C13, C29, C30, C31) are used to stabilize internal voltage supplies used for normal operation. These capacitors must be located close to the P9242-R. A 10µF decoupling capacitor is recommended to be placed as close as possible to GND from the VIN, VCC5V, and DRV_VIN nodes. A 1µF decoupling capacitor is recommended for LDO33 and LDO18 regulated output pins. A 0.1µF capacitor is also recommended in parallel with aforementioned decoupling capacitor. This will reduce the ESR of the decoupling which will reduce noise at the pin. VBRG_IN requires a 0.1µF capacitor only.

Figure 8. VIN, VCC5V, LDO33, LDO18, VBRG_IN, and DRV_VIN Pin Capacitors Placed Close to P9242-R with 0.1µF Placed Closest

1: Cin (C14,15)
3: Cout,ldo33 (C16,21)
4: Cout,ldo18 (C6,13)
6: Cdrv,vin (C30,31)
2.3 Sensitive Circuits

The term “sensitive circuits” refers to noise-sensitive circuits that should be referenced to GND in the “quiet” ground area. AC coupling, the thermistor bypass capacitors, and other capacitors are for decoupling noise. The resonance nodes generate the highest harmonic noise, which must be filtered with decoupling capacitor. Place the current sense circuitry, the voltage demodulation circuitry, and the current demodulation circuitry, in quiet ground areas away from the resonance nodes.

**Figure 9. P9242-R Typical GND Noise Areas and Sensitive Circuit Placement**

SENSITIVE CIRCUITS:
- 5: Isns, demodulation (C7,8,9,R6)
- 8: Input Current Sense (R15,18,21,C27)
- 13: Peak Detector / Vsns demodulation (D1,R11,13,14,C17,19,22)

NOISY AREAS:
- 11: Tank Resonance Caps Switch Node (C20,23,24,25)
- 12: Tank Resonance Coil Switch Node (attached to LX1)
2.4 Boost Capacitors and Gate Drive Lines

Place the boost capacitors (C33, C34) close to their respective pins for maximum transfer of the capacitive energies. Place the gate driver resistors (R25, R27, R29, R28) close to their respective pins. This limits the switching noise generated. Place the FET gate bleed resistors (R26, R32, R30, R31) close to their respective FET gate pad/pin.

14: FET Gate Driving Rs (R25,27,28,29)
14a: FET Gate Bleeding Rs (R26,32,30,31)
15: Cboost (C33,34)
2.5 5V Step Down Switching Regulator

Keep the switch node small by moving the inductor close to the switch node. This is only after placing all Cin capacitors as close to their respective pins as possible. Make the L, Cout loop small to limit the loop inductance and related noise. Place the Cout such that the ground end of the capacitor is close to the nearest ground pin (pin 6).
3. PCB Footprint Design

The P9242-R package is a fine-pitch 48-VFQFN device.

Figure 10. P9242-R Recommended PCB Land Pattern Drawing
4. Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source (i.e., the rectifier capacitors, the Tx coil ferrite, communication capacitors). Typically, the rectifier capacitors are the components that generate the audible noise. The reason the noise is present and associated with the rectifier capacitors is due to the WPC communication signals being generated in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB.

The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions, contact IDT technical support (see last page for contact information).
5. Schematics, Bill of Materials (BOM), and Board Layout

Figure 11. Application Schematics
Table 1. Application Board Bill of Materials (BOM)

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Figure 12. Silkscreen – Top of Board
Figure 13. Copper – Top Layer
Figure 14. Copper L1 Layer
Figure 15. Copper L2 Layer
Figure 16. Copper Bottom
## 6. Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
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<td>December 22, 2016</td>
<td>Initial release of document.</td>
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