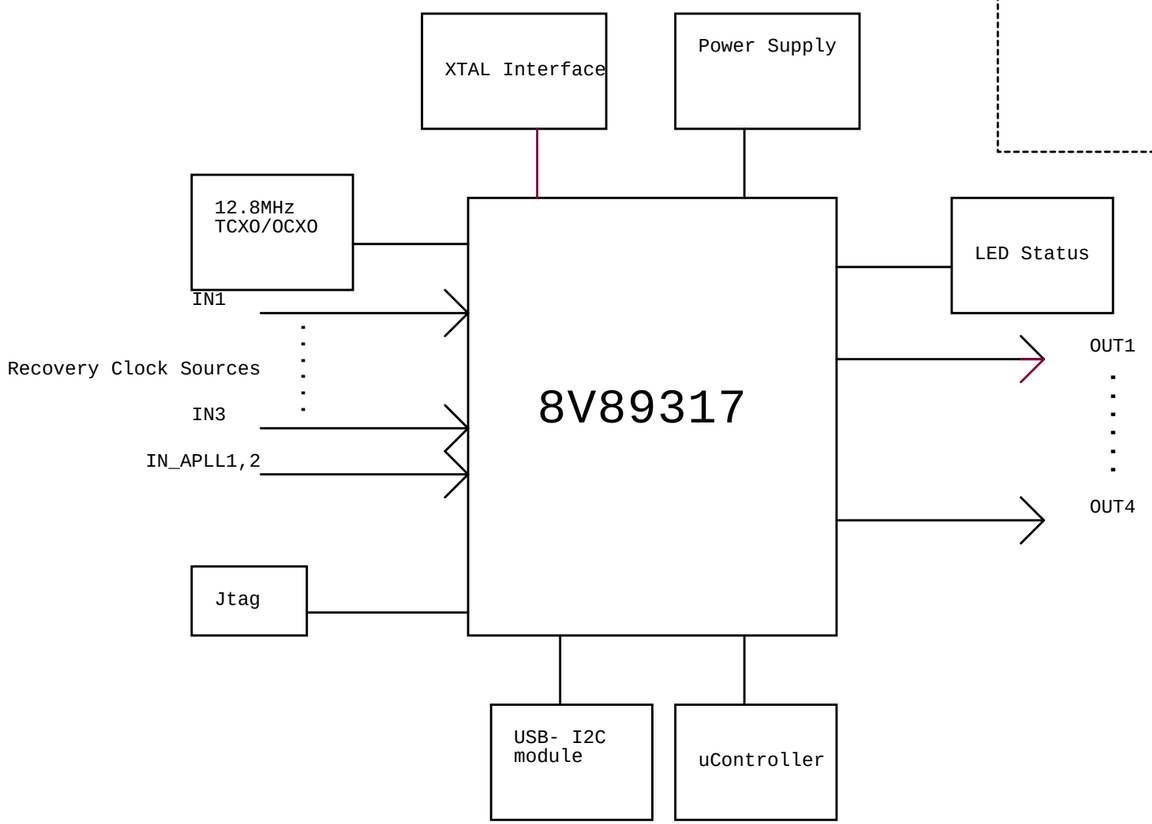
Disclaimer: IDT is providing this schematic for reference purposes only. Although the schematic was taken from a known working design, it is being provided "as is" without any express or implied warranty of any kind.



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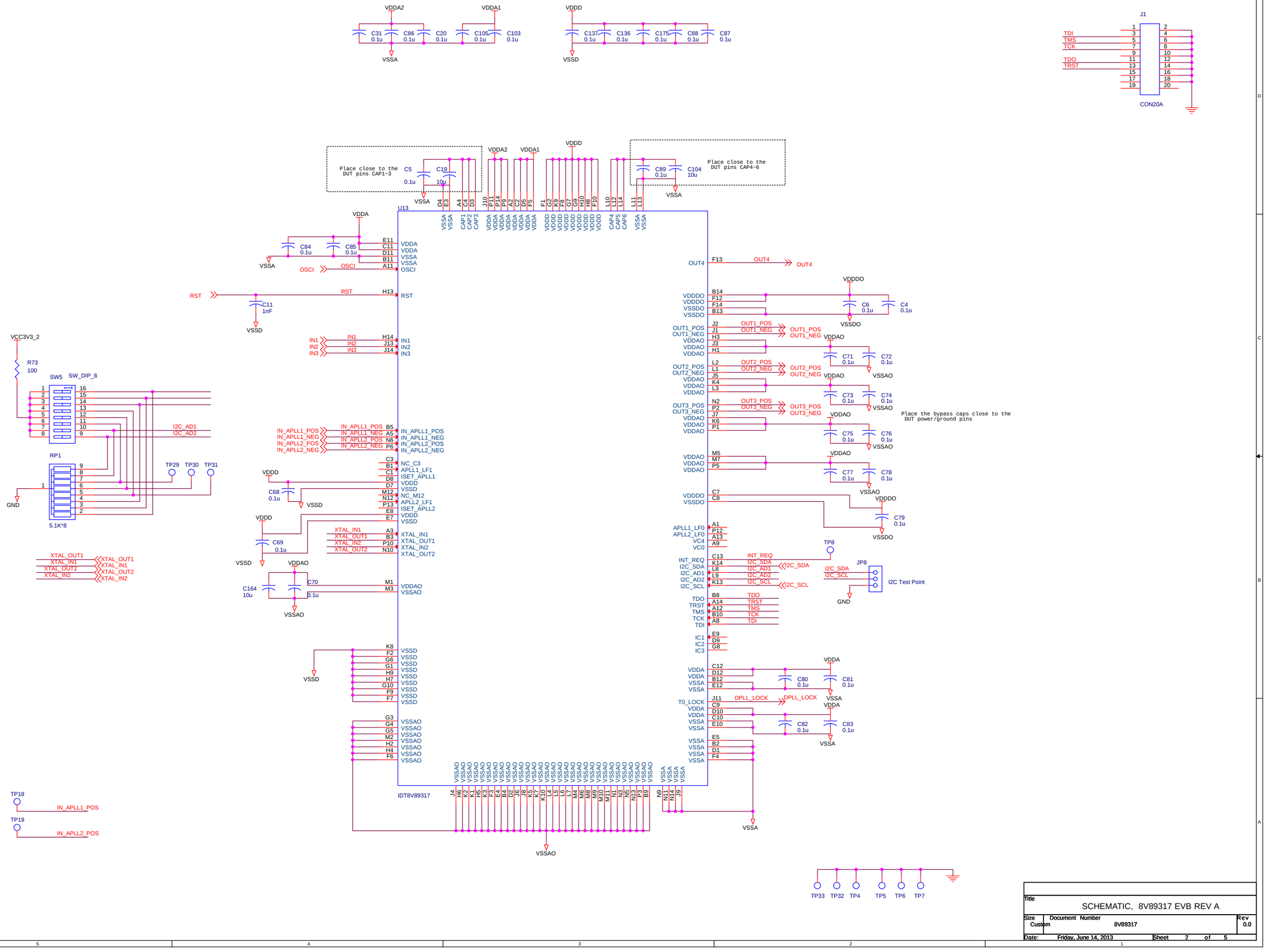

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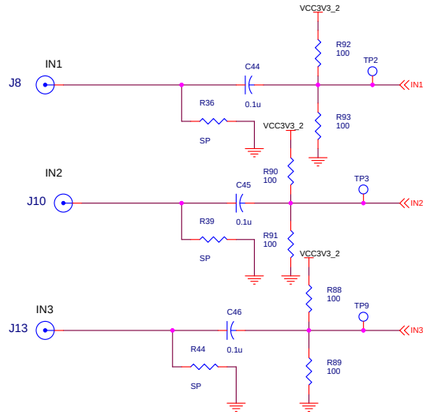
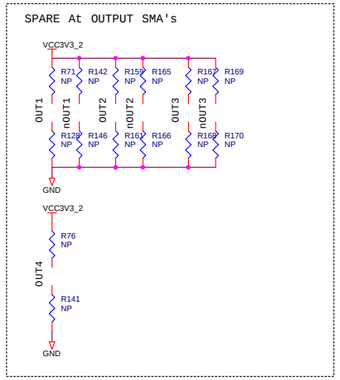
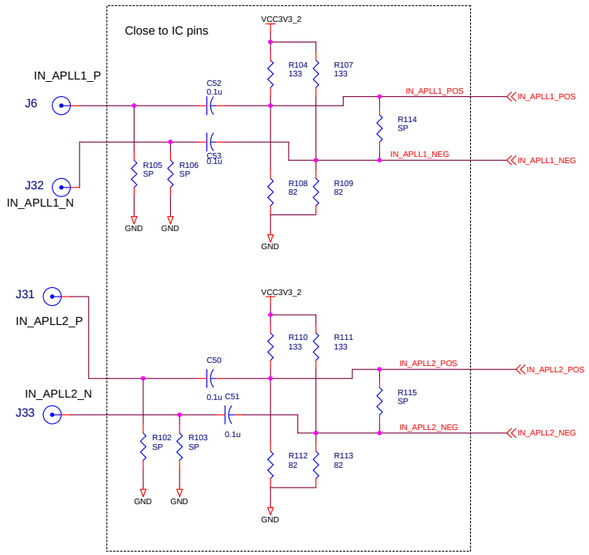
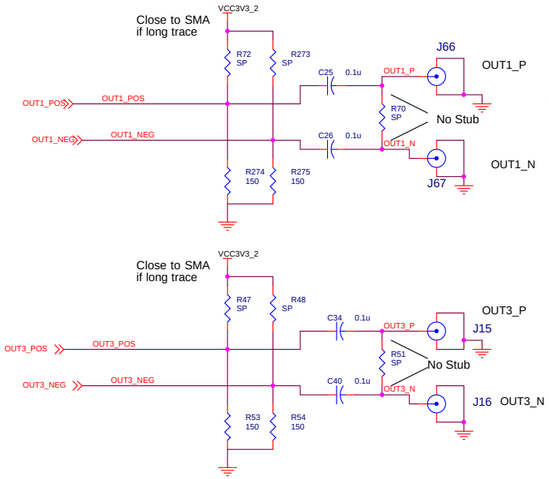
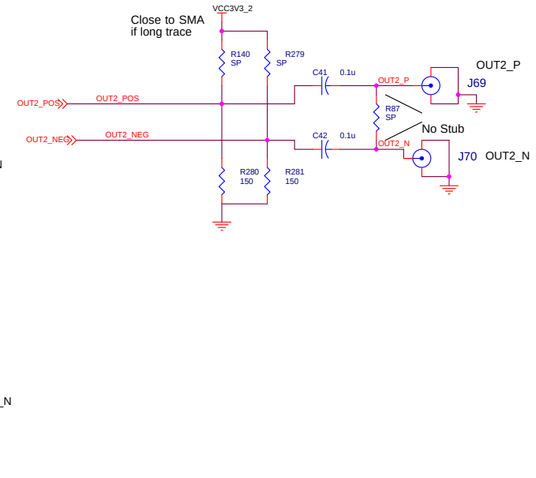


Series termination resistors close to output driver









SMA's for input can be either END LAUNCH or STRAIGHT depends on which way save space. TBD during layout

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12.8MHz, TCXO or OCXO (Place close to the DUT)

U6 M5626LF 12.8MHz
DNC GND
VCC OUT
OCXO_Power
C47 10u
C48 0.1u

U1 12M8_ TCXO
Tri-state_Enable NC7 NC6
VCC DNC10 OUT GND
DNC1 NC2 DNC3
C1 10u
C2 0.1u
C3 0.1u
R1 SP
TCXO
R24 SP
R2 SP
R3 0
J2
JP9
XO/SMA option
OSCI
R8 0
R5 SP

U4 RTX5032
NC1 NC2 NC3 GND VC FILTER RF OUT NC10 NC8 NC5 VCC
C15 0.1u
C17 0.1u
C171 0.1u
R9 100
R11 100

VCC3V3_2
L8 BLM18BB221SN1
C12 0.1u
VCC_OCXO
L9 BLM18BB221SN1
C9 0.1u
C7 10u
C8 0.1u
R6 SP
TP1
C10 0.1u

U2
INPUT_SUPPLY RF_OUTPUT NC2 NC1 NC5 NC6 GND
2910 Stratum 3E OCXO
R7 SP

25MHz XTAL Interface (Place close to the DUT and Put xtals on same layer as BGA pads, shorter trace length, no stubs)

1) Clocks and frequently switched signals should not be routed close to the crystals.
2) Digital signals should not be routed directly under the crystal or XTALn_IN/OUT pins.
3) Keep the crystal bond pads and trace width to the XTALn_IN/OUT pins as small as possible.
4) All metal layers in the PCB are recommended to be removed under the XTALn_OUT ball, crystal pad and associated trace.
5) It is recommended to protect crystal traces with ground traces and guard rings.

XTAL_OUT1 XTAL_IN1 XTAL_OUT2 XTAL_IN2

XTAL_OUT1
0025.000000 MHz X2
XTAL_IN1

XTAL_OUT2
0025.781250 MHz X4
XTAL_IN2

R152 1K
LD8 RED LED
R189 0
VCC2232
R153 470
C168 0.1u
C167 0.1u
C165 10u
C138 0.1u
C166 0.01u
VCC2232_3V
3V3_USB
C147 0.1u

J3
VBUS D- D+ GND
USB PORT
R78 27
R77 27

U3
3V3OUT AVCC VCC VCC VCCIOA VCCIOB
USBDM USBDP RSTOUT# XTIN XTOUT RESET# EECS EESK EEDATA TEST PWREN# AGND GND GND GND GND
ft2232_chip
TCK/SK TDI/DO TDO/DI TMS/CS GPIOL0 GPIOL1 GPIOL2 GPIOL3 GPIOH0 GPIOH1 GPIOH2 GPIOH3 SI/WUA UNUSED0 UNUSED1 UNUSED2 UNUSED3 UNUSED4 UNUSED5 UNUSED6 UNUSED7 UNUSED8 UNUSED9 UNUSED10 UNUSED11 SI/WUB
SCL1 SDA1

R80 1.5K
Y3 6MHz
C169 33PF
C170 33PF
R156 10K
R157 10K
R158 10K
R10 0
R188 4.7K
R187 4.7K
R190 SP
R191 SP
I2C_SCL I2C_SDA
R154 470
LD9 Green LED
R13 SP
R14 0
USB to I2C
JP6 SCL1 I2C_SCL SCL2 Header_3Pin
JP7 SDA1 I2C_SDA SDA2 Header_3Pin

U7F 74HC14/SO

SW2
C39 1u
R74 10K
SW_PUSHBUTTON
RST
U7C 74HC14/SO

Indicator
C13 0.1u
U7D 74HC14/SO
DPLL_LOCK
R79 1K
LD1

J68
SCL2 SDA2
Aardvark I2C/SPI Host Adapter

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(VCC3V3_1 is used for the 8V89317 DUT and VCC3V3_2 is for the rest of the board circuits.
We are not suggesting a dedicated LDO for the 8V89317 with this reference design, this is just convenient for the test.)

VCC5V
VCC5
J54
D1
CGRA4004-G
C90 0.1u
C91 47u
R124 0
U11 VREG_LT1764AEQ_3.3
VIN VOUT SHDN GND SENSE
C180 SP
C176 10u
C178 0.1u
R192 0
C179 0.1u
C174 47u
C177 0.1u
JP2
R139 SP
VCC3V3_2
R129 470
LD5
J55 POWER_SOCKET
5V
D2
C92 SP
C95 10u
C96 0.1u
U10 VREG_LT1764AEQ_3.3
R125 0
C97 SPARE
C93 470uF
C94 47u
C100 0.1u
JP1
R138 SP
VCC3V3_1
R195 470
LD6
VCC_OCXO
J58
D4 CGRA4004-G
C173 0.1u
C172 47u
J57
GND

(Place caps close to and accross power and ground pins)

VCC3V3_1
JP5
L2 BLM18BB221SN1
R193 SP
C98 0.1u
C99 0.1u
C102 0.1u
C116 0.1u
C118 SP
C129 SP
C148 10u
VDDA
VSSA
8V89317 Analog Power

JP12
L7 BLM18BB221SN1
R194 SP
C115 0.1u
C125 0.1u
C114 0.1u
C108 0.1u
C150 10u
VDDD
VSSD
8V89317 Digital Power

JP13
L17 BLM18BB221SN1
R196 SP
C141 0.1u
C142 0.1u
C144 0.1u
C160 0.1u
C145 10u
VDDDO
VSSDO
8V89317 Digital Output Power

JP14
L14
R197 SP
C133 0.1u
C134 0.1u
C140 0.1u
C122 0.1u
C153 10u
VDDAO
VSSAO
8V89317 Analog OUTPUT Power

VDDA1
C127 0.1u
C126 0.01u
VDDA2
C130 0.1u
C128 0.01u

Title	SCHEMATIC, 8V89317 EVB REV A	
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