Flexible Solutions for Fast Edge Rate and Low Phase Noise Requirements

IDT provides a broad range of high-performance mixed-signal semiconductor solutions that optimize our customers’ applications in key markets.

These products are part of a portfolio specifically designed with ultra-low phase noise performance and faster edge rates in mind. This makes them ideal for meeting the stringent timing requirements for the latest FPGAs used in communications, data center and industrial applications. IDT’s broad portfolio of timing devices can satisfy timing budget requirements when designing around an FPGA. This is just another reason why IDT consistently delivers extraordinary value to its customers.

**Synthesizers**

IDT’s synthesizers are industry-leading, stand-alone devices that replace crystal and SAW oscillators in high-end applications. Part of our flagship offering, these devices employ a simple, low-cost fundamental mode crystal as the low frequency reference which enables the devices to synthesize a high-quality, low-jitter clock signal with performance levels reaching <100 fs of RMS phase jitter and output frequencies >1 GHz. Versions offering the flexibility of up to 9 independent outputs, with 12 outputs total round off this versatile offering.

**Jitter Attenuators**

IDT’s family of universal frequency translator timing devices offer translations from virtually any input frequency to any output frequency, and feature eight independently-programmable clocking outputs with the flexibility to generate eight different frequencies within up to four frequency domains. The devices deliver reliable, solid jitter performance in many different applications and provide jitter attenuation and consistent phase noise performance at any loop bandwidth setting.

### Part Number | RMS Phase Jitter (typ) | Tr/Tf (max) | Inputs | Input Freq (MHz) | Outputs | Output Type | Output Voltage (V) | Output Frequency (MHz)
--- | --- | --- | --- | --- | --- | --- | --- | ---
8T49NS010 | 84 fs | 130 ps | XTAL or REF | 10 - 70 | 10 | LVPECL | 3.3 | 100 - 2500
8T49N00X | 228 fs | 400 ps | XTAL or REF | 10 - 312.5 | 4, 6, 8 | LVPECL or LVDS | 2.5, 3.3 | 15.16 - 1250
8T49N1012 | 350 fs | 250 ps (LVDS) | XTAL or REF | 10 - 600 | 12 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000

### Part Number | RMS Phase Jitter (typ) | Tr/Tf (max) | Inputs | Input Freq (MHz) | Outputs | Output Type | Output Voltage (V) | Output Frequency (MHz)
--- | --- | --- | --- | --- | --- | --- | --- | ---
8T49N285 | < 300 fs | 400 ps (LVDS) | XTAL or REF (2) | .008 - 875 | 8 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000
8T49N286 | < 300 fs | 400 ps (LVDS) | XTAL or REF (4) | .008 - 875 | 8 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000
8T49N287 | < 300 fs | 400 ps (LVDS) | XTAL or REF (2) | .008 - 875 | 8 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000
8T49N241 | < 350 fs | 350 ps | XTAL or REF (2) | .008 - 875 | 4 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000
8T49N242 | < 350 fs | 350 ps | XTAL or REF (2) | .008 - 875 | 4 | LVDS, LVPECL, HCSL, LVCMOS | 3.3, 2.5 | .008 - 1000
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8T49NS010 BLOCK DIAGRAM

Fanout Buffers

IDT offers a complete family of low additive phase jitter buffers designed for the most sensitive applications today. These buffers offer versions with up to 12 outputs and additive phase jitter as low as 30 fs! For applications where cost sensitivity and high performance are key, look to IDT’s portfolio of RF buffers.

<table>
<thead>
<tr>
<th>Series</th>
<th>RMS Additive Phase Jitter (max)</th>
<th>Tr/TF (max)</th>
<th>Inputs</th>
<th>Input Frequency Range (MHz)</th>
<th>Outputs</th>
<th>Output Type</th>
<th>Output Voltage (V)</th>
<th>Output Frequency Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8SLVP</td>
<td>100 fs</td>
<td>200 ps</td>
<td>up to 2</td>
<td>up to 2000</td>
<td>2, 4, 6, 8</td>
<td>LVPECL</td>
<td>3.3, 2.5</td>
<td>up to 2000</td>
</tr>
<tr>
<td>8SLVD</td>
<td>100 fs</td>
<td>300 ps</td>
<td>up to 2</td>
<td>up to 2000</td>
<td>2, 4, 6, 8</td>
<td>LVDS</td>
<td>3.3, 2.5</td>
<td>up to 2000</td>
</tr>
<tr>
<td>8P34S</td>
<td>100 fs</td>
<td>400 ps</td>
<td>up to 2</td>
<td>1200</td>
<td>2, 4, 6, 8, 12</td>
<td>LVDS</td>
<td>3.3, 2.5</td>
<td>1200</td>
</tr>
<tr>
<td>8T39S</td>
<td>250 fs</td>
<td>165 ps</td>
<td>XTAL or REF (2)</td>
<td>up to 2000 LVPECL, LVDS</td>
<td>4, 6, 8, 10</td>
<td>LVDS, LVPECL, HCSL, LVCMOS</td>
<td>3.3, 2.5</td>
<td>up to 2000 LVPECL, LVDS</td>
</tr>
</tbody>
</table>

To learn more about IDT’s reference clocks for Fast Edge Rate FPGAs visit IDT.com/go/timing