

Comprehensive timing portfolio from the leader in PCI Express timing solutions

**PERFORMANCE**

- PCIe Gen1, 2.5Gb/s
- PCIe Gen2, 5Gb/s
- PCIe Gen3, 8Gb/s
- PCIe Gen4, 16Gb/s
- CCIX EDR, 25Gb/s

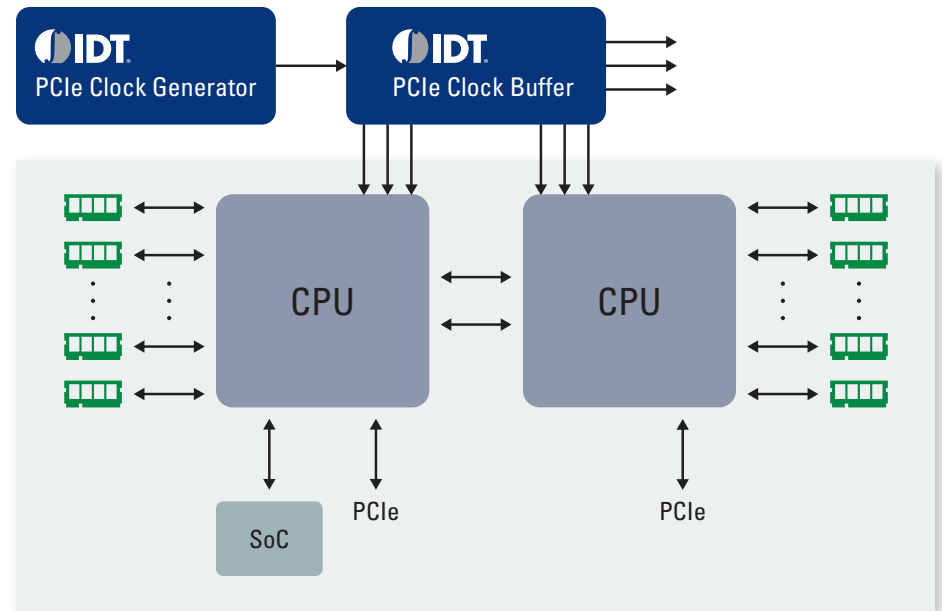
**INTEGRATION**

- Integrated termination resistors eliminate up to 76 discrete components
- Integrated crystal load capacitors on PhiClock™ devices
- Integrated crystal option on PhiClock

**SECURITY**

- SMBUS write to protect available

# PCI Express® Timing Solutions



IDT's industry-leading PCIe® timing portfolio provides the most complete solution for networking, storage and data center applications.

Our PCIe clock generators, zero-delay and fanout buffers, and fanout multiplexers support PCIe Gen1 to Gen4 data rates and derivatives such as 25G EDR. These devices are all designed to work together to form a full solution.

IDT's patented LP-HCSL outputs with integrated terminations eliminate up to 4 resistors per differential output, saving board space and reducing output power up to 90% over standard HCSL outputs.

Our extensive selection of timing devices allows designers to implement the most complex PCI Express clock trees while maintaining timing margin, ensuring robust system operation.

## PCI Express Timing Solutions

**9FG Clock (Frequency) Generators**

- Eliminate up to 32 resistors
- Save up to 55 mm<sup>2</sup> of area<sup>†</sup>
- As small as 6.25 mm<sup>2</sup>
- 85 Ω and 100 Ω system support
- SSC generation

**9ZX/9DB Zero-delay Fanout Buffers**

- Eliminate up to 76 resistors
- Save up to 130 mm<sup>2</sup> of area<sup>†</sup>
- As small as 16 mm<sup>2</sup>
- 85 Ω and 100 Ω system support
- SSC compatible

**9ZM/9DM Fanout Multiplexers**

- Eliminate up to 48 resistors
- Save up to 82 mm<sup>2</sup> of area<sup>†</sup>
- As small as 9 mm<sup>2</sup>
- 85 Ω and 100 Ω system support
- SSC compatible

<sup>†</sup> Compared to traditional HCSL outputs

## PCI Express Timing Solutions

PCIe Clock Generators								
Part Number				All parts support Spread Spectrum				
Prefix	Operating Voltage (V)	PCIe Outputs	Zout ( $\Omega$ )	Ref Output	PCIe Gen Compliance	PCIe Architecture Support**	Package Type	Package Dimensions (mm)
9FG	U = 1.5	02 04 06 08	3x = 33	Yes***	1, 2, 3	CC	QFN-16 QFN-24 QFN-32 QFN-40 QFN-48	2.5 x 2.5
	V = 1.8		4x = 100		1, 2, 3, 4			CC SRNS, SRIS
	L = 3.3		4x = 100 5x = 85			5 x 5		
<b>PhiClock PCIe Clock Generators</b>								
9FGV1001*	1.8 - 3.3	4	100 or 85	Yes	1, 2, 3, 4 25Gb EDR	CC	QFN-24	4 x 4
9FGV1005*		2				SRNS		
9FGV1006*		2				CC SRNS, SRIS	QFN-16	3 x 3
PCIe Clock Zero-Delay (PLL) Buffers with Fanout Mode								
Part Number				All parts support Spread Spectrum				
Prefix	Supply Voltage (V)	PCIe Outputs	Zout ( $\Omega$ )	Pin Control of ZDB or Fanout Mode	PCIe Gen Compliance	PCIe Architecture Support**	Package Type	Package Dimensions (mm)
9DB	V = 1.8 U = 1.5	02 04 06 08	3x = 33 4x = 100	Yes	1, 2, 3	CC	QFN-24 QFN-32 QFN-40 QFN-48	4 x 4
	L = 3.3		4x = 100 5x = 85		1, 2, 3, 4	CC SRNS, SRIS		5 x 5 6 x 6
9ZX	L = 3.3	06 08 12 15 19	3x = 100 5x = 85		1, 2, 3, 4, 25Gb EDR	CC SRNS, SRIS	QFN-40 QFN-48 QFN-64 QFN-72 GQFN-80	5 x 5 6 x 6 9 x 9 10 x 10 6 x 6
PCIe Clock Fanout Buffers								
Part Number				All parts support Spread Spectrum				
Prefix	Supply Voltage (V)	PCIe Outputs	Zout ( $\Omega$ )	Pin Control of ZDB or Fanout Mode	PCIe Gen Compliance	PCIe Architecture Support**	Package Type	Package Dimensions (mm)
9DB	V = 1.8 U = 1.5	05 07 09	3x = 33 4x = 100	N/A	1, 2, 3	CC	QFN-32 QFN-40 QFN-48	5 x 5 5 x 5 6 x 6
	L = 3.3		4x = 100 5x = 85		1, 2, 3, 4	CC SRNS, SRIS		QFN-40 QFN-48
PCIe Clock Multiplexers								
Part Number				All parts support Spread Spectrum				
Prefix	Supply Voltage (V)	PCIe Outputs	Zout ( $\Omega$ )	Sync/Async Switch Mode	PCIe Gen Compliance	PCIe Architecture Support**	Package Type	Package Dimensions (mm)
9DM	V = 1.8 U = 1.5	01 04	3x = 33 4x = 100	Yes	1, 2, 3	CC	QFN-16 QFN-24	3 x 3 4 x 4
	L = 3.3		04		4x = 100 5x = 85	1, 2, 3, 4		CC SRNS, SRIS
9ZM	L = 3.3	12	3x = 100 5x = 85	N/A	1, 2, 3, 4, 25Gb EDR	CC SRNS, SRIS	QFN-72	10 x 10

\* Integrated crystal option available with PhiClock devices

\*\* CC = Common Clock, SRNS = Separate Reference No Spread, SRIS = Separate Reference Independent Spread

\*\*\* The 9FGV0242 in the QFN16 package does not have a REF output

To request samples, download documentation or learn more visit: [idt.com/pcietiming](http://idt.com/pcietiming)

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