



Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **L0105-03** DATE: **May 24, 2001**
Product Affected: **QS3VH245, QS32XVH245, QS34XVH245**
Manufacturing Location Affected: **N/A**
Date Effective: **August 24, 2001**

MEANS OF DISTINGUISHING CHANGED DEVICES:
 Product Mark
 Back Mark
 Date Code Prefix "XQ" or "QC" to "Z"
 Other

Contact: **Bimla Paul**
Title: **Q. A. Manager**
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Attachment:: Yes No
Samples: Available upon request

DESCRIPTION AND PURPOSE OF CHANGE:

- Die Technology
- Wafer Fabrication Process
- Assembly Process
- Equipment
- Material
- Testing
- Manufacturing Site
- Data Sheet
- Other Die revision from "XQ" or "QC" to "Z" stepping to enhance the device performance

RELIABILITY/QUALIFICATION SUMMARY:

There will be no impact or effect on the product reliability. The qualification data is attached.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ***Approval for shipments prior to effective date.***
Name/Date: _____ E-Mail Address: _____
Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS:

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____



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PCN Type: Die revision

Data Sheet Change Yes.

Following data sheet limits have been revised due to the enhanced device performance:

| Test Parameter | Old Limit | New Limit |
|----------------|-----------|-----------|
| t_{PZLZH} | 9 ns | 7 ns |
| t_{PLZHZ} | 8 ns | 6.5 ns |
| f_{OE} | 1 MHz | 20 MHz |

Detail of Change

The die has been revised from "XQ" and "QC" stepping to "Z" stepping to enhance the device performance.
Selective data sheet limits have been revised due to the enhanced device performance.

Die Revision Details

| | <u>Current Die Rev - XQ</u> | <u>Current Die Rev - QC</u> | <u>New Die Rev - Z</u> |
|------------------------------|-----------------------------|-----------------------------|------------------------|
| Wafer Fab Technology | 0.8 μ | 0.8 μ | 0.8 μ |
| Poly Gate | 0.8 μ | 0.8 μ | 0.8 μ |
| Minimum Gate Oxide Thickness | 150 Å | 150 Å | 150 Å |
| Wafer Size | 6 " | 6 " | 6 " |
| Fab Facility | Fab 5 (PSA, Australia) | Fab 2 (Salinas, USA) | Fab 2 (Salinas, USA) |
| Date Code Prefix | XQ | QC | Z |

Conversion schedule (Estimated)

| | Sample Availability | Production Shipments |
|------------|----------------------------|-----------------------------|
| QS3VH245 | Available | 08/24/01 |
| QS32XVH245 | Available | 08/24/01 |
| QS34XVH245 | Available | 08/24/01 |



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Qualification Plan QLG-01-01

Test Vehicle: QS3VH862

Qualification Test Plan and Results:

| Test Description | SS/Acc # | Test Results |
|---|----------|--------------|
| Dynamic High Temp Operating Life Test Mil-Std-883, Method-1005 | 116/0 | 116/0 |
| ESD - HBM Mil-Std-883, Method-3015 | 3/0 | 3500 Volts |
| ESD-CDM JESD22-C101 | 3/0 | 1000 Volts |
| ESD-MM EIAJ-IC-121 | 3/0 | 400 Volts |
| Latch-up EIA/JESD78 | 10/0 | 10/0 |

Characterization Data:

Characterization data is available upon request.