



Device Overview

The 89HPES32T8G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES32T8G2 is a 32-lane, 8-port switch optimized for PCI Express Gen2 packet switching in high-performance applications. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Utilizing standard PCI Express Gen2 interconnect, the PES32T8G2 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. Each lane is capable of 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 2.0.

Features

◆ High Performance Non-Blocking Switch Architecture

- 32-lane 8-port PCIe switch
 - Four x8 switch ports each of which can bifurcate to two x4 ports (total of eight x4 ports)
- Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 32 GBps (256 Gbps) of switching capacity
- Supports 128 Bytes to 2 KB maximum payload size
- Low latency cut-through architecture
- Supports one virtual channel and eight traffic classes

◆ Standards and Compatibility

- PCI Express Base Specification 2.0 compliant
- Implements the following optional PCI Express features
 - Advanced Error Reporting (AER) on all ports
 - End-to-End CRC (ECRC)
 - Access Control Services (ACS)
 - Power Budgeting Enhanced Capability
 - Device Serial Number Enhanced Capability
 - Sub-System ID and Sub-System Vendor ID Capability
 - Internal Error Reporting ECN
 - Multicast ECN
 - VGA and ISA enable
 - L0s and L1 ASPM
 - ARI ECN

◆ Port Configurability

- x4 and x8 ports
 - Ability to merge adjacent x4 ports to create a x8 port
- Automatic per port link width negotiation (x8 → x4 → x2 → x1)
- Crosslink support
- Automatic lane reversal

- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
 - De-emphasis
 - Receive equalization
 - Drive strength

◆ Initialization / Configuration

- Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
- Common switch configurations are supported with pin strapping (no external components)
- Supports in-system Serial EEPROM initialization/programming

◆ Quality of Service (QoS)

- Port arbitration
 - Round robin
 - Weighted Round Robin (WRR)
- Request metering
 - IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput
- High performance switch core architecture
 - Combined Input Output Queued (CIOQ) switch architecture with large buffers

◆ Multicast

- Compliant to the PCI-SIG multicast ECN
- Supports arbitrary multicasting of Posted transactions
- Supports 64 multicast groups
- Multicast overlay mechanism support
- ECRC regeneration support

◆ Clocking

- Supports 100 MHz and 125 MHz reference clock frequencies
- Flexible clocking modes
 - Common clock
 - Non-common clock

◆ Hot-Plug and Hot Swap

- Hot-plug controller on all ports
 - Hot-plug supported on all downstream switch ports
- All ports support hot-plug using low-cost external I²C I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
 - Enables SCI/SMI generation for legacy operating system support
- Hot-swap capable I/O

◆ Power Management

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
 - Supports L0, L0s, L1, L2/L3 Ready and L3 link states
 - Configurable L0s and L1 entry timers allow performance/power-savings tuning
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
 - Supports low swing / half-swing SerDes operation
 - SerDes optionally turned-off in D3hot
 - SerDes associated with unused ports are turned-off
 - SerDes associated with unused lanes are placed in a low power state

◆ 9 General Purpose I/O**◆ Reliability, Availability and Serviceability (RAS)**

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ Test and Debug

- On-chip link activity and status outputs available for Port 0 (upstream port)
- Per port link activity and status outputs available using external I²C I/O expander for all other ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ Power Supplies

- Requires only two power supply voltages (1.0 V and 2.5 V)
- No power sequencing requirements

◆ Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing

Block Diagram

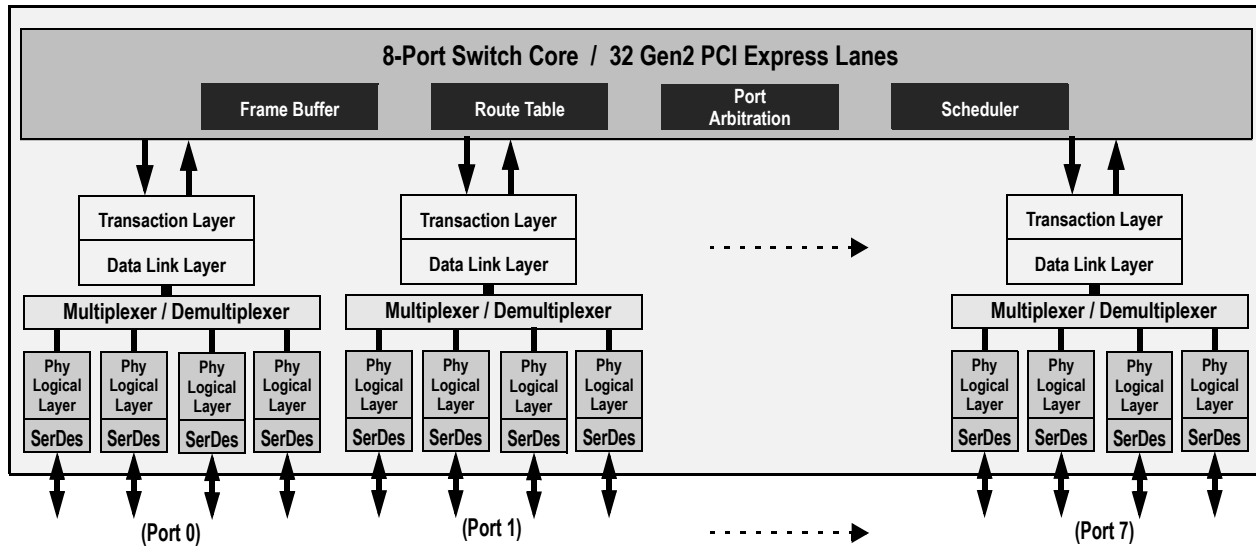


Figure 1 PES32T8G2 Block Diagram

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CORPORATE HEADQUARTERS
 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
 www.idt.com

for Tech Support:
 email: ssdhelp@idt.com
 phone: 408-284-8208