Clock Data Recovery Device
894D115i-01/-04

SECURE SUPPLY: IDT CLOCK DATA RECOVERY SOLUTION FOR THE INDUSTRY-STANDARD VSC8115 DEVICE IS NOW FULLY AVAILABLE IN PRODUCTION QUANTITIES.

**TYPICAL APPLICATIONS:**
- Clock and data recovery of STM-1/-4 (OC-3/-12) data streams
- Wireless infrastructure; transport and backhaul
- Wired communication
- Line cards with electro-optical interface
- Core switches and ADM equipment

**Description**

Clock and data recovery (CDR) circuits are designed to extract the clock signal from NRZ-coded input data signals. The device input accepts 622.08 or 155.52 Mbit/s data signals. The output signals of the device are the recovered clock and retimed data signals. An internal phased locked loop (PLL) is used for clock generation and recovery. An external clock input establishes an initial operating frequency for the clock recovery PLL and provides a clock reference in the absence of serial input data.

The CDR circuit uses differential inputs and outputs to support high clock and data rates for the best signal integrity. All control inputs and outputs are single-ended signals. The device supports a signal detect input and a lock detect output to facilitate interfacing with electro-optical modules. The 894D115i-01/-04 is pin and function compatible with the Vitesse VSC8115. The IDT CDR device family is released to production and fully available.

**Block Diagram**
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