PCle2 to S-RIO2 Bridging + Switching Evaluation Platform

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Decoupling Rule
Caps must be located in the ball grid except for >0.1uF

Make two separate power planes: 1.0V_VDD and 1.0V_VDDA_TSI721

Total DC resistance: 25mOhm max.
Expected voltage drop: 7mV
Equivalent to 110 Ohms / 4A ferrite bead
These caps must be located in the ball grid except for >0.1uF

Make two separate power planes: 1.0V_VDD and 1.0V_VDDA

Expected voltage drop: 26mV max
Total DC resistance: 12mOhm max.
Equivalent to 30 Ohms / 6A ferrite bead

Decoupling 3.3V

Decoupling 1.2V_VDD
Most of these caps must be located in the ball grid
Bulk decoupling is on the regulator page
AMC Hot plug / Power Controller

10K
3.3V

R74

C322 22U
12V

C46 47U

R182 10

J34 69190-102H

U12 74LVC1G125

R31 300

U20 FDS6680S

R102 49.9

AMC Hot plug / Power Controller

Fan connector

Fan connector

Red LED

Inserting Jumer will turn AMC power OFF

100K internal pullup

240mA current limit

6.25A current limit

Fan connector

AMC_12PGOOD

AMC_3V3

AMC_12V
Green LEDs will turn ON during normal operation
IDT has introduced new improved clocking solutions since this evaluation board was developed. The recommended timing solutions for new designs are:

1. **VersaClock 5 Devices**: In System Programmable, Very Low Power, with up to four universal output pairs.

2. **XUM LVDS Crystal Oscillator**: Ultra precise with only 300fs typical phase jitter. If using a 156.25 MHz clock source then the applicable part number is XUM535156.250JS618.
Revision History

April 7, 2015 -- Added a note on page 16 on improving clocking solutions for S-RIO components.

June 28, 2011 -- The following changes were made:
* Sheet 4 - Added connections to ground on SP_SWAP_TX and SP_SWAP_RX
* Sheet 4 - Added 10K pull up resistors to 3.3V on SP_DEVID, CLKSEL[0] and CLKSEL[1]
* Sheet 4 - Added DNP attribute on U10
* Sheet 21 - Changed U13 to SN74AUP1G07
* Sheet 21 - Changed C320 to 0.1uF

April 11, 2011 -- First release of document.