Tsi620 Evaluation Board Schematic

Function Block Diagram

1. Function Block Diagram
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Components Placement Illustration

Revision Notes

*April 2nd, 2009: Final editing for the customer release.*
Tsi620 - I2C, GPIO, and MISC
Tsi620 - FPGA XGMII Interface and PCI Clocking

Notes:
1) Tsi620 drives HSTL-15 Class-I output which is terminated on FPGA with parallel ODT.
2) Tsi620 receives HSTL-15 Class-II from FPGA with source series ODT.
Tsi620 - Power and GND
Tsi620 - Decoupling
FPGA: DSP GPIO, AMC Clock, DSP Frame Sync - Top Bank (1.8V, 2.5V, 3.3V)
FPGA driving RX as HSTL-15 Class-II with 25ohm source serial termination

FPGA driving RX as HSTL-15 Class-II with 25ohm source serial termination

FPGA: RIO-XGMII Interface - Bottom Bank (1.5V HSTL)
FPGA: Antenna Interface - Left Bank (2.5V)
FPGA: Power, Ground, and Decoupling

Notes:
1. 2.5V_A is the filtered 2.5V supply to VCCA_PLL of FPGA.
2. VCCP is the filtered 2.5V supply to VCCP of FPGA.
DSP - Power Supply and Decoupling
SFP Antenna Interface Connectors
Tsi620 JTAG to USB
Power - 5V and 3.3V
Power - 1.1V and DSP core
Power - 1.8V, 1.2V, 1.5V, and 2.5V
System Controller: Analog, MISC, and Power