This is a short form datasheet and is intended to provide an overview only. Additional details are available from IDT. Contact information may be found on the last page.

**HIGHLIGHTS**
- Synchronization Management Unit (SMU) provides tools to manage physical layer and packet based synchronous clocks for IEEE 1588 / PTP Telecom Profile applications
- Supports independent IEEE 1588 and Synchronous Ethernet (SyncE) timing paths
- Combo mode provides SyncE physical layer frequency support for IEEE 1588 Telecom Boundary Clocks (T-BC) and Telecom Time Slave Clocks (T-TSC) per G.8273.2
- Digital PLL 1 (DPLL1) and DPLL 2 can be configured as Digitally Controlled Oscillators (DCOs) for PTP clock synthesis
- DCO frequency resolution is \( \frac{(77760 / 1638400)}{2^{-48}} \) or \( \sim 1.686305041 \times 10^{-10} \) ppm
- DPLL1 and DPLL2 generate G.8262 compliant SyncE clocks
- Two independent Time of Day (ToD) counters/time accumulators, one associated with each of DPLL1 and DPLL2, can be used to track differences between the two time domains and to time-stamp external events
- DPLL3 performs rate conversions to frequency synchronization interfaces or for other general purpose timing applications
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 Pulse Per Second (PPS) references
- It can be configured from an external EEPROM after reset

**FEATURES**
- Differential reference inputs (IN1 to IN4) accept clock frequencies between 1 PPS and 650 MHz
- Single ended inputs (IN5 to IN6) accept reference clock frequencies between 1 PPS and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM, CPRI and GNSS frequencies
- Any reference input (IN1 to IN6) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 0.09 mHz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 1 PPS and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 comply with ITU-T G.8262 for Synchronous Ethernet Equipment Clock (EEC), and G.813 for Synchronous Equipment Clock (SEC); and Telcordia GR-253-CORE for Stratum 3 and SONET Minimum Clock (SMC)
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/ OSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT8
- DPLL1 and DPLL2 can be configured as DCOs to synthesize IEEE 1588 clocks
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT9 and OUT10
- APLL1 and APLL2 can be connected to DPLL1 or DPLL2
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2, OUT7 and OUT8 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT9 and OUT10 output clocks N*8kHz multiples up to 100 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN1 to IN6; the delay for each input is programmable in steps of 0.61 ns with a range of \( \pm 78 \) ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of \( \pm 20 \) μs
- The clock phase of each of the output dividers for OUT1 (from APLL1) to OUT8 is individually programmable in steps of \( \pm 200 \) ps with a total range of \( \pm 180^\circ \)
- 1149.1 JTAG Boundary Scan
- 72-pin QFN green package

**APPLICATIONS**
- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multiservice access platforms
- PON OLT
- LTE eNodeB
- IEEE 1588 / PTP Telecom Profile clock synthesizer
- ITU-T G.8273.2 Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC)
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8263 Packet-based Equipment Clock (PEC)
• ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)
• ITU-T G.813 Synchronous Equipment Clock (SEC)
• Telcordia GR-253-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

DESCRIPTION

The 82P33814 Synchronization Management Unit (SMU) provides tools to manage timing references, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. The device supports up to three independent timing paths that control: PTP clock synthesis; SyncE clock generation; and general purpose frequency translation. The device supports physical layer timing with Digital PLLs (DPLLs) and it supports packet based timing with Digitally Controlled Oscillators (DCOs). Input-to- output, input-to-output and output-to-output phase skew can all be precisely managed. The device outputs low-jitter clocks that can directly synchronize lower-rate Ethernet interfaces; as well as CPRI/OBSAI, SONET/SDH and PDH interfaces and IEEE 1588 Time Stamp Units (TSUs).

The 82P33814 accepts four differential reference inputs and two single ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH and PDH frequencies that range in frequency from 1 Pulse Per Second (PPS) to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all three DPLLs. The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors and LOS inputs.

The 82P33814 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1 or DPLL2 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4 kHz or 8 kHz. This feature enables DPLL1 or DPLL2 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

DPLL1 and DPLL2 support four primary operating modes: Free-Run, Locked, Holdover and DCO. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO mode the DPLL control loop is opened and the DCO can be controlled by a PTP clock recovery servo running on an external processor to synthesize PTP clocks.

The 82P33814 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked and DCO modes.

When used with a suitable system clock, DPLL1 and DPLL2 meet the frequency accuracy, pull-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of the following applications: ITU-T G.8262/G.813 EEC/SEC options 1 and 2, ITU-T G.8263, ITU-T G.8273.2, Telcordia GR-1244 Stratum 3 (S3), Telcordia GR-253-CORE Stratum 3 (S3) and SONET Minimum Clock (SMC).

DPLL1 and DPLL2 can be configured with a range of selectable filtering bandwidths from 0.09 mHz to 567 Hz. The 17 mHz bandwidth can be used to lock the DPLL directly to a 1 PPS reference. The 69 mHz and the 92 mHz bandwidths can be used for G.8273.2. The 92 mHz bandwidth can be used for G.8262/G.813 Option 2 or Telcordia GR-253-CORE S3 or SMC applications. The bandwidths in the range 1.1 Hz to 8.9 Hz can be used for G.8262/G.813 Option 1 applications. Bandwidths above 10 Hz can be used in jitter attenuation and rate conversion applications.

DPLL1 and DPLL2 are each connected to Time of Day (ToD) counters or time accumulators; these ToD counters/time accumulators can be used to track differences between the two time domains and to time-stamp external events by using reference inputs as triggers.

DPLL3 supports three primary operation modes: Free-Run, Locked and Holdover. DPLL3 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered line clock to a 1.544 MHz or 2.048 MHz synchronization interface clock.

In Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC) applications per ITU-T G.8275.2, DPLL1 and DPLL2 are both used; one DPLL is configured as a DCO to synthesize PTP clocks and the other DPLL is configured as an EEC/SEC to generate physical layer clocks. Combo mode provides physical layer frequency support from the EEC/SEC to the PTP clock.

In Synchronous Equipment Timing Source (SETS) applications per ITU-T G.8264, DPLL1 or DPLL2 can be configured as an EEC/SEC to output clocks for the T0 reference point and DPLL3 can be used to output clocks for the T4 reference point.

Clocks generated by DPLL1 or DPLL2 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces.

All 82P33814 control and status registers are accessed through an I2C slave, SPI or the UART microprocessor interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset.
FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram
1 PIN ASSIGNMENT

Figure 2. Pin Assignment (Top View)
## 2 PIN DESCRIPTION

### Table 1: Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| 6       | OSCI                        | I   | CMOS        | **OSCI: Crystal Oscillator System Clock**  
A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ2 |
| 58      | MS/SL                       | pull-up | CMOS   | **MS/SL: Master / Slave Selection**  
This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit. |
| 59      | LOS3                        | pull-down | CMOS  | **LOS3:** This pin is used to disqualify input clocks. See input clocks section for more details.                                       |
| 52      | RSTB                        | pull-up | CMOS        | **RSTB: Reset**  
Refer to section 2.2 reset operation for detail.                                                                                          |
| 7 8 9   | XO_FREQ0/LOS0/XO_FREQ1/LOS1/XO_FREQ2/LOS2 | pull-down | CMOS  | **XO_FREQ0 ~ XO_FREQ2:** These pins set the oscillator frequency.  
**XO_FREQ[2:0] Oscillator Frequency (MHz)**  
- 000: 10.000  
- 001: 12.800  
- 010: 13.000  
- 011: 19.440  
- 100: 20.000  
- 101: 24.576  
- 110: 25.000  
- 111: 30.720  
**LOS0 ~ LOS2:** These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2 |
| 31 32   | IN1_POS/IN1_NEG              | I   | PECL/LVDS   | **IN1_POS / IN1_NEG: Positive / Negative Input Clock 1**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 33 34   | IN2_POS/IN2_NEG              | I   | PECL/LVDS   | **IN2_POS / IN2_NEG: Positive / Negative Input Clock 1**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 35 36   | IN3_POS/IN3_NEG              | I   | PECL/LVDS   | **IN3_POS / IN3_NEG: Positive / Negative Input Clock 3**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 38 39   | IN4_POS/IN4_NEG              | I   | PECL/LVDS   | **IN4_POS / IN4_NEG: Positive / Negative Input Clock 4**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 37      | IN5                          | pull-down | CMOS  | **IN5: Input Clock 5**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 41      | IN6                          | pull-down | CMOS  | **IN6: Input Clock 6**  
A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin. |
| 43      | FRSYNC_8K_1PPS               | O   | CMOS        | **FRSYNC_8K_1PPS: 8 kHz Frame Sync Output**  
An 8 kHz signal or a 1PPS sync signal is output on this pin.                                                                                       |
| 44      | MFRSYNC_2K_1PPS              | O   | CMOS        | **MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output**  
A 2 kHz signal or a 1PPS sync signal is output on this pin.                                                                                      |
| 30 28   | OUT1 / OUT2                 | O   | CMOS        | **OUT1 ~ OUT2: Output Clock 1 ~ 2**                                                                                                        |
### Table 1: Pin Description (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25, 26</td>
<td>OUT3_POS / OUT3_NEG</td>
<td>O</td>
<td>PECL/LVDS</td>
<td>OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.</td>
</tr>
<tr>
<td>21, 22</td>
<td>OUT4_POS / OUT4_NEG</td>
<td>O</td>
<td>PECL/LVDS</td>
<td>OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4 This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.</td>
</tr>
<tr>
<td>71, 70</td>
<td>OUT5_POS / OUT5_NEG</td>
<td>O</td>
<td>PECL/LVDS</td>
<td>OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5 This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.</td>
</tr>
<tr>
<td>68, 67</td>
<td>OUT6_POS / OUT6_NEG</td>
<td>O</td>
<td>PECL/LVDS</td>
<td>OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.</td>
</tr>
<tr>
<td>65, 63</td>
<td>OUT7 / OUT8</td>
<td>O</td>
<td>CMOS</td>
<td>OUT7 ~ OUT8: Output Clock 7 ~ 8</td>
</tr>
<tr>
<td>61, 60</td>
<td>OUT9 / OUT10</td>
<td>O</td>
<td>CMOS</td>
<td>OUT9 ~ OUT10: Output Clock 9 ~ 10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Miscellaneous</strong></td>
</tr>
<tr>
<td>13</td>
<td>VC1</td>
<td>O</td>
<td>Analog</td>
<td>VC1: APLL1 VC Output An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.</td>
</tr>
<tr>
<td>1</td>
<td>VC2</td>
<td>O</td>
<td>Analog</td>
<td>VC2: APLL2 VC Output An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Lock Signal</strong></td>
</tr>
<tr>
<td>54</td>
<td>DPLL3_LOCK</td>
<td>O</td>
<td>CMOS</td>
<td>DPLL3_LOCK This pin goes high when DPLL3 is locked</td>
</tr>
<tr>
<td>56</td>
<td>DPLL2_LOCK</td>
<td>O</td>
<td>CMOS</td>
<td>DPLL2_LOCK This pin goes high when DPLL2 is locked</td>
</tr>
<tr>
<td>55</td>
<td>DPLL1_LOCK</td>
<td>O</td>
<td>CMOS</td>
<td>DPLL1_LOCK This pin goes high when DPLL1 is locked</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Microprocessor Interface</strong></td>
</tr>
<tr>
<td>57</td>
<td>INT_REQ</td>
<td>O</td>
<td>CMOS</td>
<td>INT_REQ: Interrupt Request This pin is used as an interrupt request.</td>
</tr>
<tr>
<td>46, 45</td>
<td>MPU_MODE1/ I2CM_SCL</td>
<td>I/O</td>
<td>CMOS/ Open Drain</td>
<td>MPU_MODE[1:0]: Microprocessor Interface Mode Selection During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.</td>
</tr>
<tr>
<td></td>
<td>MPU_MODE0/ I2CM_SDA</td>
<td>I/O</td>
<td>CMOS/ Open Drain</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>SDI/2C_AD2/ UART_RX</td>
<td>I</td>
<td>CMOS</td>
<td>SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. UART_RX In UART mode, this pin is used as the receive data (UART Receive).</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Name</td>
<td>I/O</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>----------------</td>
<td>-----</td>
<td>-----------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 48     | CLKE/I2C_AD1   | I   | CMOS      | CLKE: SCLK Active Edge Selection  
In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO:  
High - The falling edge;  
Low - The rising edge.  
I2C_AD1: Device Address Bit 1  
In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. |
| 49     | CS/I2C_AD0     | I   | CMOS      | CS: Chip Selection  
In Serial modes, this pin is an input. A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.  
I2C_AD0: Device Address Bit 0  
In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. |
| 50     | SCLK/I2C_SCL   | I   | CMOS      | SCLK: Shift Clock  
In Serial mode, a shift clock is input on this pin.  
Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE.  
I2C_SCL: Serial Clock Line  
In I2C mode, the serial clock is input on this pin. |
| 51     | SDO/I2C_SDA/UART_TX | I/O | CMOS Open Drain | SDO: Serial Data Output  
In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK.  
I2C_SDA: Serial Data Input/Output  
In I2C mode, this pin is used as the input/output for the serial data.  
UART_TX:  
In UART mode, this pin is used as the transmit data (UART Transmit) |
| JTAG (per IEEE 1149.1) |                      |     |           |                                                                             |
| 14     | TMS            | I   | CMOS      | TMS: JTAG Test Mode Select  
The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK. |
| 15     | TRSTB          | I   | CMOS      | TRSTB: JTAG Test Reset (Active Low)  
A low signal on this pin resets the JTAG test port.  
This pin should be connected to ground when JTAG is not used. |
| 16     | TCK            | I   | CMOS      | TCK: JTAG Test Clock  
The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK.  
If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state. |
| 17     | TDI            | I   | CMOS      | TDI: JTAG Test Data Input  
The test data are input on this pin. They are clocked into the device on the rising edge of TCK. |
| 18     | TDO            | O   | CMOS      | TDO: JTAG Test Data Output  
The test data are output on this pin. They are clocked out of the device on the falling edge of TCK.  
TDO pin outputs a high impedance signal except during the process of data scanning. |
| Power & Ground |                      |     |           |                                                                             |
| 2, 3, 4, 5, 10, 11, 12 | VDDA | Power    | -         | VDDA: Analog Core Power - +3.3V DC nominal |
| 20, 24, 69, 72 | VDDAO | Power    | -         | VDDAO: Analog Output Power - +3.3V DC nominal |
| 27, 29, 64, 66 | VDDDO | Power    | -         | VDDDO: Digital Output Power - +3.3V DC nominal |
2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs
For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs
For applications not requiring the use of a differential input, both _POS and _NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

2.1.2 OUTPUTS

Status Pins
For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs
All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs
All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair

Table 1: Pin Description (Continued)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>I/O</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>40, 62</td>
<td>VDDD</td>
<td>Power</td>
<td></td>
<td>VDDD: Digital Core Power - +3.3V DC nominal</td>
</tr>
<tr>
<td>42, 53</td>
<td>VDDD_1_8</td>
<td>Power</td>
<td></td>
<td>VDDD_1_8: Digital Core Power - +1.8V DC nominal</td>
</tr>
<tr>
<td>19, 23</td>
<td>VSSAO</td>
<td>Ground</td>
<td></td>
<td>VSSAO: Ground</td>
</tr>
<tr>
<td>73 (e_PAD)</td>
<td>VSS</td>
<td>Ground</td>
<td></td>
<td>VSS: Ground</td>
</tr>
</tbody>
</table>
Figure 3. 72-Pin QFN Package Outline Page 1 (SAWN Option)
Figure 4. 72-Pin QFN Package Outline Page 2 (SAWN Option)
Figure 5. 72-Pin QFN Package Recommended Land Pattern

1. Recommended land pattern shown for reference in green.
2. Top down view is reversed on page.
3. All dimension are in mm. Angles in degrees.

Notes:

RECOMMENDED LAND PATTERN

SAWN LAND PATTERN

NOTES
ORDERING INFORMATION

Table 2: Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>82P33814ANLG</td>
<td>72-pin QFN green package</td>
<td>Tray</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>82P33814ANLG8</td>
<td>72-pin QFN green package</td>
<td>Tape &amp; Reel, Pin 1 Orientation: EIA-481-C</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>82P33814ANLG/W</td>
<td>72-pin QFN green package</td>
<td>Tape &amp; Reel, Pin 1 Orientation: EIA-481-D</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Table 3: Pin 1 Orientation in Tape and Reel Packaging

<table>
<thead>
<tr>
<th>Part Number Suffix</th>
<th>Pin 1 Orientation</th>
<th>Illustration</th>
</tr>
</thead>
<tbody>
<tr>
<td>NLG8</td>
<td>Quadrant 1 (EIA-481-C)</td>
<td><img src="image1" alt="Illustration" /></td>
</tr>
<tr>
<td>NLG/W</td>
<td>Quadrant 2 (EIA-481-D)</td>
<td><img src="image2" alt="Illustration" /></td>
</tr>
</tbody>
</table>