Description

The 8V19N492 is a fully integrated FemtoClock NG jitter attenuator and clock synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. The device supports JESD204B subclass 0 and 1 clocks.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency.

The device supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The device is configured through a three-wire SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The 8V19N492 is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

Typical Applications

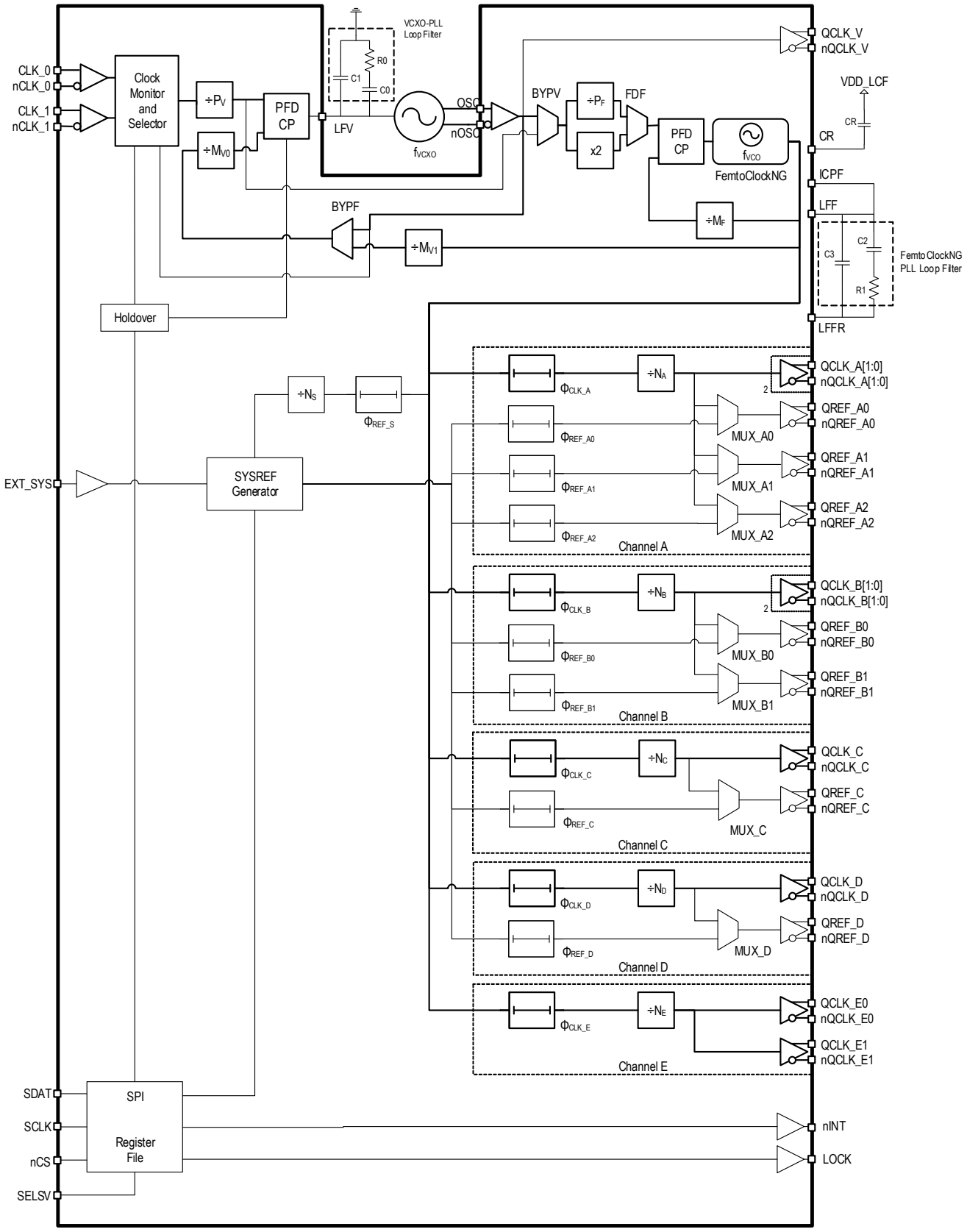
- Wireless infrastructure applications: GSM, WCDMA, LTE, and LTE-A
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

Features

- High-performance clock RF-PLL with support for JESD204B
- Optimized for low phase noise: -150dBc/Hz (800kHz offset; 245.76MHz clock)
- Integrated phase noise of 80fs RMS typical (12k-20MHz).
- Dual-PLL architecture
- 1st-PLL stage with external VCXO for clock jitter attenuation
- 2nd-PLL with internal FemtoClockNG PLL: 2949.12MHz
- Six output channels with a total of 16 outputs, organized in:
  - Four JESD204B channels (device clock and SYSREF output) with two, four and five outputs
  - One clock channel with two outputs
  - One VCXO output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include: 2949.12, 1474.56, 983.04, 491.52, 245.76, and 122.88MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Phase delay circuits
  - Clock phase delay with 256 steps of 339ps and a range of 0 to 86.466ns
  - Individual SYSREF phase delay with 8 steps of 169ps
  - Additional individual SYSREF fine phase delay with 25ps steps
  - Global SYSREF signal delay with 256 steps of 339ps and a range of 0 to 86.466 ns
- Redundant input clock architecture with two inputs and
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and hitless switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B
- Supply voltage: 3.3V
- SPI and control I/O voltage: 1.8V/3.3V (Selectable)
- Package: 10 × 10 mm 88-VFQFPN
- Temperature range: -40°C to +105°C (Case)

Block Diagram

Figure 1. Block Diagram (f_{VCO} = 2949.12MHz)



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