



**FEATURES**

**HIGHLIGHTS**

- Digital PLL locks to Ethernet physical layer clocks
- Provides clocks for 1 Gigabit Ethernet and QSGMII
- Internal Digitally Controlled Oscillator supports IEEE 1588 clock generation
- Jitter generation <0.65 ps RMS (10 kHz to 20 MHz) meets jitter requirements of 1 GbE PHYs and QSGMII

**MAIN FEATURES**

- Digital PLL synchronizes with Ethernet connected synchronization sources
- DPLL bandwidth of 1.2 Hz
- DPLL holdover accuracy is 1.1X10<sup>-5</sup> ppm and instantaneous hold-over accuracy is 4.4X10<sup>-8</sup> ppm
- Input references are monitored for frequency offset and activity
- DPLL holdover, free run and hitless reference switching can be forced by the host processor or can be automatically controlled by an internal state machine

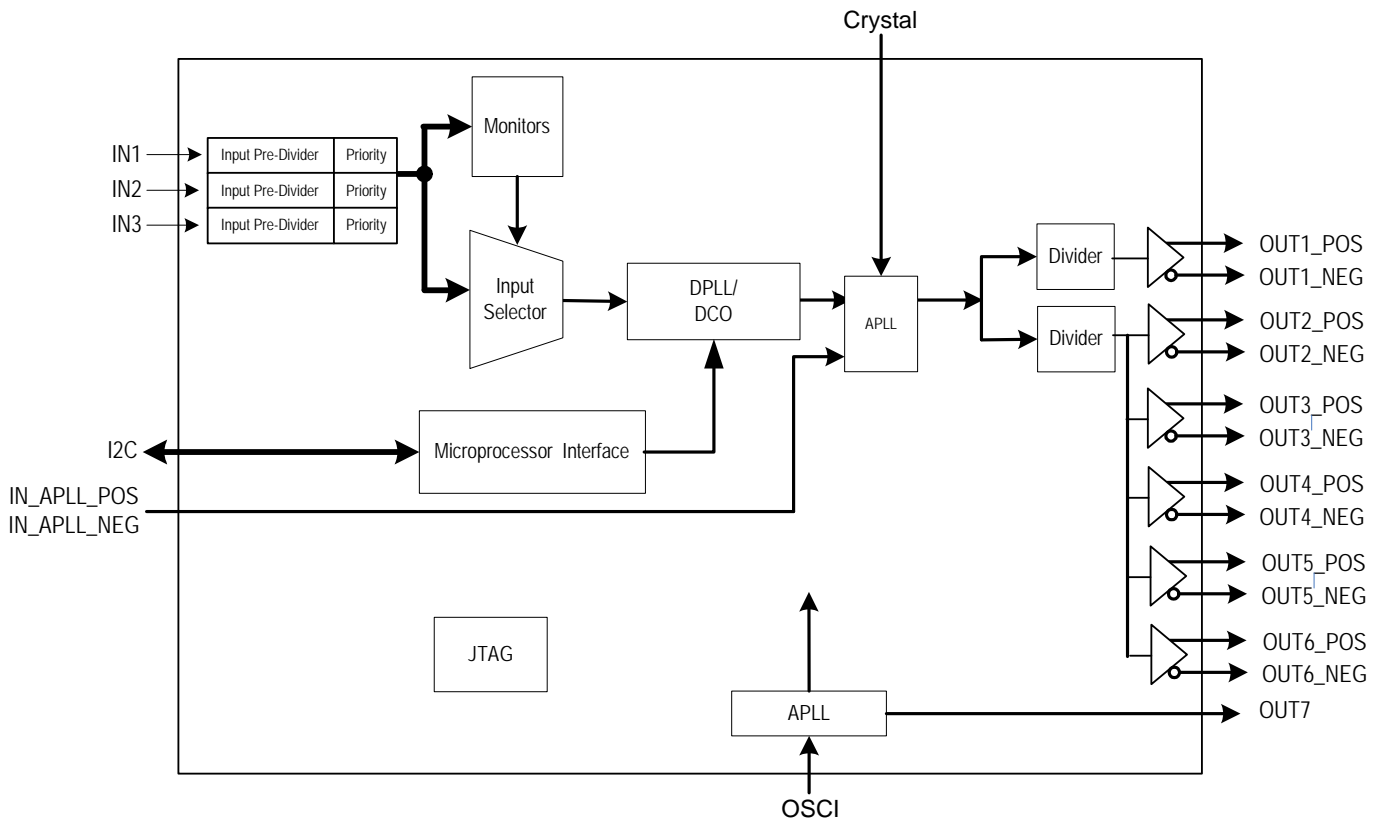
- Internal DCO has resolution of 0.01105 ppb and can be controlled by an external processor via I2C interface for IEEE 1588 clock generation
- One Analog PLL for jitter attenuation
- IN1, IN2 and IN3 accept single ended reference clocks whose frequencies can be 25 MHz, 125 MHz or 156.25 MHz
- OUT1 outputs a differential clock with frequency of 125 MHz or 156.25 MHz
- OUT2 to OUT6 output differential clocks all with the same frequency of 125 MHz or 156.25 MHz
- OUT7 outputs a free-running LVCMOS clock with frequency of 25 MHz

**OTHER FEATURES**

- I2C microprocessor interface mode
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 1mm ball pitch CABGA green package

**APPLICATIONS**

- Industrial Automation
- Power Systems



**Figure 1. Functional Block Diagram**

## DESCRIPTION

The IDT8V89316 Ethernet PLL for Industrial Automation and Power Systems is used to synchronize equipment with synchronization sources using the Ethernet physical layer; it can also be used by external IEEE 1588 clock recovery servos to synthesize IEEE 1588 clocks. The IDT8V89316 low jitter output clocks can be used to directly synchronize 1 Gigabit Ethernet PHYs and QSGMII devices.

The IDT8V89316 synchronization functions are provided by a Digital PLL (DPLL) with an embedded clock synthesizer. The DPLL accepts three single ended reference inputs that can operate at 25 MHz, 125 MHz or 156.25 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. The active reference for the DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors.

The DPLL supports four primary operating modes: Free-Run, Locked, Holdover and Digitally Controlled Oscillator (DCO) Control. In Free-Run mode the DPLL generates a clock based on the master clock alone. In Locked mode the DPLL filters reference clock jitter with the selected bandwidth. In Locked mode the long-term DPLL frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO Control Mode the DPLL

control loop is opened and the DCO can be used by an algorithm (e.g. IEEE 1588 clock servo) running on an external processor to synthesize clock signals.

The IDT8V89316 requires a 12.8 MHz master clock for its reference monitors and other digital circuitry. The frequency accuracy of the master clock determines the frequency accuracy of the DPLL in Free-Run mode. The frequency stability of the master clock determines the frequency stability of the DPLL in Free-Run mode and in Holdover mode. Refer to the IDT application note "Recommended Crystal Oscillators for IDT's Network Synchronization WAN-PLL™" for guidance.

The clock synthesized by the IDT8V89316 DPLL is passed through a voltage controlled crystal oscillator (VCXO) based jitter attenuating analog PLL (APLL). The APLL drives independent dividers that have differential outputs. The APLL uses an external crystal resonator with resonant frequencies equal to the APLL base frequency divided by 25. The output clocks generated by the APLL exhibits jitter below 0.65ps RMS over the integration range 10 kHz to 20 MHz.

The IDT8V89316 generates a 25MHz single ended output that is based on the free running 12.8 MHz master clock. The frequency accuracy and the frequency stability of this 25 MHz clock are determined by the master clock.

# 1 PIN ASSIGNMENT

|   | 1            | 2        | 3        | 4        | 5      | 6           | 7     | 8       | 9       | 10       | 11        | 12    | 13      | 14      |   |
|---|--------------|----------|----------|----------|--------|-------------|-------|---------|---------|----------|-----------|-------|---------|---------|---|
| A | NC           | VDDAO    | OUT6_NEG | NC       | NC     | IC1         | IC1   | TDI     | IC1     | IC2      | OSCI      | TMS   | IC1     | TRST    | A |
| B | NC           | VSSAO    | OUT6_POS | VSSAO    | NC     | IC1         | IC1   | TDO     | VSSA    | TCK      | VSSA      | VSSA  | VSSDO   | VDDDO   | B |
| C | NC           | VDDAO    | NC       | NC       | IC1    | IC1         | VDDDO | VSSDO   | VDDA    | VSSA     | VDDA      | VDDA  | INT_REQ | IC1     | C |
| D | VSSAO        | VSSAO    | NC       | VSSAO    | VDDAO  | IC1         | VSSD  | VDDD    | IC1     | VDDA     | VSSA      | VDDA  | IC1     | IC1     | D |
| E | OUT5_NEG     | OUT5_POS | VSSAO    | VSSAO    | VSSAO  | IC3         | VSSD  | VDDD    | IC1     | VSSA     | VDDA      | VSSA  | IC1     | IC1     | E |
| F | VDDAO        | VSSAO    | VSSAO    | VSSAO    | VDDAO  | VSSAO       | VSSD  | VDDD    | VSSD    | VDDD     | IC1       | VDDDO | OUT7    | VSSDO   | F |
| G | VSSAO        | VDDAO    | VSSAO    | VSSAO    | VSSAO  | VSSD        | VDDD  | IC1     | VDDD    | VSSD     | IC1       | IC1   | IC1     | IC1     | G |
| H | VDDAO        | VSSAO    | VDDAO    | VSSAO    | VSSAO  | VSSAO       | VSSD  | VDDD    | VSSD    | VDDD     | IC1       | IC1   | RST     | IN1     | H |
| J | OUT4_NEG     | OUT4_POS | VDDAO    | VSSAO    | VDDAO  | VSSAO       | VDDAO | VSSAO   | VSSA    | VDDA     | DPLL_LOCK | IC1   | IN2     | IN3     | J |
| K | VSSAO        | VSSAO    | VSSAO    | VDDAO    | VSSAO  | VDDAO       | VSSAO | VSSD    | VDDD    | VSSD     | IC1       | IC1   | I2C_SCL | I2C_SDA | K |
| L | OUT3_NEG     | OUT3_POS | VDDAO    | VSSAO    | VSSAO  | VSSAO       | VSSAO | I2C_AD1 | I2C_AD2 | CAP1     | VSSA      | CAP2  | VSSA    | CAP3    | L |
| M | VDDAO        | VSSAO    | VSSAO    | VSSAO    | VDDAO  | VSSAO       | VDDAO | VSSAO   | VSSA    | VSSA     | VSSA      | NC    | NC      | NC      | M |
| N | VSSAO        | OUT2_POS | VSSAO    | OUT1_POS | VSSAO  | IN_APLL_POS | IC2   | IC2     | VSSA    | XTAL_OUT | VSSA      | IC1   | VSSAO   | VSSA    | N |
| P | VDDAO        | OUT2_NEG | VSSAO    | OUT1_NEG | VDDAO  | IN_APLL_NEG | IC2   | IC2     | VDDA    | XTAL_IN  | VDDA      | IC1   | IC1     | VDDA    | P |
|   | 1            | 2        | 3        | 4        | 5      | 6           | 7     | 8       | 9       | 10       | 11        | 12    | 13      | 14      |   |
|   | Key:         |          |          |          |        |             |       |         |         |          |           |       |         |         |   |
|   | Diff Outputs | Outputs  | Inputs   | Power    | Ground |             |       |         |         |          |           |       |         |         |   |

Figure 2. Pin Assignment (Top View)

## 2 PIN DESCRIPTION

Table 1: Pin Description

| Name                           | Pin No.       | I/O                                    | Type            | Description <sup>1</sup>   |
|--------------------------------|---------------|--|-----------------|--|
| <b>Global Control Signal</b>   |               |  |                 |  |
| OSCI                           | A11           | I                                      | CMOS            | <b>OSCI: Crystal Oscillator Master Clock</b><br>A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.            |
| RST                            | H13           | I<br>pull-up                           | CMOS            | <b>RST: Reset</b><br>A low pulse of at least 50 $\mu$ s on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).    |
| <b>Input Clock</b>             |               |  |                 |  |
| IN1                            | H14           | I<br>pull-down                         | CMOS            | <b>IN1: Input Clock 1</b><br>Either a 25 MHz, 125 MHz or 156.25 MHz is input on this pin.  |
| IN2                            | J13           | I<br>pull-down                         | CMOS            | <b>IN2: Input Clock 2</b><br>Either a 25 MHz, 125 MHz or 156.25 MHz is input on this pin.  |
| IN3                            | J14           | I<br>pull-down                         | CMOS            | <b>IN3: Input Clock 3</b><br>Either a 25 MHz, 125 MHz or 156.25 MHz is input on this pin.  |
| IN_APLL_POS<br>IN_APLL_NEG     | N6<br>P6      | I pull-down<br>I pull-up/<br>pull-down | LVPECL/<br>LVDS | <b>IN_APLL_POS/ IN_APLL_NEG: Input Clock APLL</b><br>Direct input clock to APLL.   |
| <b>Output Clock</b>            |               |  |                 |  |
| OUT1_POS<br>OUT1_NEG           | N4<br>P4      | O                                      | LVPECL          | <b>OUT1_POS / OUT1_NEG: Positive / Negative Output Clock 1</b><br>A clock is differentially output on this pair of pins. It outputs either 125 MHz or 156.25 MHz                     |
| OUT2_POS<br>OUT2_NEG           | N2<br>P2      | O                                      | LVPECL          | <b>OUT2_POS / OUT2_NEG: Positive / Negative Output Clock 2</b><br>A clock is differentially output on this pair of pins. One of 5 copies of either 125 MHz or 156.25 MHz.            |
| OUT3_POS<br>OUT3_NEG           | L2<br>L1      | O                                      | LVPECL          | <b>OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3</b><br>A clock is differentially output on this pair of pins. One of 5 copies of either 125 MHz or 156.25 MHz.            |
| OUT4_POS<br>OUT4_NEG           | J2<br>J1      | O                                      | LVPECL          | <b>OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4</b><br>A clock is differentially output on this pair of pins. One of 5 copies of either 125 MHz or 156.25 MHz.            |
| OUT5_POS<br>OUT5_NEG           | E2<br>E1      | O                                      | LVPECL          | <b>OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5</b><br>A clock is differentially output on this pair of pins. One of 5 copies of either 125 MHz or 156.25 MHz.            |
| OUT6_POS<br>OUT6_NEG           | B3<br>A3      | O                                      | LVPECL          | <b>OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6</b><br>A clock is differentially output on this pair of pins. One of 5 copies of either 125 MHz or 156.25 MHz.            |
| OUT7                           | F13           | O                                      | CMOS            | <b>OUT7: CMOS Output Clock 7</b><br>A free run 25 MHz clock is output on this pin.   |
| <b>Miscellaneous</b>           |               |  |                 |  |
| CAP1, CAP2,<br>CAP3            | L10, L12, L14 | Output                                 | Analog          | <b>CAP1, CAP2 and CAP3: Analog Power Filter Capacitor connection 1 to 3</b><br>Connect a 10 $\mu$ F capacitor in parallel with a low ESR 100nF capacitor between these pins and VSS1 |
| XTAL_IN                        | P10           | Input                                  | Analog          | <b>Crystal oscillator input.</b><br>Crystal oscillator input for APLL.   |
| XTAL_OUT                       | N10           | Output                                 | Analog          | <b>Crystal oscillator output.</b><br>Crystal oscillator output for APLL.   |
| <b>Lock Indication Signals</b> |               |  |                 |  |
| DPLL_LOCK                      | J11           | O                                      | CMOS            | <b>DPLL lock indicator.</b><br>This pin goes high when DPLL is locked.   |

Table 1: Pin Description (Continued)

| Name                            | Pin No.  | I/O            | Type       | Description <sup>1</sup>   |
|---------------------------------|--|----------------|------------|--|
| <b>Microprocessor Interface</b> |  |                |            |  |
| INT_REQ                         | C13  | O              | CMOS       | <b>INT_REQ: Interrupt Request</b><br>This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).   |
| I2C_SCL                         | K13  | I              | Open Drain | <b>I2C_SCL: Serial Clock Line</b><br>In I2C mode, the serial clock is input on this pin.   |
| I2C_SDA                         | K14  | I/O            | Open Drain | <b>I2C_SDA: Serial Data Input/Output</b><br>In I2C mode, this pin is used as the input/output for the serial data.   |
| I2C_AD1                         | L8   | I<br>pull-up   | CMOS       | <b>I2C_AD1: Device Address Bit 1</b><br>In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.   |
| I2C_AD2                         | L9   | I<br>pull-up   | CMOS       | <b>I2C_AD2: Device Address Bit 2</b><br>In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.   |
| <b>JTAG (per IEEE 1149.1)</b>   |  |                |            |  |
| TRST                            | A14  | I<br>pull-down | CMOS       | <b>TRST: JTAG Test Reset (Active Low)</b><br>A low signal on this pin resets the JTAG test port.<br>This pin should be connected to ground when JTAG is not used.  |
| TMS                             | A12  | I<br>pull-up   | CMOS       | <b>TMS: JTAG Test Mode Select</b><br>The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.   |
| TCK                             | B10  | I<br>pull-down | CMOS       | <b>TCK: JTAG Test Clock</b><br>The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK.<br>If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.   |
| TDI                             | A8   | I<br>pull-up   | CMOS       | <b>TDI: JTAG Test Data Input</b><br>The test data is input on this pin. It is clocked into the device on the rising edge of TCK.   |
| TDO                             | B8   | O              | CMOS       | <b>TDO: JTAG Test Data Output</b><br>The test data is output on this pin. It is clocked out of the device on the falling edge of TCK.<br>TDO pin outputs a high impedance signal except during the process of data scanning.<br>This pin can indicate the interrupt of DPLL selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). |
| <b>Power &amp; Ground</b>       |  |                |            |  |
| VDDD                            | D8, E8, F8, F10, G7, G9, H8, H10, K9                                       | Power          | -          | Digital Core Power - +3.3V DC nominal  |
| VDDDO                           | B14, C7, F12   | Power          | -          | Digital Output Power - +3.3V DC nominal  |
| VDDA                            | C9, C11, C12, D10, D12, E11, J10, P9, P11, P14                             | Power          | -          | Analog Core Power - +3.3V DC nominal   |
| VDDAO                           | A2, C2, D5, F1, F5, G2, H1, H3, J3, J5, J7, K4, K6, L3, M1, M5, M7, P1, P5 | Power          | -          | Analog Output Power - +3.3V DC nominal   |
| VSSD                            | D7, E7, F7, F9, G6, G10, H7, H9, K8, K10                                   | Ground         | -          | Ground   |
| VSSDO                           | B13, C8, F14   | Ground         | -          | Ground   |
| VSSA                            | B9, B11, B12, C10, D11, E10, E12, J9, L11, L13, M9, M10, M11, N9, N11, N14 | Ground         | -          | Analog Ground  |

Table 1: Pin Description (Continued)

| Name   | Pin No.   | I/O    | Type | Description <sup>1</sup>  |
|--|---|--------|------|---|
| VSSAO  | B2, B4, D1, D2, D4, E3, E4, E5, F2, F3, F4, F6, G1, G3, G4, G5, H2, H4, H5, H6, J4, J6, J8, K1, K2, K3, K5, K7, L4, L5, L6, L7, M2, M3, M4, M6, M8, N1, N3, N5, N13, P3 | Ground | -    | Analog Output Ground  |
| Others   |   |        |      |   |
| IC1  | A6, A7, A9, A13, B6, B7, C5, C6, C14, D6, D9, D13, D14, E9, E13, E14, F11, G8, G11, G12, G13, G14, H11, H12, J12, K11, K12, N12, P12, P13                               | -      | -    | <b>IC1: Internal Connection</b><br>Internal Use. These pins should be left open for normal operation. |
| IC2  | A10, N7, N8, P7, P8   | -      | -    | <b>IC2: Internal Connection</b><br>Internal Use. These pins should be left open for normal operation. |
| IC3  | E6  | -      | -    | <b>IC3: Internal Connection</b><br>Internal Use. This pin should be left open for normal operation.   |
| NC   | A1, A4, A5, B1, B5, C1, C3, C4, D3, M12, M13, M14   | -      | -    | <b>NC: Not Connected</b><br>These pins should be left open for normal operation.                      |
| <b>Note:</b><br>1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care. |   |        |      |   |

## 2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### 2.1.1 INPUTS

#### Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

#### Differential Clock Inputs

For applications not requiring the use of a differential input, both \*\_POS and \*\_NEG can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from \_POS to ground.

### XTAL Inputs

For applications not requiring the use of a crystal oscillator input, both \_IN and \_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from \_IN to ground.

### 2.1.2 OUTPUTS

#### Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

#### Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

#### Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

PACKAGE DIMENSIONS

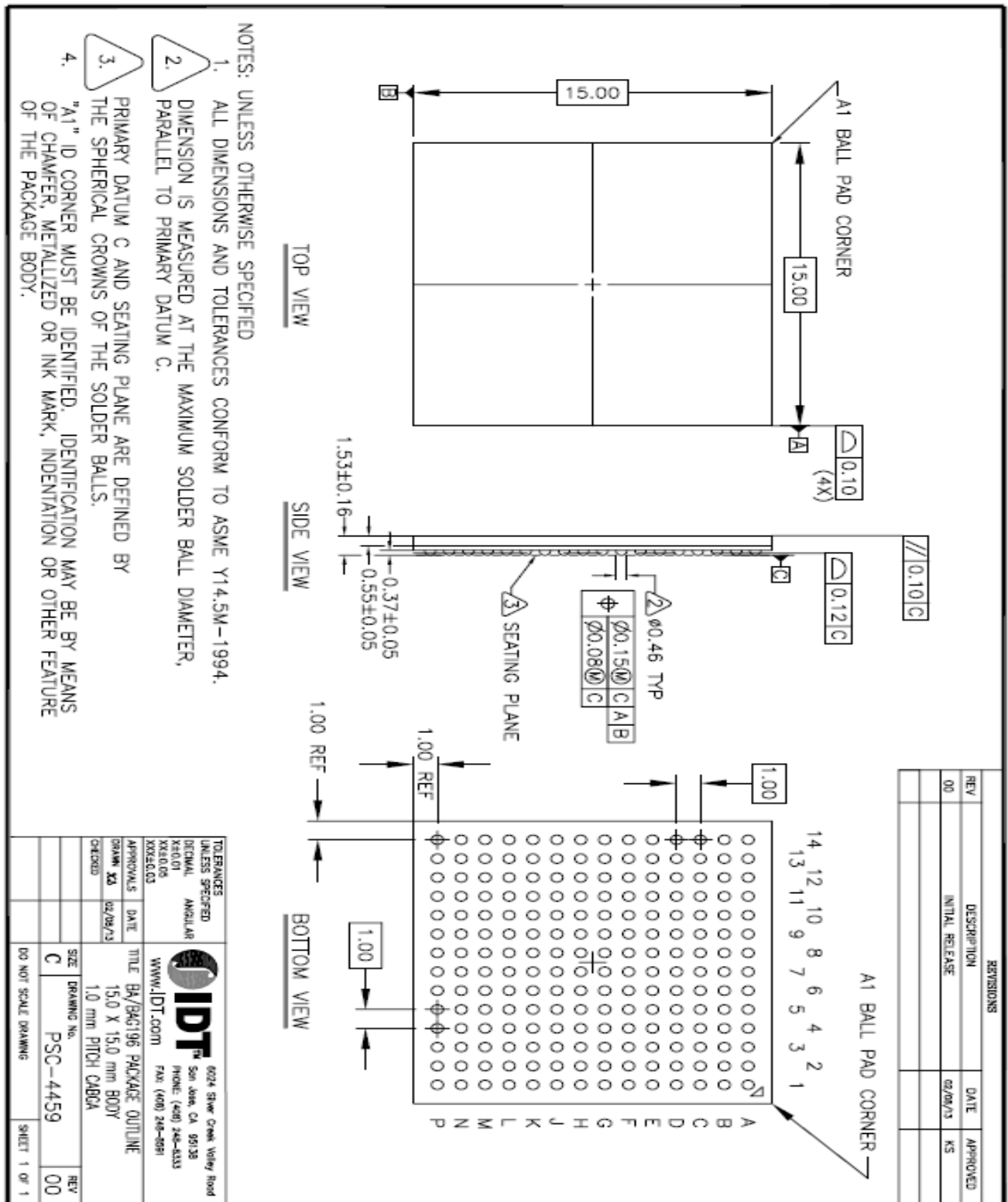
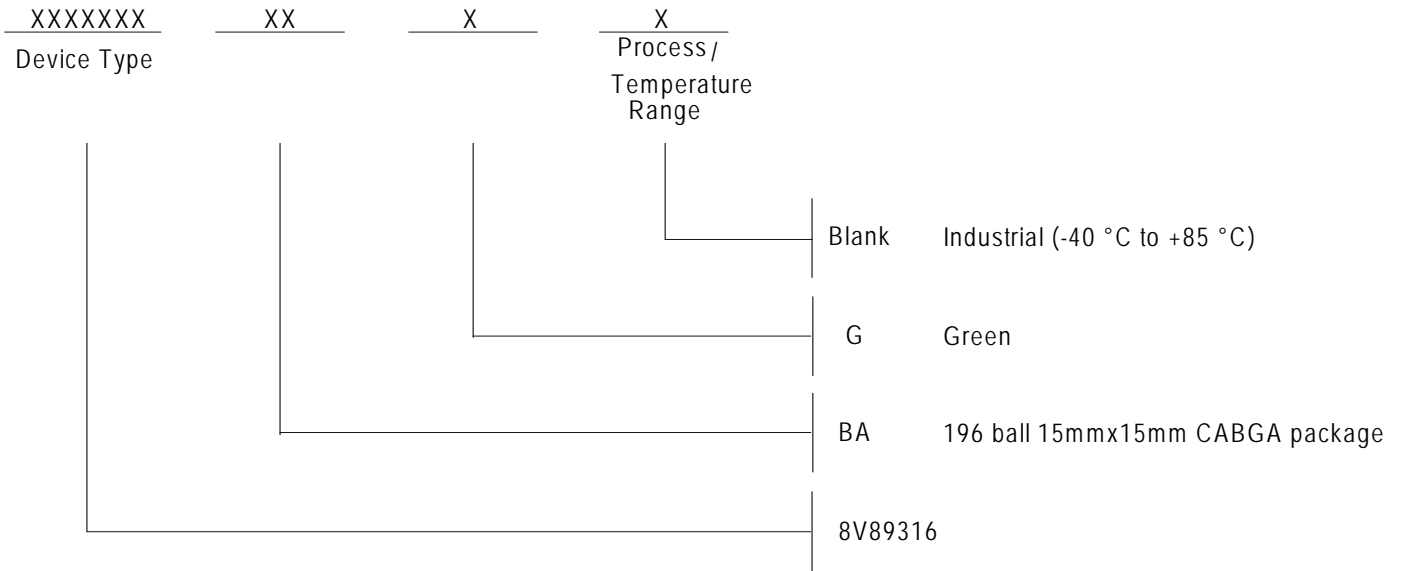


Figure 3. 196-Pin BAG Package Dimensions

### ORDERING INFORMATION



### REVISION HISTORY



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