Description

The 9DB1233 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB1233 is driven by a differential SRC output pair from an IDT 932S421 or 932SQ420 or equivalent main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without spread-spectrum clocking.

Typical Applications

- 12-output PCIe Gen3 zero-delay/fanout buffer

Output Features

- Twelve 0.7V current mode differential HSCL output pairs

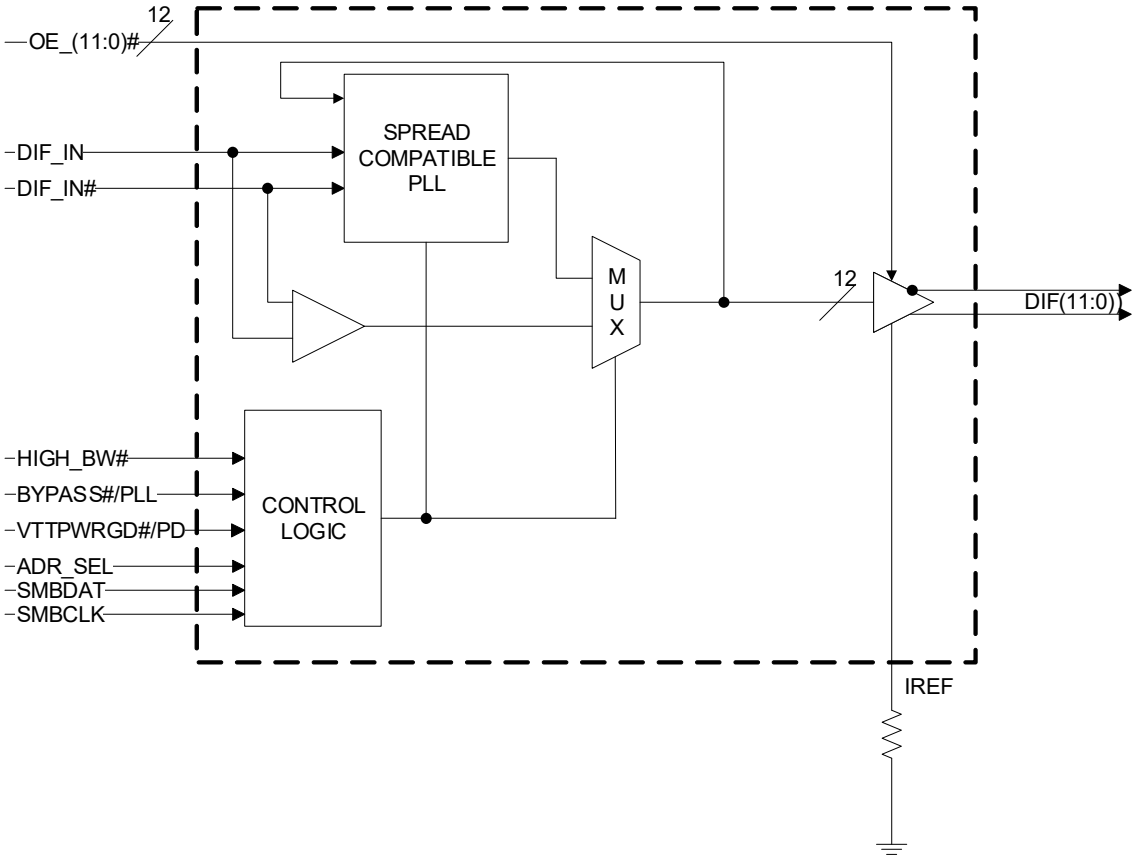
Features

- 3 selectable SMBus addresses; multiple devices can share the same SMBus segment
- 12 OE# pins; hardware control of each output
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible; tracks spreading input clock for low EMI
- SMBus interface; unused outputs can be disabled
- Undriven differential outputs in Power-down; improved power management

Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- Pin compatible with DB1200 Yellow Cover device

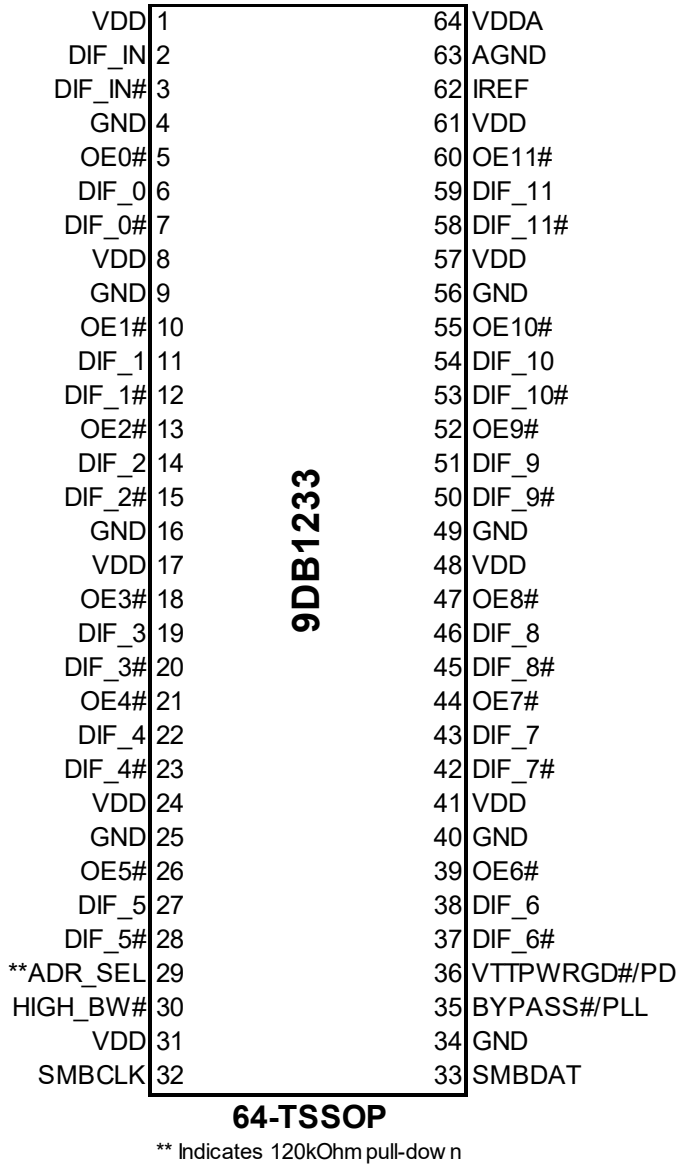
Block Diagram



Contents

Pin Assignments

Figure 1. Pin Assignments for 6.10mm Body 64-TSSOP Package – Top View



64-TSSOP

** Indicates 120kOhm pull-down

SMBus Address Selection (Pin 29)

ADR_SEL	Voltage	SMBus Adr (Wr/Rd)
Low	<0.8V	DC/DD
Mid	1.2<Vin<1.8V	D6/D7
High	Vin > 2.0V	D4/D5

Power Groups

Pin Number		Description
VDD	GND	
1	4	DIF_IN/DIF_IN#
8, 17, 24, 41, 48, 57	9, 16, 25, 40, 49, 56	DIF(11:0)
N/A	63	IREF
64	63	Analog VDD & GND for PLL core

Note: Please treat pin 1 as an analog VDD.

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	DIF_IN	IN	0.7 V Differential TRUE input
3	DIF_IN#	IN	0.7 V Differential Complementary Input
4	GND	PWR	Ground pin.
5	OE0#	IN	Active low input for enabling DIF pair 0. 1 =disable outputs, 0 = enable outputs
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential Complementary clock output
8	VDD	PWR	Power supply, nominal 3.3V
9	GND	PWR	Ground pin.
10	OE1#	IN	Active low input for enabling DIF pair 1. 1 =disable outputs, 0 = enable outputs
11	DIF_1	OUT	0.7V differential true clock output
12	DIF_1#	OUT	0.7V differential Complementary clock output
13	OE2#	IN	Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs
14	DIF_2	OUT	0.7V differential true clock output
15	DIF_2#	OUT	0.7V differential Complementary clock output
16	GND	PWR	Ground pin.
17	VDD	PWR	Power supply, nominal 3.3V
18	OE3#	IN	Active low input for enabling DIF pair 3. 1 =disable outputs, 0 = enable outputs
19	DIF_3	OUT	0.7V differential true clock output
20	DIF_3#	OUT	0.7V differential Complementary clock output
21	OE4#	IN	Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs
22	DIF_4	OUT	0.7V differential true clock output
23	DIF_4#	OUT	0.7V differential Complementary clock output
24	VDD	PWR	Power supply, nominal 3.3V
25	GND	PWR	Ground pin.
26	OE5#	IN	Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs
27	DIF_5	OUT	0.7V differential true clock output
28	DIF_5#	OUT	0.7V differential Complementary clock output
29	**ADR_SEL	IN	This tri-level input selects one of 3 SMBus addresses. See the SMBus Address Select Table for the addresses.
30	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
31	VDD	PWR	Power supply, nominal 3.3V
32	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant

Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
33	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
34	GND	PWR	Ground pin.
35	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
36	VTTPWRGD#/PD	IN	VTTPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
37	DIF_6#	OUT	0.7V differential Complementary clock output
38	DIF_6	OUT	0.7V differential true clock output
39	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
40	GND	PWR	Ground pin.
41	VDD	PWR	Power supply, nominal 3.3V
42	DIF_7#	OUT	0.7V differential Complementary clock output
43	DIF_7	OUT	0.7V differential true clock output
44	OE7#	IN	Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs
45	DIF_8#	OUT	0.7V differential Complementary clock output
46	DIF_8	OUT	0.7V differential true clock output
47	OE8#	IN	Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs
48	VDD	PWR	Power supply, nominal 3.3V
49	GND	PWR	Ground pin.
50	DIF_9#	OUT	0.7V differential Complementary clock output
51	DIF_9	OUT	0.7V differential true clock output
52	OE9#	IN	Active low input for enabling DIF pair 9. 1 =disable outputs, 0 = enable outputs
53	DIF_10#	OUT	0.7V differential Complementary clock output
54	DIF_10	OUT	0.7V differential true clock output
55	OE10#	IN	Active low input for enabling DIF pair 10. 1 =disable outputs, 0 = enable outputs
56	GND	PWR	Ground pin.
57	VDD	PWR	Power supply, nominal 3.3V
58	DIF_11#	OUT	0.7V differential Complementary clock output
59	DIF_11	OUT	0.7V differential true clock output
60	OE11#	IN	Active low input for enabling DIF pair 11. 1 =disable outputs, 0 = enable outputs
61	VDD	PWR	Power supply, nominal 3.3V
62	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
63	AGND	PWR	Analog Ground pin for Core PLL
64	VDDA	PWR	3.3V power for the PLL core.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DB1233 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Clock Input Parameters

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Current Consumption

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, C_L = Full load;		300	325	mA	1
Powerdown Current	$I_{DD3.3PD}$	All diff pairs driven		NA		mA	1
	$I_{DD3.3PDZ}$	All differential pairs tri-stated		21	30	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	10		166	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	90	100.00	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		5	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2.4	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		9.1	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	825	850	mV	1
Voltage Low	VLow		-150	0	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		859	1150	mV	1
Min Voltage	Vmin		-300				1
Vswing	Vswing	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250		550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off			140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V at Z_O = 50Ω (100Ω differential impedance).

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	3	4	MHz	1
		-3dB point in Low BW Mode	0.7	1	1.4	MHz	1
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain		1.5	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45		55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz	-2	0	2	%	1,4
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2500		4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-250		250	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%		47	50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		25	50	ps	1,3
		Additive Jitter in Bypass Mode		12	50	ps	1,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V at Z_O = 50Ω.

[3] Measured from differential waveform.

[4] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Electrical Characteristics–PCIe Phase Jitter Parameters

$T_A = T_{COM;}$ Supply voltage VDD = 3.3V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		34	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.1	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.2	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.4	1	ps (rms)	1,2,4,5
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1}$	PCIe Gen 1		2	5	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.5	0.6	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.8	1	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.35	0.5	ps (rms)	1,2,4,5, 6

[1] Applies to all outputs when driven by 932SQ420DGLF or equivalent.

[2] See http://www.pcisig.com for complete specs.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] Subject to final ratification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.4.

[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter) = SQRT{(total jitter)^2 - (input jitter)^2}.

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2,3

Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The 9DB1233 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PLL or Bypass mode.

Terminations

DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

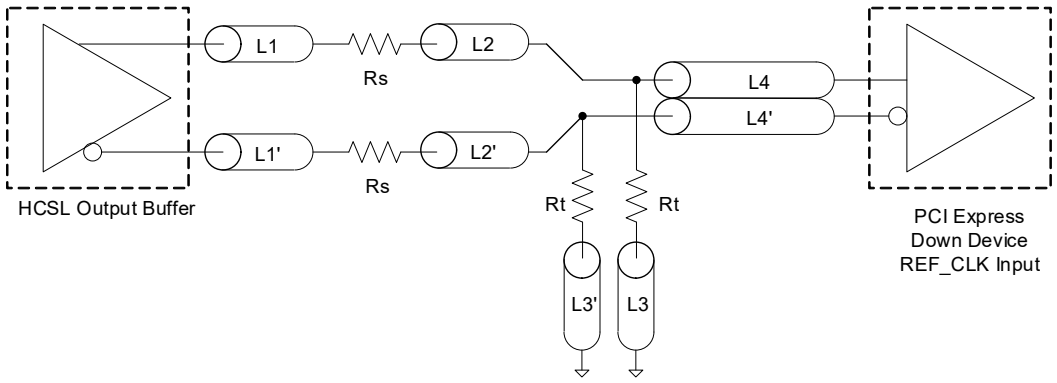
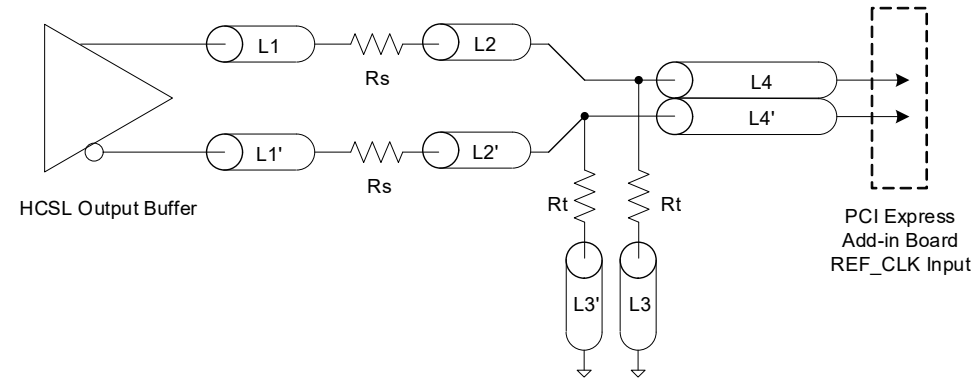


Figure 2: Differential Routing to PCI Express Controller

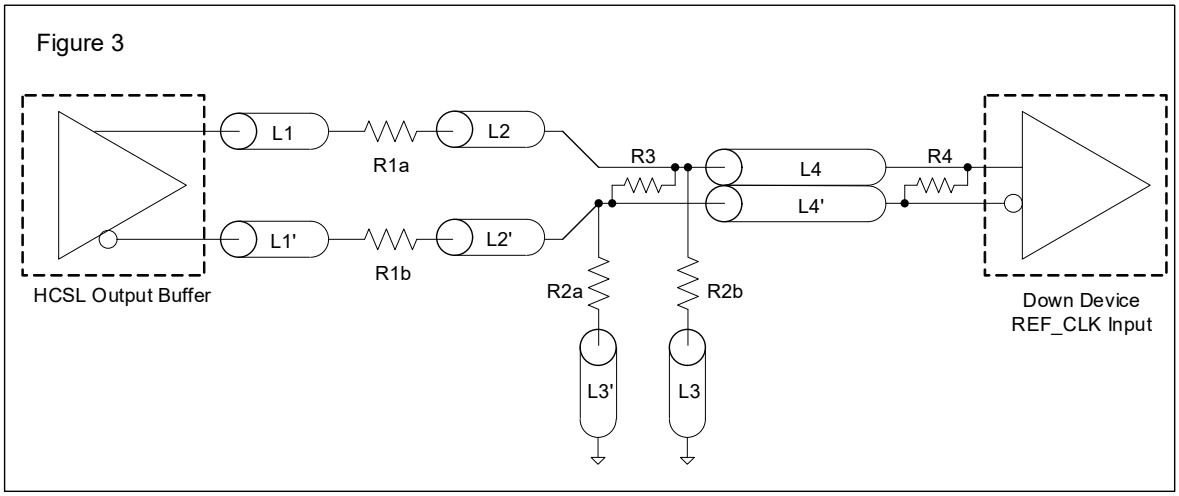


Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1

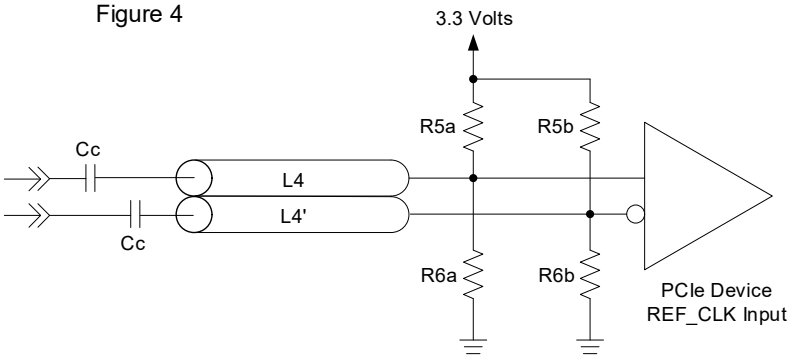
R2a = R2b = R2

Figure 3



Termination for Cable AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
			Beginning Byte N
ACK			
			O
O		X Byte	O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	HIGH_BW#	High or Low BW	RW	High BW	Low BW	Latch
Bit 6	-	BYPASS#/PLL	Bypass (non-PLL Mode) or PLL Mode	RW	Bypass	PLL	Latch
Bit 5	-	Reserved	Reserved	RW	Reserved		X
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	-	Reserved	Reserved	RW	Reserved		1
Bit 1	-	Reserved	Reserved	RW	Reserved		0
Bit 0	-	Reserved	Reserved	RW	Reserved		1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	43,42	DIF_7	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 6	38,37	DIF_6	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 5	27,28	DIF_5	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 4	22,23	DIF_4	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 3	19,20	DIF_3	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	14,15	DIF_2	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	11,12	DIF_1	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	6,7	DIF_0	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	Reserved	Reserved	RW	Reserved		0
Bit 3	58,59	DIF_11	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 2	53,54	DIF_10	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 1	50,51	DIF_9	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1
Bit 0	45,46	DIF_8	Output Control (Disable = Hi-Z)	RW	Disable	Enable	1

SMBus Table: Output Enable Readback

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	43,42	OE7#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 6	38,37	OE6#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 5	27,28	OE5#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 4	22,23	OE4#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 3	19,20	OE3#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 2	14,15	OE2#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 1	11,12	OE1#	OE# Pin Readback	R	Enabled	Disabled	X
Bit 0	6,7	OE0#	OE# Pin Readback	R	Enabled	Disabled	X

SMBus Table: Output Enable Readback

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Reserved	Reserved	R	Reserved		0
Bit 6	-	Reserved	Reserved	R	Reserved		0
Bit 5	-	Reserved	Reserved	R	Reserved		0
Bit 4	-	Reserved	Reserved	R	Reserved		0
Bit 3	58,59	OE11#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 2	53,54	OE10#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 1	50,51	OE9#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X
Bit 0	45,46	OE8#	Output Control (Disable = Hi-Z)	R	Enabled	Disabled	X

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBus Table: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	VENDOR ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	REVISION ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	1
Bit 0	-	VID0		R	-	-	0

SMBus Table: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		RW	Device ID is 0C Hex		0
Bit 6	-	Device ID 6		RW			0
Bit 5	-	Device ID 5		RW			0
Bit 4	-	Device ID 4		RW			0
Bit 3	-	Device ID 3		RW			1
Bit 2	-	Device ID 2		RW			1
Bit 1	-	Device ID 1		RW			0
Bit 0	-	Device ID 0		RW			0

SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/64-tssop-package-outline-drawing-610-mm-body-050mm-pitch-pag64d1

Marking Diagram

- Line 1 indicates the lot number.
- Line 2 indicates the following:
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
- Line 3 indicates the part number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9DB1233AGLF	6.10mm body, 64-TSSOP	Tubes	0° to +70°C
9DB1233AGLFT	6.10mm body, 64-TSSOP	Tape and Reel	0° to +70°C

"LF" after the package code denotes Pb-free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Revision Date	Description of Change
December 17, 2019	▪ Updated Byte 5 and 6. ▪ Converted datasheet to updated template.
November 14, 2010	▪ Corrected Additive phase jitter calculation in PCIe phase jitter table. ▪ Added footnotes 5 and 6 to this table.
July 12, 2010	▪ Changed 'PWD' to 'Default' in SMBus. ▪ Updated Electrical Tables. ▪ Move to Final.
July 7, 2010	Initial release.

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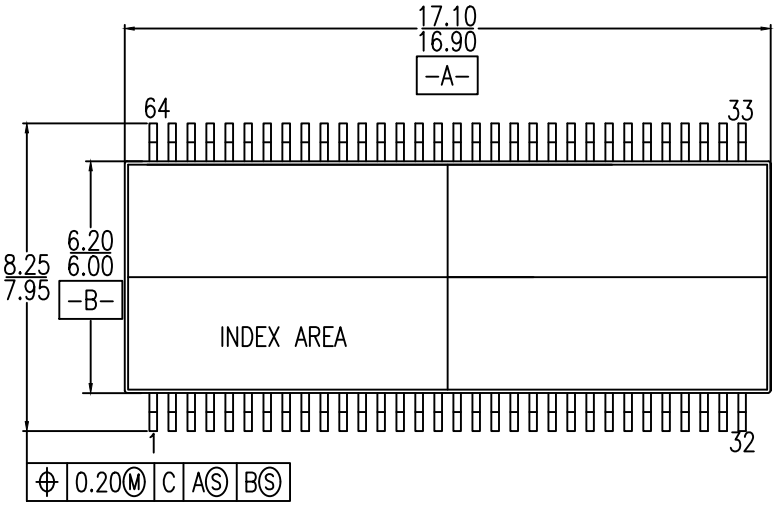
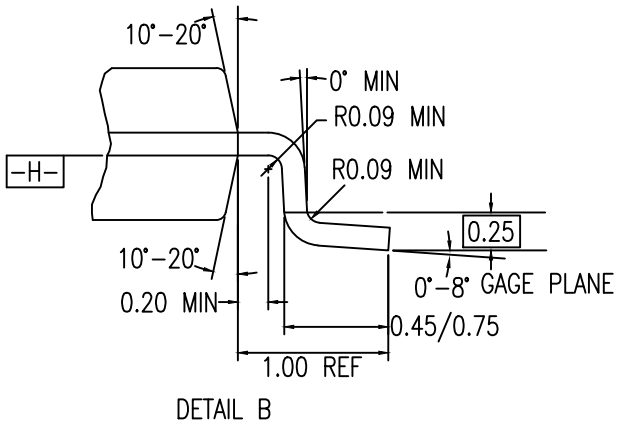
64-TSSOP Package Outline Drawing

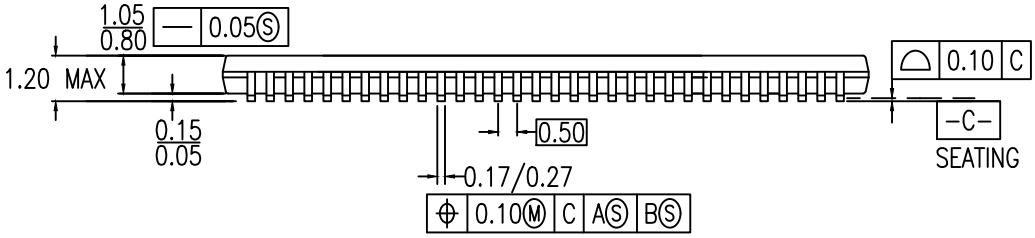
6.10 mm Body 0.50mm Pitch

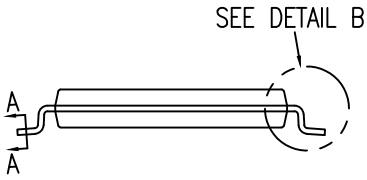
PAG64D1, PSC-4767-01, Rev 00, Page 1

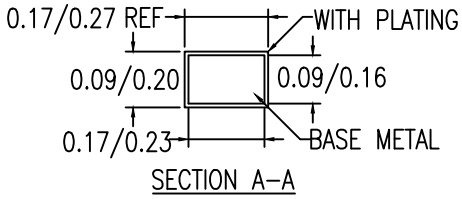




DETAIL B

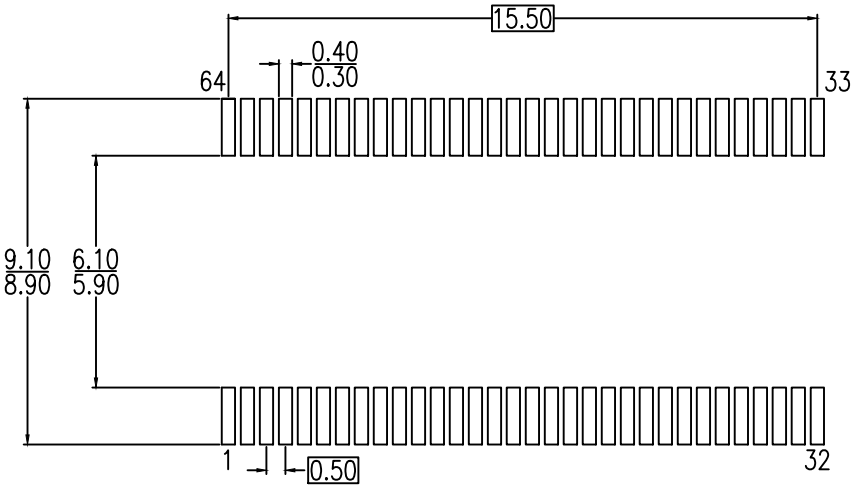






SECTION A-A

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.



RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 18, 2018	Rev 00	Initial Release